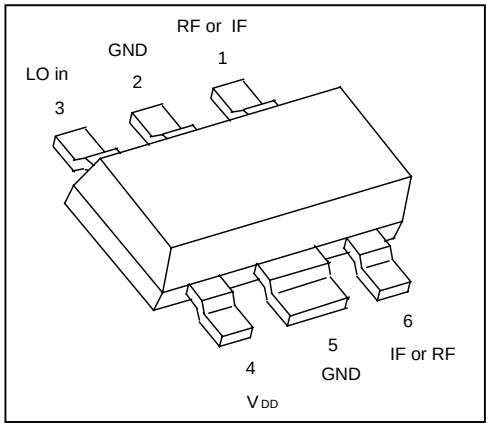
GaAs MMIC

Preliminary Data



- **Linear Mixer** with integrated LO-Buffer
- High **Input-IP3 of typical 17.5dBm**
- Very low **LO-Power demand of typ. 0dBm**
- Suited for Up- and Down-Conversion
- Wide LO-Frequency Range
  <500MHz to >2,5GHz
- Wide LO-Level Range
- Single ended Ports
- RF- and IF-Port Impedance 50 Ohm
- Operating Voltage Range: < 3 to 6V
- Very low Current Consumption of typical 2.5mA

ESD: **E**lectro**s**tatic **d**ischarge sensitive device
Observe handling Precautions!

Type	Marking	Ordering code (tape and reel)	Package [1]
CMY211	M4s	Q62702M17	MW-6

Maximum Ratings

Characteristics	Port	Symbol	Value		Unit
			min	max	
Supply Voltage	4	V_{DD}	0	6	V
DC-Voltage at LO Input	3	V_3	-3	0,5	V
DC-Voltage at RF-IF Ports [2]	1, 6	$V_{1,6}$	- 0,5	+ 0,5	V
Power into RF-IF Ports	1, 6	$P_{in,RF}$		10	dBm
Power into LO Input	3	$P_{in,LO}$		10	dBm
Channel Temperature		T_{Ch}		150	°C
Storage Temperature		T_{stg}	-55	150	°C

Thermal Resistance

Characteristics	Symbol	Value	Unit
Channel to Soldering Point (GND)	R_{thChS}	≤100	K/W

1) For detailed dimensions see page 7.

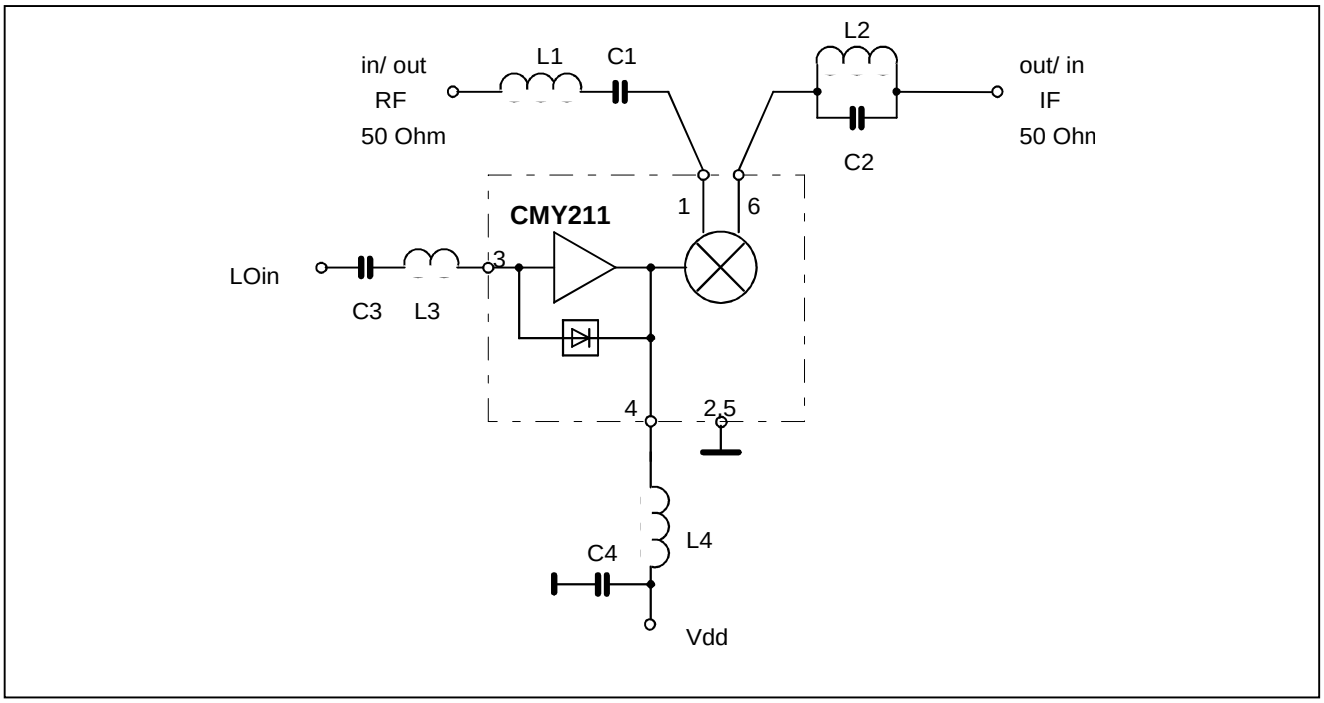
2) For DC test purposes only, no DC voltages at pins 1, 6 in application

Electrical Characteristics

Test conditions: T_a = 25°C; V_{DD}= 3V, see test circuit; f_{RF} = 808MHz; f_{LO} = 965MHz; P_{LO} = 0dBm; f_{IF} = 157MHz, unless otherwise specified:

Parameter, Test Conditions	Symbol	min	typ	max	Unit
Operating Current	I_{op}	-	2.5	-	mA
Conversion Loss	L_c	-	6.0	-	dB
SSB Noise Figure	F_{ssb}	-	6.0	-	dB
2 Tone 3rd Order IMD $P_{RF1} = P_{RF2}$ = -3dBm f_{RF1} = 806MHz; f_{RF2} = 810MHz; f_{LO} =965MHz	d_{IM3}	-	41	-	dBc
3rd Order Input Intercept Point	$IP3_{in}$	-	17.5	-	dBm
P_{-1dB} Input Power	P_{-1dB}	-	tbf.	-	dBm
LO Leakage at RF/IF-Port (1,6)	$P_{LO\ 1,6}$	-	-13	-	dBm

Test circuit / application example



Notes for external elements:

L1, C1: Filter for upper frequency;
C2, L2: Filter for lower frequency;
each filter is a throughpath for the desired frequency (RF or IF) and isolates the other frequency (IF or RF) and its harmonics.
These two filters must be connected to pin 1 and pin 6 directly.
Parasitic capacitances at the ports 1 and 6 must be as small as possible.
L4 and C4 are optimized by indicating lowest I_{op} at used LO-frequency; same procedure for L3.
The ports 1, 3 and 6 must be DC open.

Element values for 800MHz test and application circuit:

f *LO*	F *RF*	F *IF*	L1	C1	L2	C2	L3	C3	L4	C4
MHz	MHz	MHz	nH	pF	nH	pF	nH	pF	nH	pF
965	808	157	8.2	3.9	8.2	3.9	6.8	47	15	33

PCB-Layout for 800MHz test and application circuit:

General description and notes:

The CMY 211 is an all port single ended general purpose Up- and Down-Converter.
It combines small conversion losses and excellent intermodulation characteristics with a low demand of LO- and DC-power.
The internal level controlled LO-Buffer enables a good performance over a wide LO level range. The internal mixers principle with one port RF and IF requires a frequency separation at pin 1 and 6 respectively.

Note 1:
Best performance with lowest conversion loss is achieved when each circuit or device for the frequency separation meets the following requirements:

Input Filter: Throughpass for the signal to be mixed; reflection of the mixed signal and the harmonics of both.

Output Filter: Throughpass for the mixed signal and reflection of the signal to be mixed and the harmonics of both.

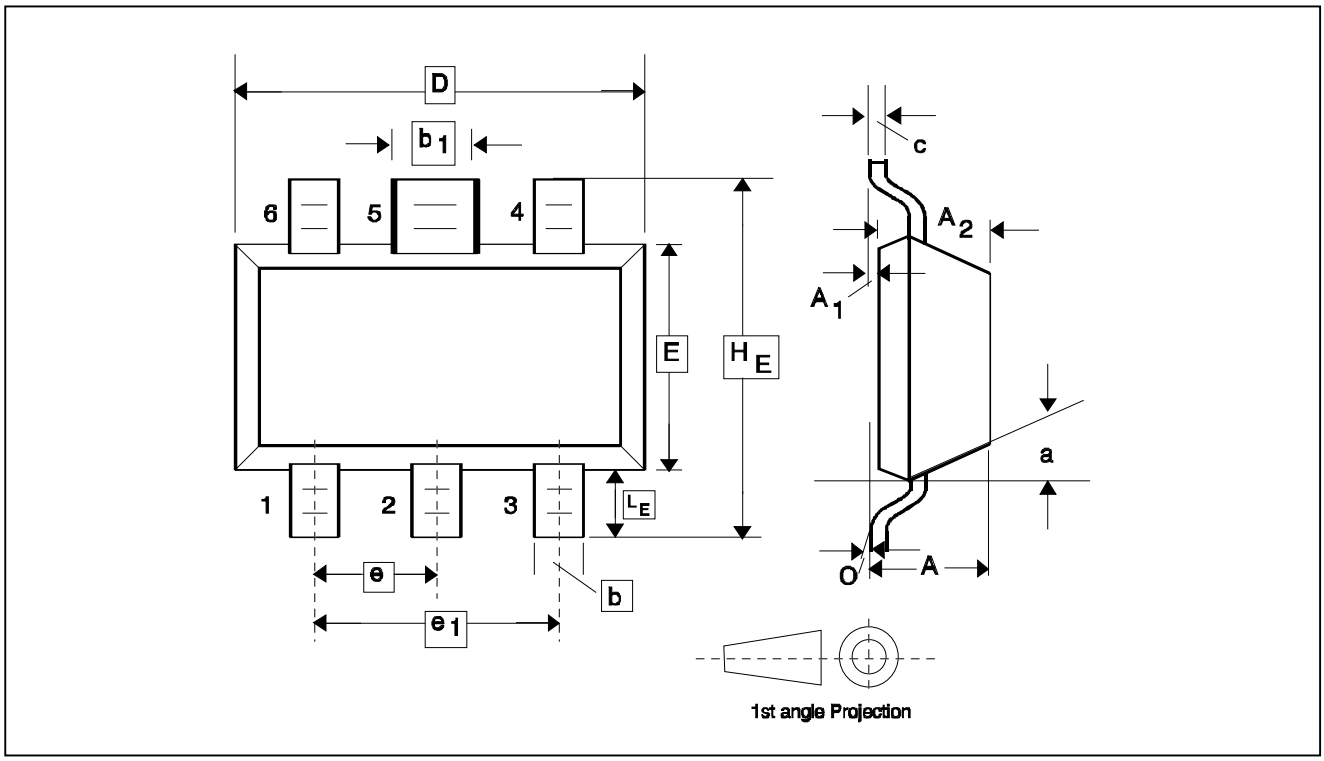
The impedance for the reflecting frequency range of each filter toward the ports 1 and 6 should be as high as possible.
In the simplest case a series- and a parallel- resonator circuit will meet these requirements but also others as appropriate drop in filters or micro stripline elements can be used.
The two branches with filters should meet immediately at the package leads of the port 1 and 6. Parasitic capacitances at these ports must be kept as small as possible.
The mixer also can be driven with a source- and a load impedance different to 50Ω, but performance will degrade at larger deviations.

Note 2:

The LO-Buffer needs an external inductor L4 at port 4; the value of inductance depends on the LO frequency. It is tuned for minimum I_{op} consumption into port 4.

Note 3:
The LO Input impedance at Port 3 can be matched with a series inductor. It also can be tuned for a minimum current I_{op} into port 4. C3 is a DC blocking capacitor.
Since the input impedance of port 3 can be slightly negative at lower frequencies, the source reflection coefficient should be kept below 0.8 ($Z_0 = 50\ \Omega$) within this frequency range.
The Conversion Noise Figure Fssb is corresponding with the value of Conversion Loss L_c.
The LO signal must be clean of noise and spurious at the frequencies $f_{LO} \pm f_{IF}$.

Semiconductor Device Outline MW-6



Dim.	min.	nom.	max.	Gradient	Remark
A			1.1		
A_1			0.1		
A_2			1.0		
b		0.3			
b_1		0.6			
c	0.08		0.15		
D	2.8		3.0		
E	1.2		1.4		
|e|		0.95			
$\|e_1\|$		1.9			
H_E			2.6		
L_E			0.6		
a				max 10°	1
q				2°...30°	

1. Applicable on all case top sides

Published by Siemens AG, Bereich Halbleiter, Marketing-Kommunikation,
Balanstraße 73, D-81541 München.

As far as patents or other rights of third parties are concerned, liability is only assumed for components per se, not for applications, processes and cirucits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

For questions on technology, delivery, and prices please contact the Offices of Semiconductor Group in Germany or the Siemens Companies and Representatives worldwide (see address list).

Due to technical requirements components may contain dangerous substances. For information on the type in question please contact your nearest Siemens Office, Semiconductor Group.

Siemens AG is an approved CECC manufacturer.