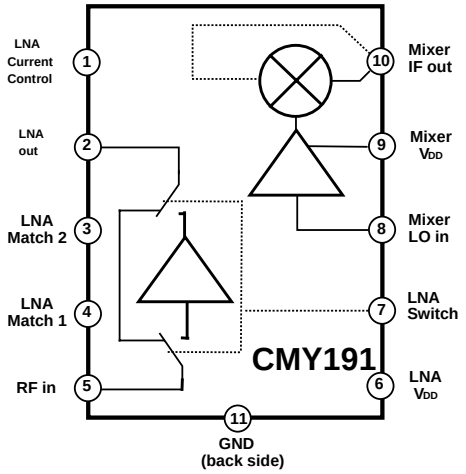
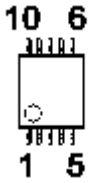
Preliminary Datasheet

- Ultralinear Mixer with integrated high IP3i LNA and LO-Buffer for PCS - CDMA receiver applications.
- Bypass switch for LNA integrated.
- Mixer Input IP3 of typical 24dBm.
- LNA + Mixer mode (3V; 15mA; f= 1.96GHz; @ Gc = 7.5dB; Ip3i = +5.5dBm; NF = 3.5dB typical)
- Low LO - Power demand of typ. 0dBm
- RF–Frequency Range 1.9GHz...2.0GHz
- Operating Voltage Range: 2.6 to 5V
- Total current consumption of typical 21mA

ESD: **E**lectro**s**tatic **d**ischarge sensitive device
Observe handling Precautions!





Type	Marking	Ordering code (tape and reel)	Package [1)]
CMY191	**tbd.**	**tbd.**	**TSSOP-10**

Maximum Ratings	**Port**	**Symbol**	**Value**		**Unit**
			min	**max**	
Supply Voltage	6,9	V_{DD}	0	5	V
DC-Voltage at LO Input	8	V_8	-3	0,5	V
DC-Voltage at Mixer IF Port	10	V_{10}	- 0,5	+ 0,5	V
Power into Mixer IF Port	10	P_{RF}		10	dBm
Power into LO Input	8	$P_{in,LO}$		10	dBm
Channel Temperature		T_{Ch}		150	°C
Storage Temperature		T_{stg}	-55	150	°C

Thermal Resistance			
Channel to Soldering Point (GND)	R_{thChS}	### tbd	K/W

Electrical Characteristics - Downconverter

Parameter,	Comment	min	typ	max	Unit
RF - frequency range	external match	1.90	-	2.050	GHz
LO - Frequency range	external match	0.5	-	2.5	GHz
IF Frequency range	external match	0.01		1	GHz

Test conditions: T_a = 25°C; V_{DD}= 3V, Vcurrent ctrl. = 3V; Vswitch ctrl = 3V; f_{RF} = 1960MHz; f_{LO} = 1750MHz; P_{LO} = 0dBm; f_{IF} = 210MHz, Zs = ZL = 50Ohm; unless otherwise specified

Parameter, Test Conditions	Symbol	min	typ	max	Unit
Total operating Current (LNA + Mixer) (LNA - current tunable by external resistor)	I_{op}	-	21	-	mA
Conversion Gain	G_c	-	8.0	-	dB
SSB Noise Figure	F_{ssb}	-	3.5	-	dB
RFInput -/ IFoutput return loss	RFIrl / IFOrl		>10		dB
3rd Order Input Intercept Point	IP3i	-	5.5	-	dBm

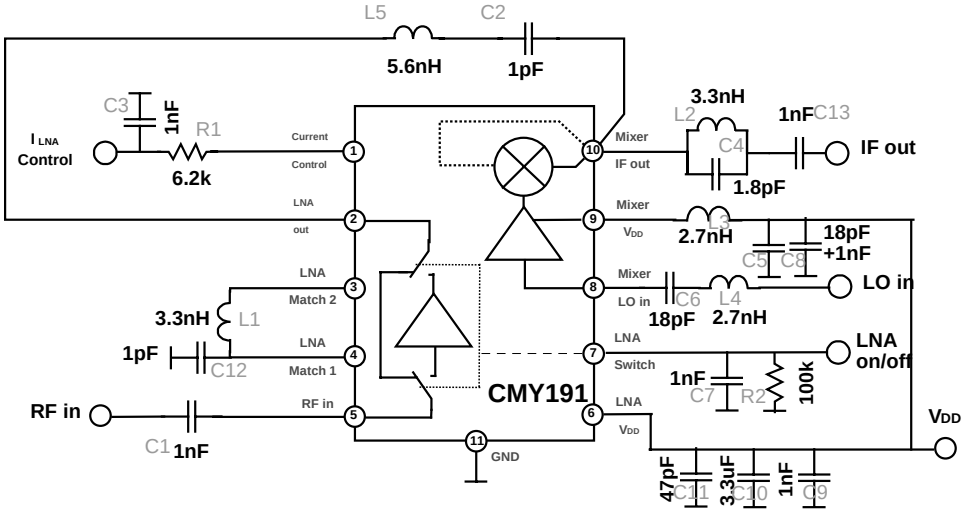
Electrical Characteristics of Mixer section “Bypass Mode”

Test conditions: T_a = 25°C; V_{DD}= 3V, Pin 1 “Vcurrent ctrl” open; Vswitch ctrl = 0V; f_{RF} = 1960MHz; f_{LO} = 1750MHz; P_{LO} = 0dBm; f_{IF} = 210MHz, unless otherwise specified:

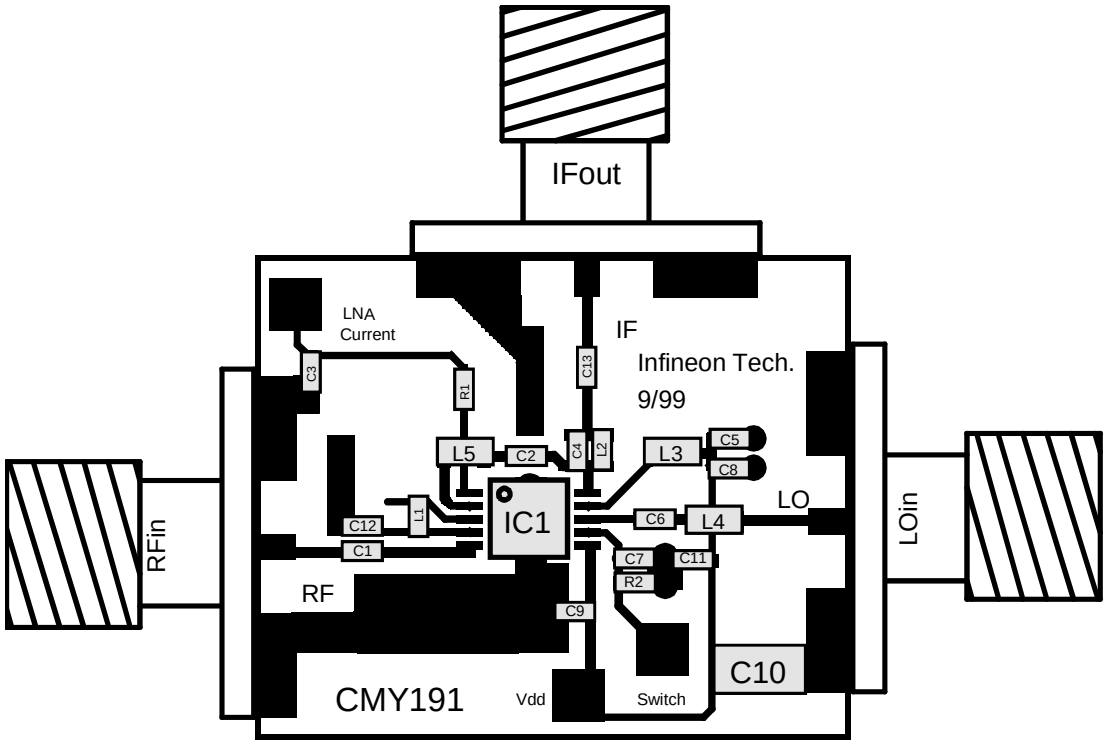
Parameter, Test Conditions	Symbol	min	typ	max	Unit
Operating Current	I_{op}	-	6	-	mA
Conversion Loss	L_c	-	8.5	-	dB
SSB Noise Figure	F_{ssb}	-	9.0	-	dB
2 Tone 3rd Order IMD $P_{RF1} = P_{RF2}$ = -3dBm f_{RF1} = 1959.5MHz; f_{RF2} = 1960.5MHz	d_{IM3}	-	52	-	dBc
RFInput -/ IFoutput return loss	RFIrl / IFOrl		>10		dB
3rd Order Input Intercept Point	$IP3_{in}$	-	24	-	dBm

1) LNA uses an LO - power feeded negative voltage generator; Therefore an LO-power of -5dBm minimum is required to operate the LNA

Testcircuit:



PCB Layout:



General description and notes for CMY191:

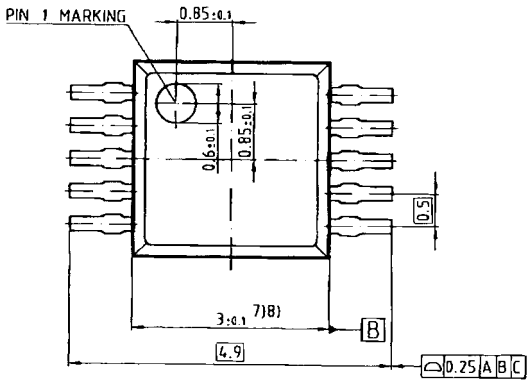
CMY191 is downconverter device for PCS-CDMA receiver applications. It combines a bypassable high IP3 single stage LNA and an ultralinear mixer + LO - driver in a TSSOP10 package. An integrated negative voltage generator allows to operate the device with one positive supply voltage. The LNA operating current can be changed by a discrete resistor R1. If the operating current of the LNA is changed significantly, the RF - input match might have to be optimised. This can be done by changing the position of C9 and/or L1 on the PCB or tuning the value of L1. Placing C9 closer to the mixer device rises gain, but lowers IP3 and input match. Moving L1 closer to CMY191 rises the resonance frequency of the input match. In order to avoid unwanted variations of the operating current, the voltage applied to the current control pin should be stable.
Switch control (pin 7) controls the bypass and connects/disconnects LNA RF path. It does not turn on/off the LNA. To shut down the LNA, you have to disconnect LNA Current Control (pin 1), which is usually connected to Vdd or a D/A converter with series resistor R1. Please note that even in shut down operation a typical LNA rest current of 20uA may occur. If LNA Current Control (pin 1) is not open but connected to ground, the LNA shut down current may increase to about 100 uA typ..

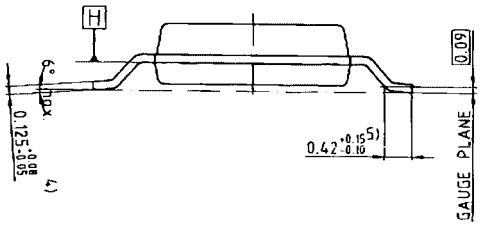
The mixersection of CMY191 is an all port single ended general purpose Down-Converter.
It combines small conversion losses and excellent intermodulation characteristics with a low demand of LO- and DC-power.
The internal level controlled LO-Buffer enables a good performance over a wide LO level range. The Conversion Noise Figure Fssb in bypass mode is corresponding with the value of Conversion Loss L_C.
The attached application hints will help to tune the mixersection for best performance:

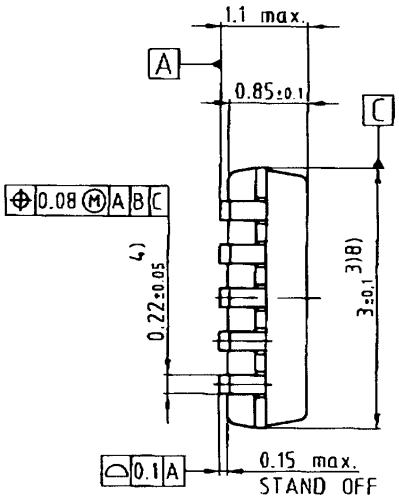
Application hints.:

- Parallel resonant circuit L2, C4 at pin 10 should be tuned for f_{RF} and passes through f_{IF}.
- L3 and C5 are tuned for lowest operating current at used LO-frequency
- ports 10 and 8 have to be decoupled from DC
- parasitic capacitance to GND at port 10 must be as low as possible
- Since the input impedance of port 1 can be slightly negative at lower frequencies, the source reflection coefficient should be kept below 0.8 (Z0 = 50Ω within this frequency range.
- The LO signal must be clean of noise and spurious at the frequencies $f_{LO} \pm f_{IF.}$

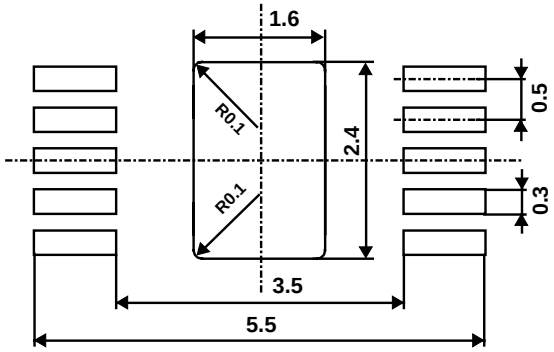
Semiconductor Device Outline TSSOP-10







Footprint **(in mm)**



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