Ultra-Low-Power System-on-a-Chip with LCD Controller

FEATURES

- **Ultra low power**
  - — Designed for applications that require long battery life while using standard AA/AAA batteries or rechargeable cells
  - — Average 45 mW/66 mW in normal operation (2.7 V/3.3 V, 13 MHz/18.432 MHz)
  - — Average 15 mW in idle mode (clock to the CPU stopped, everything else running)
  - — Average 15 µA in standby mode (realtime clock on, everything else stopped)
- **LCD controller**
  - — Interfaces directly to a single-scan panel monochrome LCD
  - — Panel width size is programmable from 16 to 1024 pixels in 16-pixel increments
  - — Video frame size programmable up to 128 Kbytes
  - — Bits per pixel programmable from 1, 2, or 4
- **Performance matching 33-MHz Intel® '486-based PC**

(cont.)

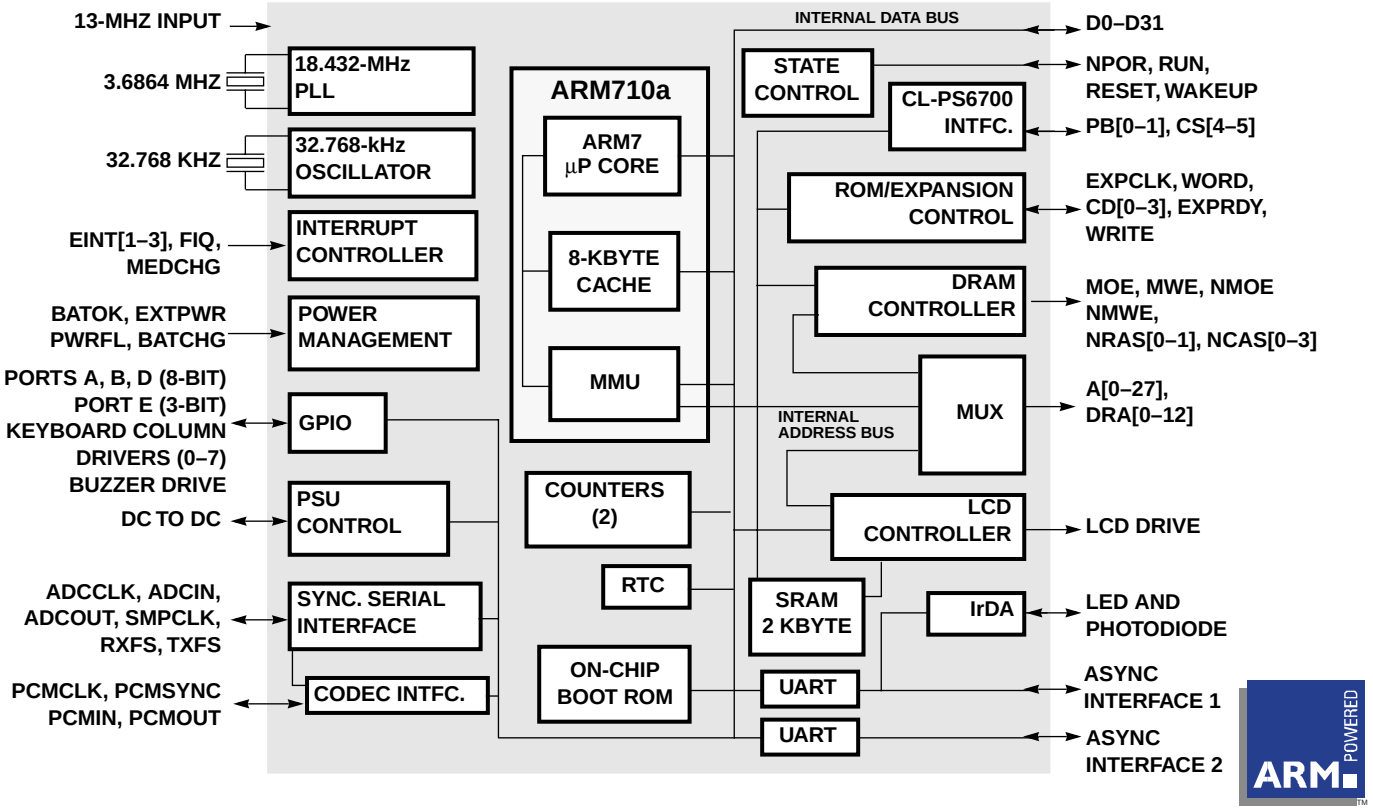
OVERVIEW

The CL-PS7111 is designed for ultra-low-power applications such as organizers/PDAs, two-way pagers, smart cellular phones, and industrial hand-held information appliances. The core-logic functionality of the device is built around an ARM710a microprocessor with 8 Kbytes of four-way set-associative unified cache.

At 18.432 MHz (for 3.3-V operation), the CL-PS7111 delivers roughly the same level of performance offered by a 33-MHz Intel® '486-based PC.

(cont.)

Functional Block Diagram



FEATURES (cont.)

- **ARM710a microprocessor**
  - — ARM7 CPU
  - — 8 Kbytes of four-way set-associative cache
  - — MMU with 64-entry TLB (transition look-aside buffer)
- **DRAM controller**
  - — Supports both 16- and 32-bit-wide DRAMs
- **ROM/SRAM/flash memory control**
  - — Decodes 4, 5, or 6 separate memory segments of 256 Mbytes
  - — Each segment can be configured as 8, 16, or 32 bits wide and supports page-mode access
  - — Programmable access time for conventional SRAM/ROM/flash memory
- **2 Kbytes of on-chip SRAM for fast program execution or as a frame buffer**
- **On-chip boot ROM**
- **Two synchronous serial interfaces**
  - — Supports SPI®[1] or Microwire®[2]-compatible
  - — Audio codec
- **27-bit general-purpose I/O**
  - — Three 8-bit and one 3-bit GPIO port
  - — Supports scanning keyboard matrix
- **Two UARTs**
  - — Supports bit rates up to 115.2 kbps
  - — Contains two 16-byte FIFOs for Tx and Rx
  - — Supports modem control signals
- **SIR (slow — up to 115.2 kbps — infrared) encoder**
  - — IrDA (Infrared Data Association) SIR protocol encoder can be optionally switched into Tx and Rx signals of UART1 up to 115 kbps
- **DC-to-DC converter interface**
  - — Provides two 96-kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16)
- **Timer and counters**
- **3.3 V at 18.432 MHz and 2.7 V at 13 MHz**
- **208-pin LQFP or new 256-lead PBGA packages**
- **Evaluation kit available with BOM, schematics, and design database**
- **Support for up to two ultra-low-power CL-PS6700 PC Card controllers**

[1] SPI is a registered trademark of Motorola®.

[2] Microwire is a registered trademark of National Semiconductor®.

OVERVIEW (cont.)

Power Management

The CL-PS7111 is designed for ultra-low-power operation. There are three basic power states:

- **Standby —** This state is equivalent to the computer being switched off (no display), and the main oscillator shut down.
- **Idle —** In this state**,** the device is functioning and all oscillators are running, but the processor clock is halted while waiting for an event such as a key press.
- **Operating —** This state is the same as the idle state, except that the processor clock is running.

Memory Interface

There are two main external memory interfaces and a DMA controller that fetches video display data for the LCD controller from main DRAM memory.

The SRAM/ROM-style interface has programmable wait-state timings and includes burst-mode capability, with six chip selects decoding six 256-Mbyte sections of addressable space. For maximum flexibility, each bank can be specified to be 8, 16, or 32 bits wide to enable the use of low-cost memory in a 32-bit system. The system can have an 8-bit-wide boot option to optimize memory size.

The programmable 16- or 32-bit-wide DRAM interface allows direct connection of up to two banks of DRAM, each bank containing up to 256 Mbytes. To assure the lowest possible power consumption, the CL-PS7111 supports self-refresh DRAMs, which are placed in a low-power state by the device when it enters low-power standby mode.

Serial Interface

For RS-232 serial communications, the CL-PS7111 includes two UARTs, both of which have two 16-byte FIFOs for receive and transmit data. The UARTs support bit rates of up to 115.2 kbps. An IrDA SIR protocol encoder/decoder can be optionally switched into the Rx/Tx signals to/from one of the UARTs to enable these signals to drive an infrared communication interface directly.

A full-duplex codec interface allows direct connection of a standard audio codec chip to the CL-PS7111, allowing storage and playback of

OVERVIEW (cont.)

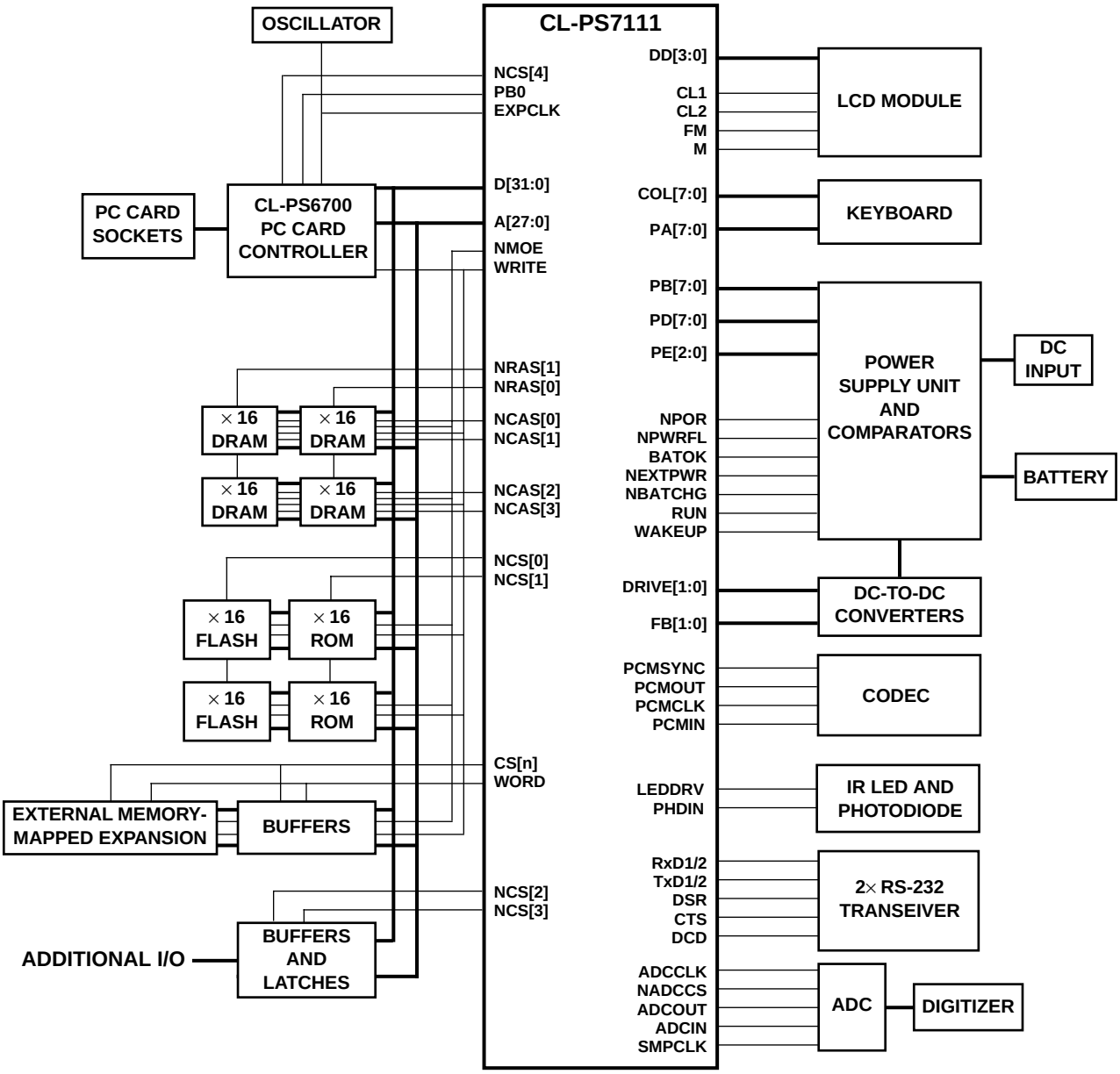
sound. A separate synchronous serial interface supports two industry-standard protocols (SPI® and Microwire®) for interfacing to standard devices (like an ADC), allowing for peripheral expansion (for example, a digitizer pen).

Packaging

The CL-PS7111 is available in a 208-pin LQFP package and a new 256-lead PBGA package.

System Design

As shown in the system block diagram below, simply adding desired memory and peripherals to the highly integrated CL-PS7111 completes a low-power device system board. All the interface logic is integrated on-chip.



A CL-PS7111–Based System

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