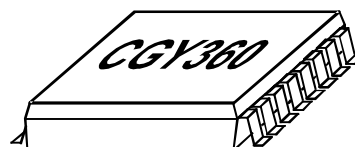


WLL Receive Downconverter IC for 3.5GHz

- Fully Integrated Two-Stage Preamplifier, Mixer, LO-Buffer, IF Amplifier and two Switched Attenuators
- Very high Input-IP3 of typical +5 dBm at max. gain and +28 dBm at min. gain
- Very low LO-Power demand of typ. -5 to 0 dBm
- High Conversion Gain: typ. 19dB
- Minimum of external components and easy matching
- Total Current Consumption: typ. 90mA @ 5V
- Temperature Range: -40°C to +85°C

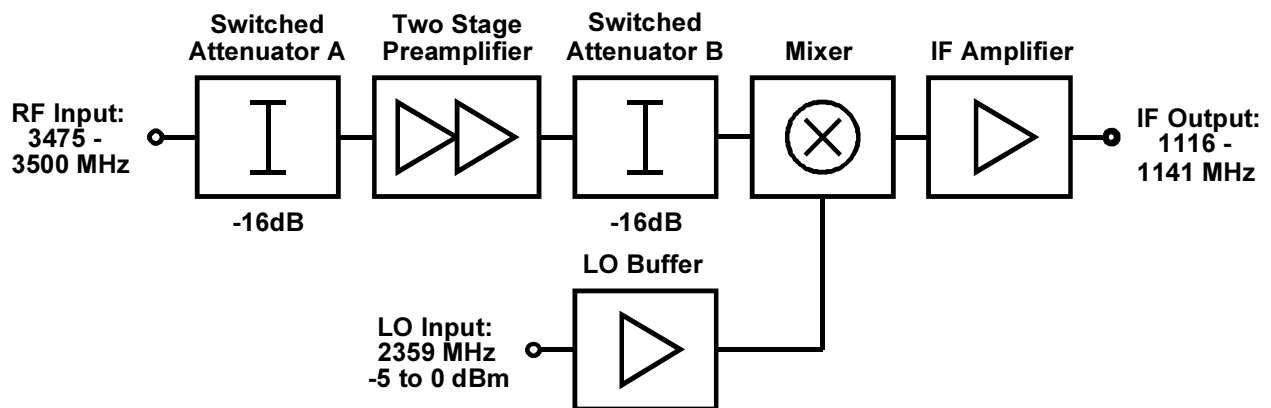


ESD: **E**lectro**s**tatic **d**ischarge sensitive device
Observe handling Precautions!

Type	Marking	Ordering code (tape and reel)	Package
CGY360	CGY360	T.b.d.	MW-16

Maximum Ratings	Port	Symbol	Value		Unit
			min	max	
Positive Supply Voltage	3, 4, 11, 15	$V_{DLO}, V_{DRF2},$ V_{DRF1}, V_{DIF}	0	+6	V
Negative Supply Voltage	13	V_G	0	-6	V
Voltage at Step Attenuators	6, 7, 9, 10	A, A bar, B bar, B	0	+6	V
Power into RF Input	8	RF		10	dBm
Power into LO Input	1	LO		10	dBm
Channel Temperature		T_{Ch}		150	°C
Storage Temperature		T_{stg}	-55	150	°C
Thermal Resistance					
Channel to Soldering Point (GND)		R_{thChS}	T.b.d.		K/W

RF Block Diagram



Electrical Characteristics

Test conditions: $T_a = 25^\circ\text{C}$; $V_{DD} = 5\text{V}$, $V_{GG} = -5\text{V}$; $f_{RF} = 3475\text{-}3500\text{ MHz}$; $f_{LO} = 2359\text{ MHz}$; $P_{LO} = 0\text{ dBm}$; $P_{RF} = -20\text{ dBm}$; $f_{IF} = 1116\text{-}1141\text{ MHz}$, attenuators “OUT” or “IN”:

Parameter, Test Conditions	Symbol	min	typ	max	Unit
Operating Drain Current	I_{op}	-	90	-	mA
Operating Drain Current LO Buffer only ($P_{LO} = 0\text{ dBm}$)	I_{LO}	-	10	-	mA
Operating Gate Current	I_g	-	0.7	-	mA

Test conditions: As above, but attenuators “OUT” (for further information about the attenuators see “Attenuator State” on page 5).

Parameter, Test Conditions	Symbol	min	typ	max	Unit
Conversion Gain	G_c	-	19,0	-	dB
SSB Noise Figure	F_{ssb}	-	6,0	-	dB
3rd Order Input Intercept Point at max. gain	$IP3_{in}$	-	+5	-	dBm
LO Leakage at RF-Port with 0 dBm LO Input	P_{LO}	-	-28	-	dBm
LO Leakage at IF-Port with 0 dBm LO Input	P_{LO}	-	-19	-	dBm
Return Loss RF Port ¹⁾	S_{11}	-	14	-	dB
Return Loss IF Port ¹⁾	S_{22}	-	11	-	dB
Return Loss LO Port ¹⁾	S_{11}	-	9	-	dB

Test conditions: As above, but attenuator A “OUT” and attenuator B “IN” or attenuator A “IN” and attenuator B “OUT” (for further information about the attenuators see “Attenuator State” on page 5).

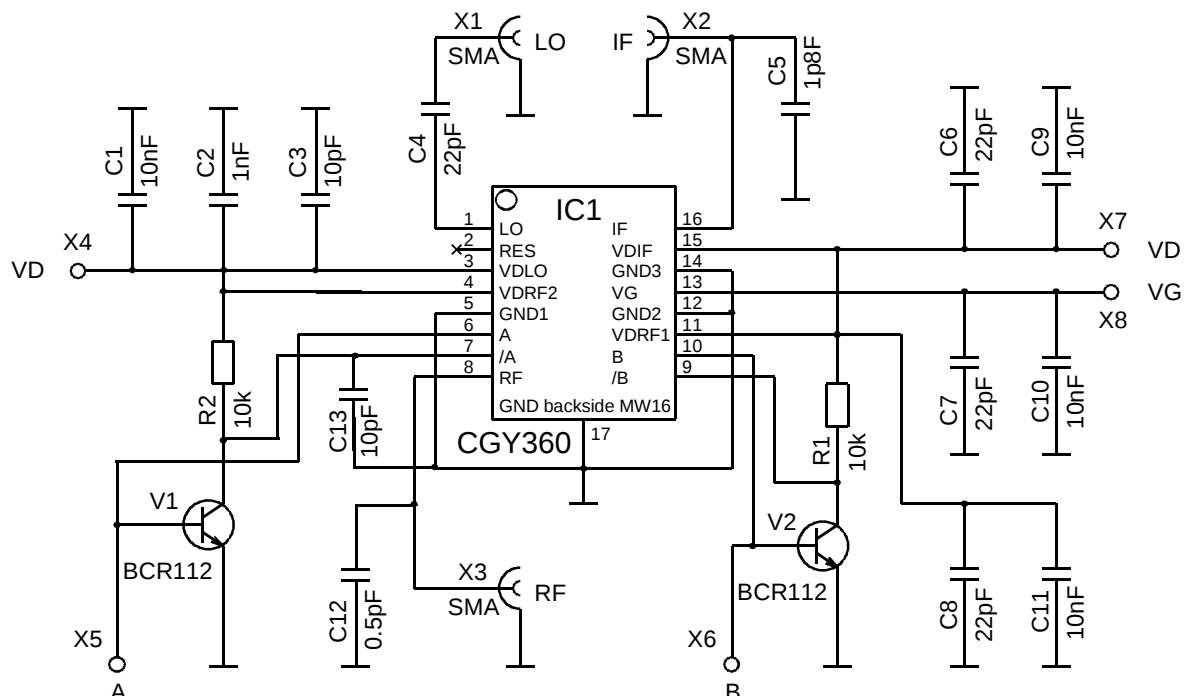
Parameter, Test Conditions	Symbol	min	typ	max	Unit
Conversion Gain	G_c	-	3,0	-	dB
SSB Noise Figure (A "IN", B "OUT")	F_{ssb}	-	16,0	-	dB
3rd Order Input Intercept Point (A "IN", B "OUT")	$IP3_{in}$	-	+18	-	dBm

Test conditions: As above, but attenuator A "IN" and attenuator B "IN" (for further information about the attenuators see "Attenuator State" on page 5).

Parameter, Test Conditions	Symbol	min	typ	max	Unit
Conversion Gain	G_c	-	-13,0	-	dB
SSB Noise Figure	F_{ssb}	-	35,0	-	dB
3rd Order Input Intercept Point at min. gain	$IP3_{in}$	-	+28	-	dBm

Note 1: Configuration as shown on application board

Application Circuit



Notes: Package of capacitor C12: 0402.

Package of all other capacitors and of all resistors: 0603.

The attenuators A and B are "OUT" without supplying the ports A and B (for further information about the attenuators see "Attenuator State" on page 5).

Pin Definitions and Functions

Pin No.	Symbol	Function	Bias Voltage
1	LO	LO Input	---
2	Res	Reserved	Leave open
3	VDLO	Mixer Drain Bias	+5V
4	VDRF2	2 nd RF Amp Drain Bias	+5V
5	GND1	GND	0V
6	A	1 st Attenuator Control	+5V, 0V
7	A bar	1 st Attenuator Control bar	0V, +5V
8	RF	RF Input	---
9	B bar	2 nd Attenuator Control bar	+5V, 0V
10	B	2 nd Attenuator Control	0V, +5V
11	VDRF1	1 st RF Amp Drain Bias	+5V
12	GND2	GND	0V
13	VG	Amplifier Gate Bias	-5V
14	GND3	GND	0V
15	VDIF	IF Amp Drain Bias	+5V
16	IF	IF Output	---
MW16 Heatsink Slug	GND	OWP Ground	0V

Attenuator State

Attenuator A "IN" Pin 6 = High, Pin 7 = Low
 "OUT" Pin 6 = Low, Pin 7 = High
 Attenuator B "IN" Pin 9 = Low, Pin 10 = High
 "OUT" Pin 9 = High, Pin 10 = Low

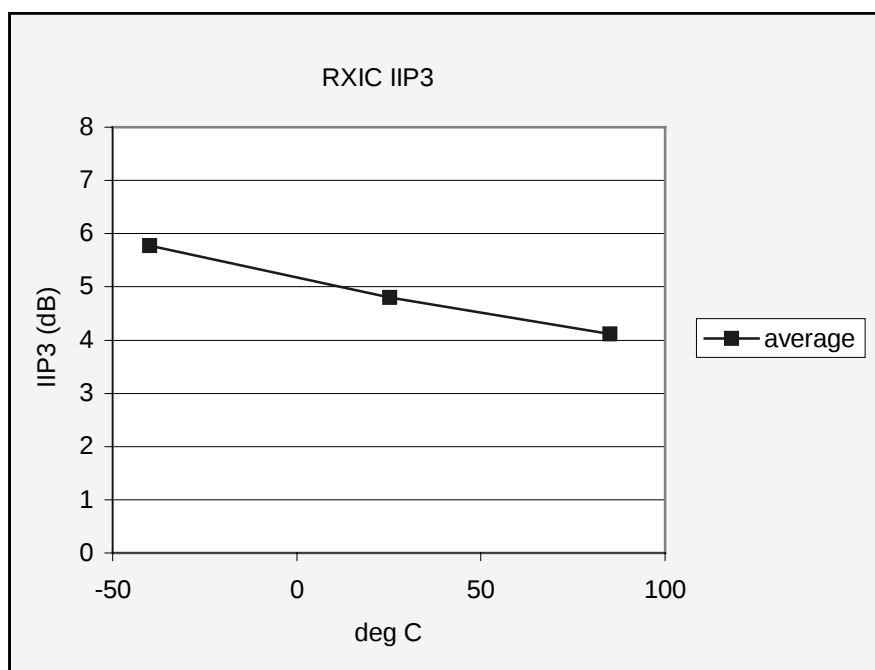
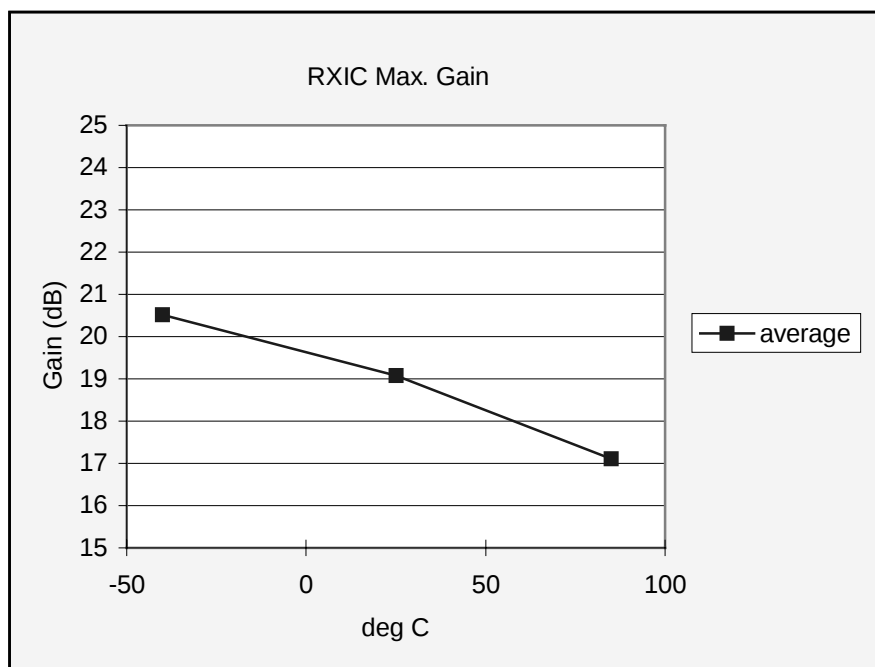
Logic level High: $V_{\text{High}} > V_{\text{D}} - 0.15\text{V}$
 Logic level Low: $V_{\text{Low}} < +0.5\text{V}$

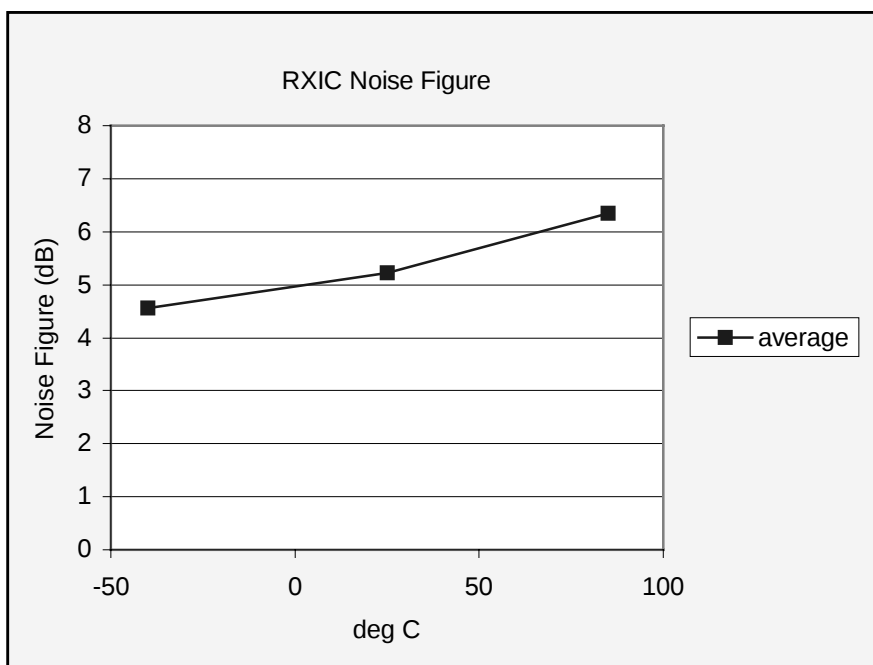
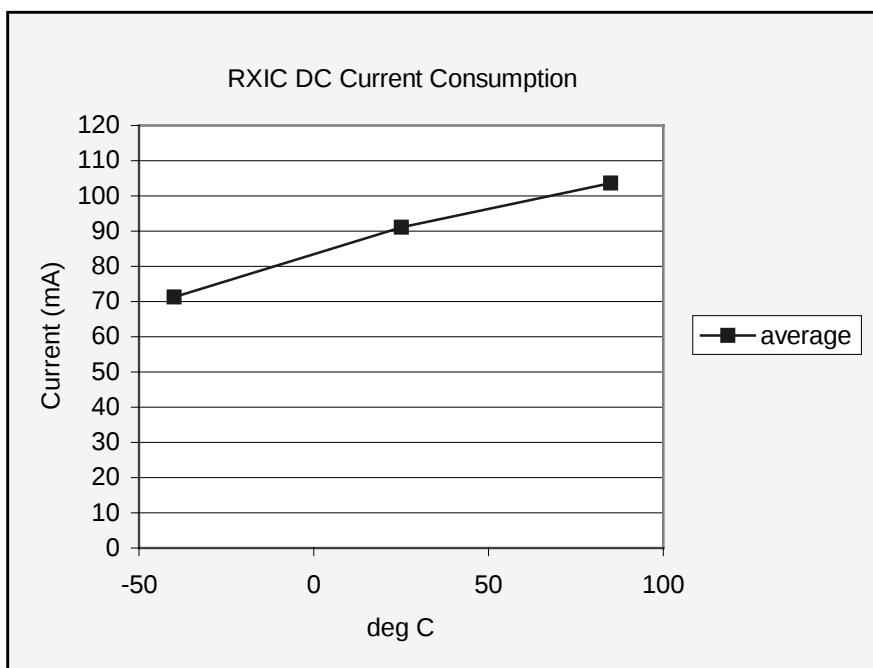
Note: Attenuator "OUT" is defined as maximum gain state.
 Attenuator "IN" is defined as minimum gain state.

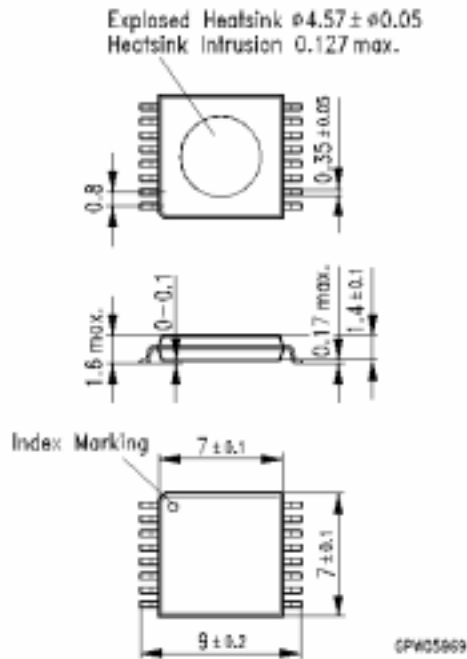
Electrical Characteristics versus Temperature

Test conditions: $V_{\text{DD}} = 5\text{V}$, $V_{\text{GG}} = -5\text{V}$; $f_{\text{RF}} = 3475\text{-}3500\text{ MHz}$; $P_{\text{RF}} = -20\text{ dBm}$;

$f_{LO} = 2359$ MHz; $P_{LO} = 0$ dBm; $f_{IF} = 1116$ -1141MHz, both attenuators “OUT” (for further information about the attenuators see “Attenuator State” on page 5).





Semiconductor Device Outline MW-16


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