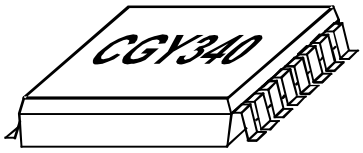
WLL Transmit Upconverter IC for 3.5GHz

- Fully Integrated IF Variable Gain Amplifier, Mixer, LO-Buffer, three RF Amplifier Stages and a switched Attenuator
- High Conversion Gain: typ. 29 dB
- Gain Control Range: >75 dB
- 1dB-Compression Point P_{1dB}: +17,0 dBm
- Output 3rd Order Intercept Point (OIP3) at G_{max}: +28 dBm
- Very low LO-Power demand of typ. -5 to 0 dBm
- Minimum of external components and easy matching
- Total Current Consumption: typ. 270mA @ 5V
- Temperature Range: -40°C to +85°C



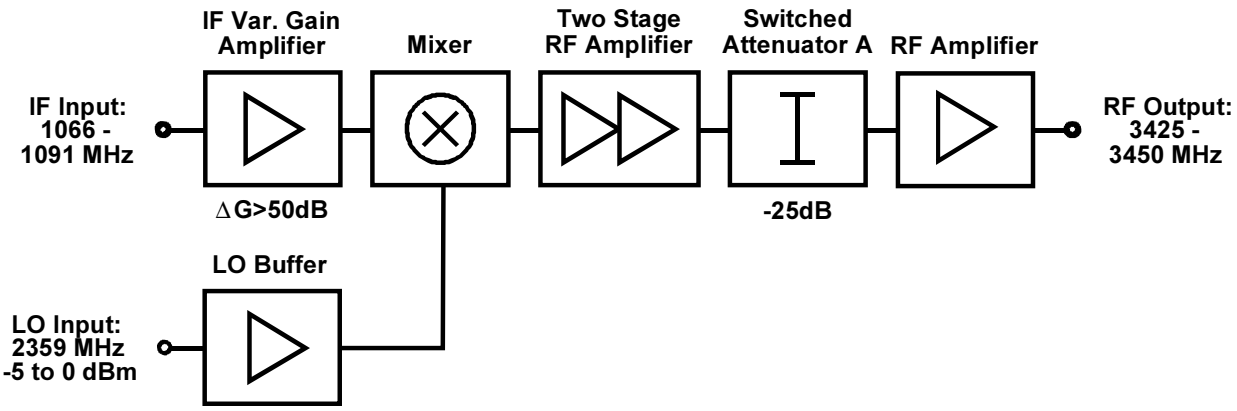
ESD: **E**lectro**s**tatic **d**ischarge sensitive device
Observe handling Precautions!

Type	Marking	Ordering code (tape and reel)	Package
CGY340	**CGY340**	**Q62702G81**	**MW-16**

Maximum Ratings	Port	Symbol	Value		Unit
			min	max	
Positive Supply Voltage	3, 5, 6, 11, 12	V_{DLO}, V_{DRF1}, V_{DRF3}, V_{DRF2}, V_{DVGA}	0	+8	V
Negative Supply Voltage	13	V_G	0	-6	V
IF VGA Control Voltage	14	VGA	-2.0	+8	V
Voltage at Step Attenuator	9, 10	A, A bar	-0.5	+8	V
Power into IF Input	16	IF		10	dBm
Power into LO Input	1	LO		10	dBm
Channel Temperature		T_{Ch}		150	°C
Storage Temperature		T_{stg}	-55	150	°C

Thermal Resistance			
Channel to Soldering Point (GND)	R_{thChS}	T.b.d.	K/W

RF Block Diagram



Electrical Characteristics

Test conditions: T_a = 25°C; V_{DD} = 5V, V_{GG} = -5V; f_{IF} = 1066-1091 MHz; P_{IF} = -20 dBm; f_{LO} = 2359 MHz; P_{LO} = 0 dBm; f_{RF} = 3425-3450 MHz, VGA adjusted to max. gain, attenuator A "OUT" or "IN" (for further information about the VGA and the attenuator see "Attenuator State" on page 5).:

Parameter, Test Conditions	Symbol	min	typ	max	Unit
Operating Drain Current	I_{op}	-	270	-	mA
Operating Drain Current LO Buffer only	I_{LO}	-	10	-	mA
Operating Gate Current	I_g	-	1.3	-	mA

Test conditions: As above, but VGA adjusted to max. gain and attenuator A "OUT" (for further information about the VGA and the attenuator see "Attenuator State" on page 5).

Parameter, Test Conditions	Symbol	min	typ	max	Unit
Conversion Gain	G_c	-	29,0	-	dB
Total Dynamic Range Output Power [1)]	ΔG_{tot}	-	>75	-	dB
VGA Dynamic Range Output Power	ΔG_{VGA}	-	>50	-	dB
SSB Noise Figure	F_{ssb}	-	5,5	-	dB
1dB-Compression Point	P_{1dB}	-	17,0	-	dBm
Output 3rd Order Intercept Point (OIP3) at G_{max}	OIP3	-	+28	-	dBm

Signal Breakthrough at P_{LO} = 0 dBm and P_{RF} = +8.5 dBm:					
LO Leakage at RF-Port	P_{LO}	-	-38	-	dBm
LO Leakage at IF-Port	P_{LO}	-	-31	-	dBm
Spectral Regrowth at G_{max} and P_{out} = +8.5 dBm: [2)]					
Offset: ±256kHz		-	-46	-	dBc
Offset: ±512kHz		-	-66	-	dBc
Offset: ±768kHz		-	>-70	-	dBc
Return Loss:					
IF Port [3)]	S_{11}	-	14	-	dB
RF Port [3)]	S_{22}	-	10	-	dB
LO Port [3)]	S_{11}	-	20	-	dB

Note 1: Variable Gain Amplifier (VGA) and Switched Attenuator A
Note 2: Modulation: π/4 DQPSK (2b/sym). Symbol Rate: 256ksym/s. Mode: PHS. Filter: RNYQ. Filter Alpha: 0.40.
Note 3: Configuration as shown on application board

Test conditions: As above, but VGA adjusted to max. gain and attenuator A “IN” (for further information about the VGA and the attenuator see “Attenuator State” on page 5).

Parameter, Test Conditions	Symbol	min	typ	max	Unit
Conversion Gain	G_c	-	3,0	-	dB

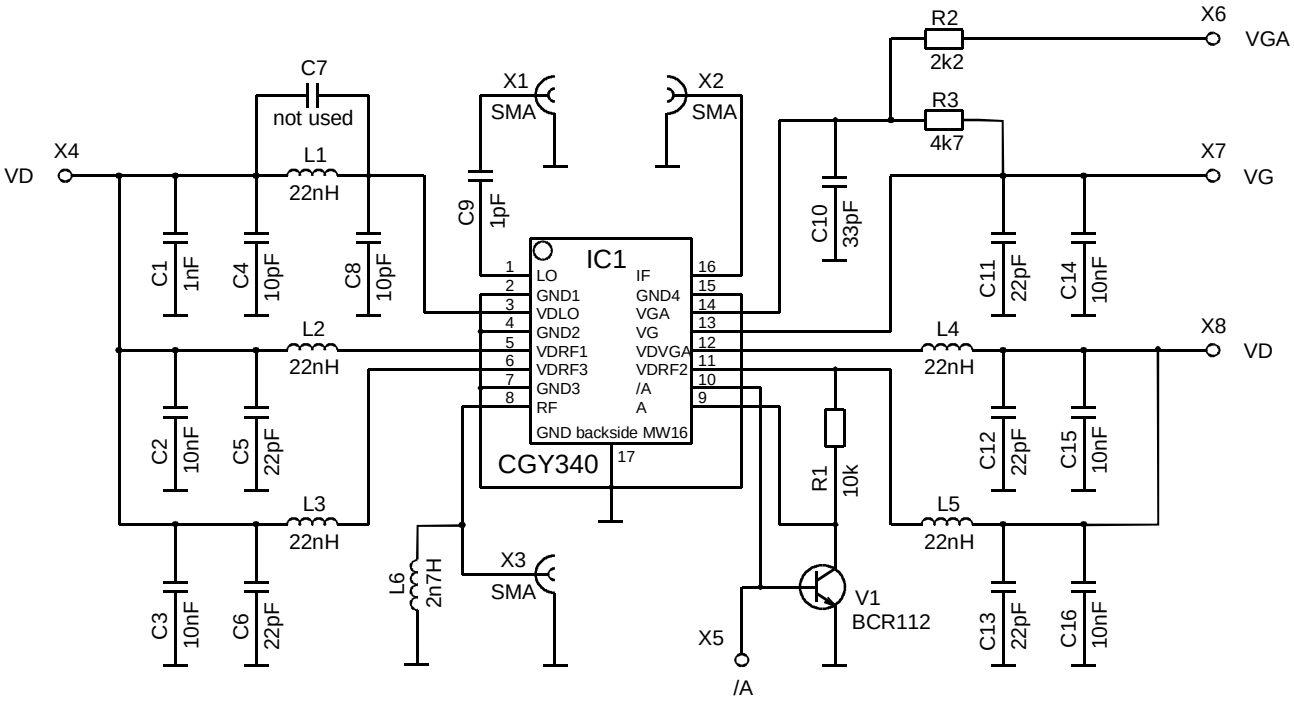
Test conditions: As above, but VGA adjusted to min. gain and attenuator A “OUT” (for further information about the VGA and the attenuator see “Attenuator State” on page 5).

Parameter, Test Conditions	Symbol	min	typ	max	Unit
Conversion Gain	G_c	-	<-29,0	-	dB

Test conditions: As above, but VGA adjusted to min. gain and attenuator A “IN” (for further information about the VGA and the attenuator see “Attenuator State” on page 5).

Parameter, Test Conditions	Symbol	min	typ	max	Unit
Conversion Gain	G_c	-	<-50,0	-	dB

Application Circuit



Notes: Package of all resistors and capacitors: 0603.

All inductors: TOKO LL-1608-FH.

The attenuator A is “OUT” without supplying port A, the gain of the variable gain amplifier is maximum when X6 (VGA) is supplied with +5.0V (for further information about the VGA and the attenuator see “Attenuator State” on page 5).

Pin Definitions and Functions

Pin No.	Symbol	Function	Bias Voltage
1	**LO**	LO Input	---
2	**GND1**	GND	0V
3	**VDLO**	Mixer Drain Bias	+5V
4	**GND2**	GND	0V
5	**VDRF1**	1st RF Amp Drain Bias	+5V
6	**VDRF3**	3rd RF Amp Drain Bias	+5V
7	**GND3**	GND	0V
8	**RF**	RF Output	---
9	**A**	Attenuator Control	+5V, 0V
10	**A bar**	Attenuator Control bar	0V, +5V
11	**VDRF2**	2nd RF Amp Drain Bias	+5V
12	**VDVGA**	IF VGA Drain Bias	+5V
13	**VG**	Negative Supply	-5V
14	**VGA**	IF VGA Control Voltage	-1.6V to +1.8V [1)]
15	**GND4**	GND	0V
16	**IF**	IF Input	---
MW16 Heatsink Slug	**GND**	OWP Ground	0V

Note 1: A voltage of –1.6V to +1.8V on Pin 14 is equal to a voltage of 0V to +5V on pad X6 of the application circuit.

Attenuator State

Attenuator A "IN" Pin 9 = Low, Pin 10 = High
"OUT" Pin 9 = High, Pin 10 = Low

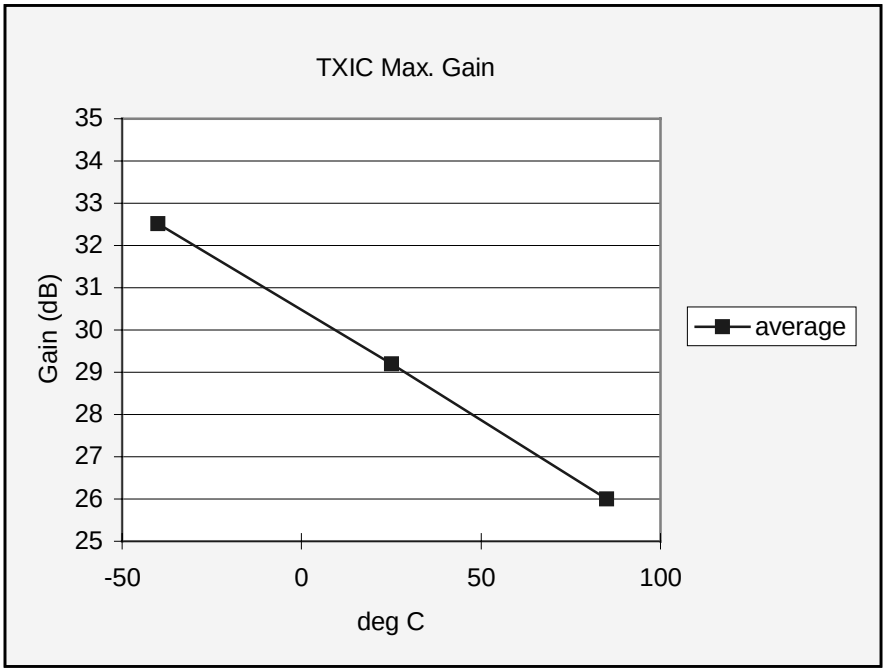
Logic level High: $V_{High} > V_D - 0.15V$
Logic level Low: $V_{Low} < +0.5V$

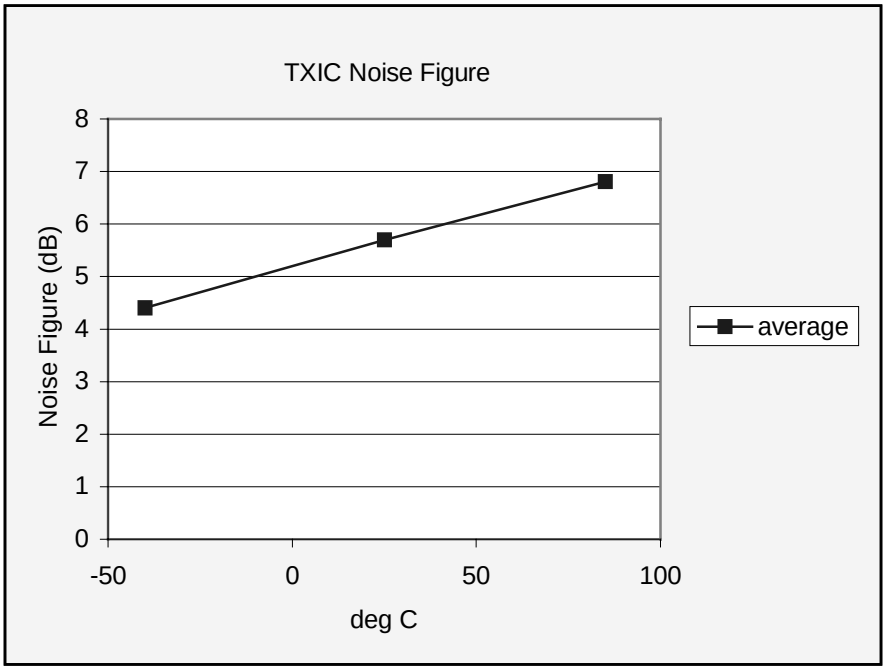
Note: Attenuator "OUT" is defined as maximum gain state.
Attenuator "IN" is defined as minimum gain state.

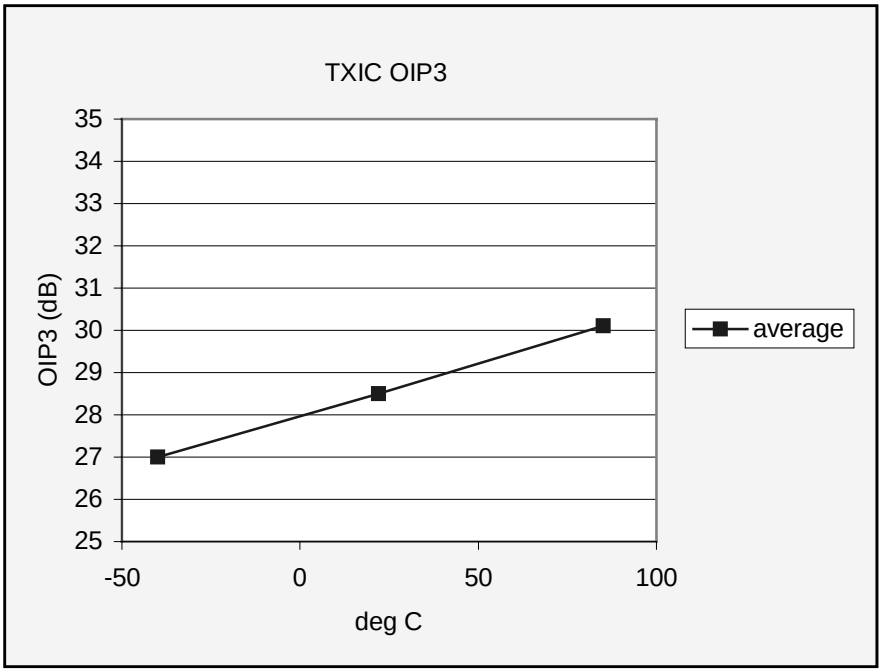
VGA Min. Gain Pin 14 = -1.5V (equal to a voltage of 0V on pad X6 of the application circuit)
Max. Gain Pin 14 = +1.8V (equal to a voltage of 5V on pad X6 of the application circuit)

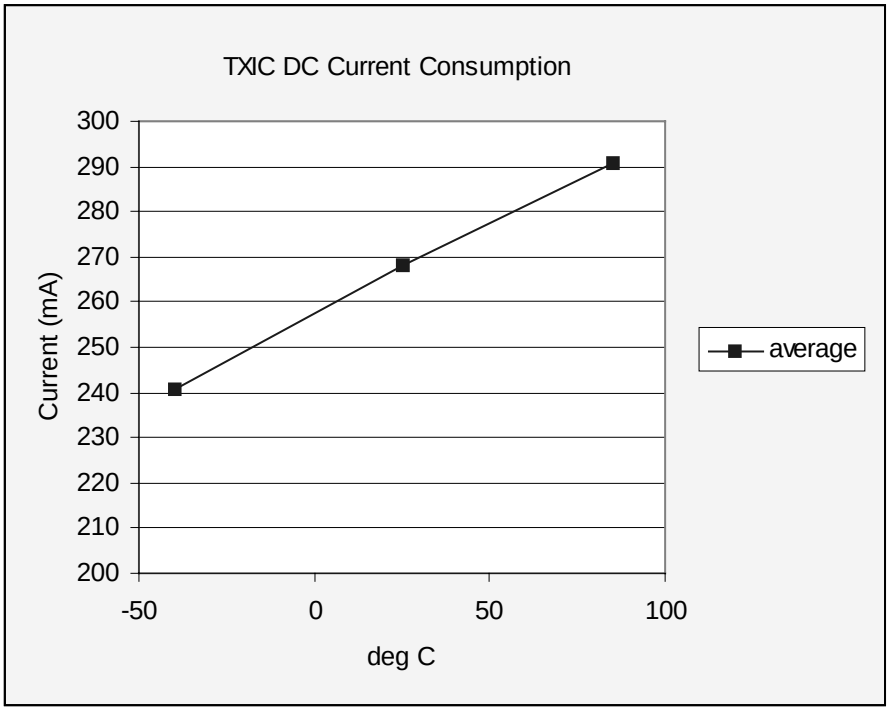
Electrical Characteristics versus Temperature

Test conditions: V_{DD} = 5V, V_{GG} = -5V; f_{IF} = 1066-1091 MHz; P_{IF} = -20 dBm; f_{LO} = 2359 MHz; P_{LO} = 0 dBm; f_{RF} = 3425-3450 MHz, VGA adjusted to max. gain and attenuator A "OUT" (for further information about the VGA and the attenuator see "Attenuator State" on page 5).

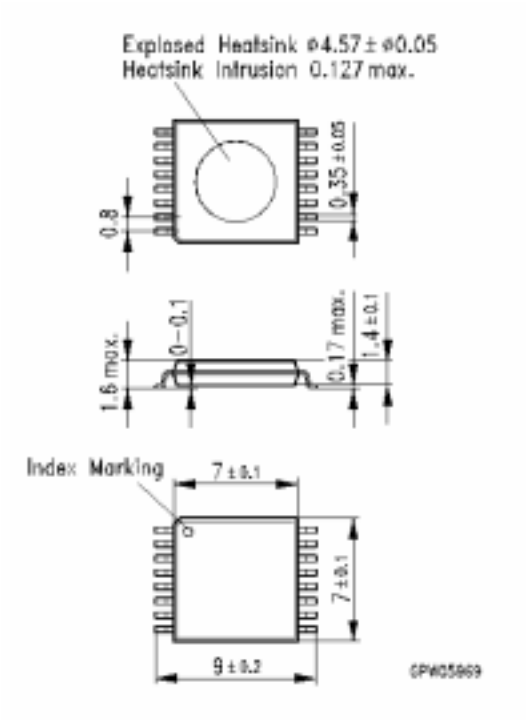








Semiconductor Device Layout MW16



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