Panel interface for telephones BU8317KV

The BU8317KV is a large-scale integrated circuit which enables a serial input / output interface between the key input required for panel boards used in PHS systems, portable telephones, and telephone answering machines and LED and LCD control functions. It reduces the number of wiring harnesses needed between the main board in the telephone and the panel board, and takes some of the processing load off the main CPU.

Applications

PHS systems, portable telephones, telephone answering machines

Features

- 1) 7×7 keypad matrix interface.
- 12-bit LED driver. (6 bits can also function as input pins)
- 4-column 32-segment LCD driver. (internal bias-generating resistor)
- 4) Standby mode.
- 5) VQFP80 package.

● Absolute maximum ratings (unless otherwise noted, Ta = 25°C)

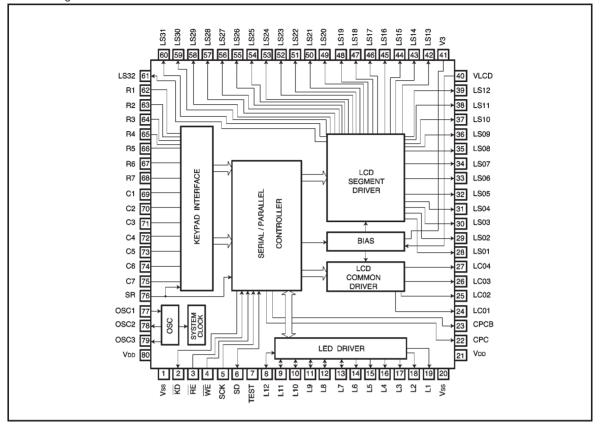
Parameter	Symbol	Limits	Unit	Conditions
Power supply voltage	V _{DD}	7.0	V	Including power supply for LCD drive
Power dissipation	Pd	400	mW	_
Operating temperature	Topr	−25~ +60	°C	_
Storage temperature	Tstg	−55∼ +125	င	_
Input voltage	VIN	Vss-0.3~Vdd+0.3	V	RE, WE, SCK, SD pins
Output voltage 1	Vout1	Vss-0.3~Vpp+0.3	V	SD, L7~L12 pins
Output voltage 2	Vout2	Vss-0.3~7.0	V	L1∼L6, KD pins
Output current 1	Іоит1	20	mA	L1∼L6 pins
Output current 2	Іоит2	15	mA	L7~L12 pins

• Recommended operating conditions (Ta = 25°C)

Parameter		Symbol	Limits	Unit	Conditions
Power supply voltage		V _{DD}	1.8~5.5	V	*
Oscillation frequency		fosc	800	Hz	$R_i=1M\Omega$, $R_x=270k\Omega$ $C_x=2.2nF$
Input voltage	Н	ViH	0.8Vpp~Vpp	V	RE, WE, SCK, SD,
L		VıL	0~0.2V _{DD}	V	L7~L12 pins
Key connection resistar	nce	Rкс	0~5	kΩ	_

^{*} The power supply voltage range listed is for the BU8317KV operated as a stand-alone unit, and operations originating in characteristics of attachments such as LEDs and LCDs are not guaranteed at these values.

Block diagram



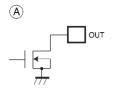
Pin descriptions

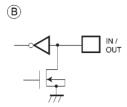
Pin No.	Pin name	Function	Model
19~14	L1~L6	These are the output pins for LED drive. They output a LOW state and cause the LED to light when "1" is applied to the LED register, and they output a Z (high impedance) state when "0" is written, and cause the LED to go off.	A
13~8	L7~L12	These are the LED control output and parallel input pins. They output a LOW state when "1" is applied to the LED register, and they output a Z (high impedance) state when "0" is written. When used as parallel input pins, "0" should be written to the pertinent LED register. The pin state is read as serial data.	B
24~27	LC01~LC04	These are the LCD drive common output pins. They are connected to the common pins on the LCD panel, and when a standby mode, all LEDs valid, or all LEDs invalid command is executed, they output a LOW state and cause the LCD to go out.	©
28~39 42~61	LS01~LS32	These are the LCD drive segment output pins. They are connected to the segment pins on the LCD panel, and when a standby mode, all LEDs valid, or all LEDs invalid command is executed, they output a LOW state and cause the LCD to go out.	©
62~68 69~75	R1~R7 C1~C7	These are the keypad input and output pins. They can be used to configure a keypad of up to 7 \times 7 using single-contact key switches.	(D)
2	KD	This is the output pin for the key press state. When a key is pressed, an on debounce state is valid, and a LOW state is output. After the key has been released, an off debounce state is valid, and these are Z (high impedance).	A

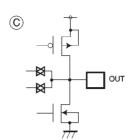
Pin No.	Pin name	Function								
		This is the read enable input pin and serves as the Schmitt trigger input. The read mode (serial output of key data) is accessed								
3	RE	when this is LOW. Key data is set to the output serial RE WE Operation mode	E							
		register at the falling edge. H H Normal operation								
		H L Write mode								
		This is the write enable input pin and serves as the Schmitt trigger								
4	WE	input.The write mode (serial input L L Standby mode	E							
		of data) is accessed when this key is LOW. Serial data is taken up internally at the rising edge.								
5	SCK	his is the shift clock input pin for serial data, and serves as the chmitt trigger input. When RE is LOW, data is read from the SD pin one bit at a ne, at the rising edge of a Schmitt trigger input. When WE is LOW, data is written the SD one bit at a time, at the falling edge of the Schmitt trigger input.								
6	SD	This is the serial data input pin. Data is input and output in the pertinent data format. Data is output when $\overline{RE} = LOW$ and $\overline{WE} = HIGH$. In any state other than data output state, this pin is Z (high impedance).								
76	SR	This is the standby mode cancel input pin. Input is possible when \overline{RE} is LOW and \overline{WE} is LOW, and the standby mode is cancelled when this pin is LOW. Because this pin is pulled up to a resistance, this can be used to configure a standby mode cancel key for V_{SS} by connecting it to a single-contact key switch.	G							
77~79	OSC1~OSC3	These are the I/O pins for the internal oscillator. The recommended values are as follows: R_1 : =1M Ω $_{\rm N}$ R $_{\rm N}$ =270k Ω $_{\rm N}$ C $_{\rm N}$ =2.2nF	()							
22, 23	CPC, CPCB	These are the output pins for the booster circuit drive. A VLCD booster power supply can be configured using an external diode and capacitor.								
21, 80	V _{DD}	This is the V _{DD} pin.								
1, 20	Vss	This is the Vss pin.	_							
40	VLCD	This is the power supply pin for the LCD. Voltages higher than V _{DD} and lower than the absolute maximum rating can be applied to this pin.	J							
41	V3	This is the LCD bias correction pin. When selected, a LOW level reference voltage is output.	J							
7	TEST	This is the test input pin and should not be connected to anything.	G							

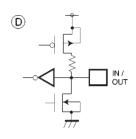


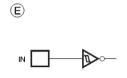
●Input / output circuits

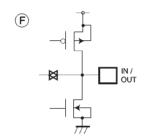


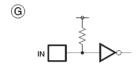


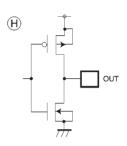


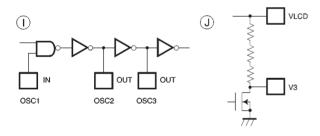












For the corresponding pins, please see "Model" under "Pin descriptions".

●Electrical characteristics (unless otherwise noted, Ta = 25°C, VDD=2.7 to 5.5V)

	Parame	eter	Symbol	Min.	Тур.	Max.	Unit	Cond	itions	Measurement circuit
Supply	current 1		IDD1	_	_	2	μΑ	When oscillation	is stopped	Fig.3
Supply	current 2		I _{DD2}	_	30	50	μΑ	V _{DD} =3.0V		Fig.3
Supply	current 3		I _{DD3}	_	180	300	μΑ	V _{DD} =5.0V		Fig.3
Innuit s	alta a a	Н	lін	_	_	1	μΑ	RE, WE, SCK, S	Duine	Fig.3
Input v	ollage	L	lıL	_	_	1	μΑ	HE, WE, SCK, S	Dpins	Fig.3
		Н	Vон	0.9V _{DD}	_	V _{DD}	٧	SDpin no I	oad	Fig.3
		L1	V _{OL1}	0	_	0.1V _{DD}	٧	SD, KDpin no k	oad	Fig.3
		L2	V _{OL2}	0	_	0.5	٧	L1~L6 pin VDD=5V, loL=15	imA	Fig.3
		L3	Vol3	0	_	0.5	٧	L7~L12 pin V _{DD} =5V, loL=10)mA	Fig.3
Output	voltage	H ⁺	V _H +	0.95V _{DD}	_	V _{DD}	٧	HIGH when selected		Fig.3
		L+	VL+	-0.05V _{DD}	_	-2/3√DD -+0.05√DD	٧	HIGH when not selected	LC01~LC04	Fig.3
		L-	V _L -	-13VDD -0.05VDD	_	13VDD +0.05VDD	٧	LOW when not selected	LS01~LS32 with no load	Fig.3
		H-	V _H -	0.05V _{DD}	_	0	٧	LOW when selected		Fig.3
	Setup tin	ne S	tsus	100	_	_	ns	_	_	Fig.4
Input	Setup tin	ne I	tsuı	100	_	_	ns	_	_	Fig.4
	Hold time	e I	tнı	100	_	_	ns		_	Fig.4
	Setup tin	ne K	tsuk	100	_	_	ns	_		Fig.4
Output	Setup tin	ne R	tsur	100	_	_	ns	_	-	Fig.4
	SD outp	ut delay time	too	100	_	_	ns	_	-	Fig.4
Commo	n Serial	clock cycle	tcyc	500	_	_	ns	DUTY=50%		Fig.4
Key on	debounce	e time	tobn	_	30	_	ms	_	-	Fig.4
Key off	debounce	e time	tobe	_	50	_	ms	-	_	Fig.4

ONot designed for radiation resitance.

Timing charts

Serial data input timing

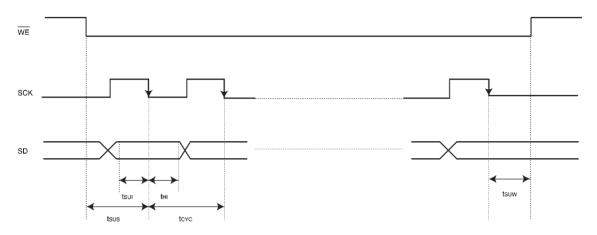


Fig. 1

Serial data output timing

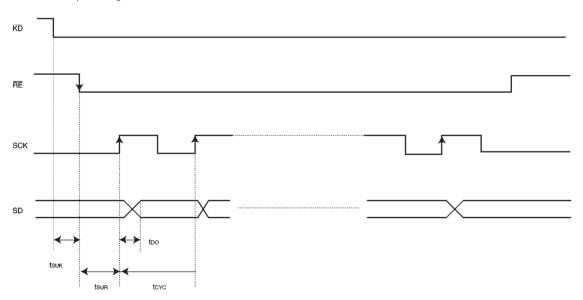


Fig. 2

Communication ICs BU8317KV

Measurement circuits

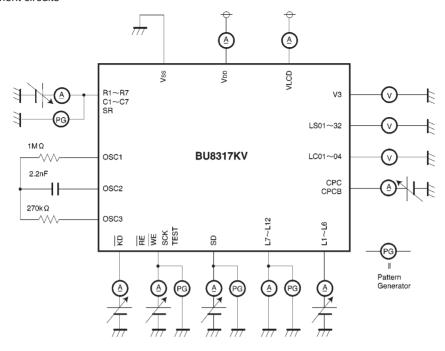


Fig. 3 Measurement circuit for DC items

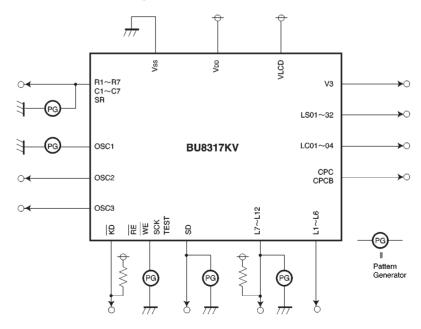
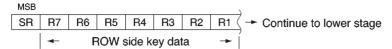


Fig. 4 Measurement circuit for AC items

- •Data formats (Serial data is input and output with the MSB coming first.)
- (1) Reading data



From upper stage → C7 C6 C5 C4 C3 C2 C1 L12 L11 L10 L9 L8 L7

COL side key data → LED pin data →

SR : Outputs SR pin status. Pressing a key (low level) outputs "1" and

releasing the key (high level) outputs "0".

A "0" is output is the key is not pressed on low level.

 $R1\sim R7,\,C1\sim C7$: Outputs key data. Pressing a key outputs "1" and not pressing the

key outputs "0", when on low level.

 $L7\sim L12$: Outputs parallel input data. Output "1" when the pin is on high lev-

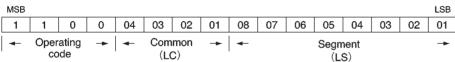
el and "0" when it is on low level.

(2) LED resitor writing command



L1~L12 : Used for LED control. LED lights up with "1" and is unlit with "0".

(3) LCD register writing command



MSB															LSB
1	1	0	1	04	03	02	01	16	15	14	13	12	11	10	09
+		ating de	→	-	Com	~)	→	-			Segm (L:				→

MSB															LSB
1	1	1	0	04	03	02	01	24	23	22	21	20	19	18	17
-		ating	-	-	Com		-	-			Segn	nent			-
	CC	de			(L(C)					(L:	S)			

MSB															LSB
1	1	1	1	04	03	02	01	32	31	30	29	28	27	26	25
-		ating	-	-	Com		-	-			Segn	nent			-
	CC	ode			(L(C)					(L:	S)			

LC01 ~ LC04 : Selects LCD common. "1" means select and "0" means do not se-

lect.

Segment control is active on the selected common, only.

Multiple commons can be selected simultaneously.

LS01 \sim LS32 : Used for LCD segment control. Lights up with "1" and is unlit with

"0".

Communication ICs BU8317KV

(4) All LEDs, LCDs activate command

MSB															LSB
0	0	1	0	0	0	0	0	*	*	*	*	*	*	*	*
-			Opera	ating o	code		-	•			T'NO	CAF	RΕ		-

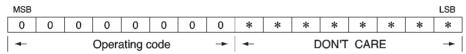
Used to clear non-active status of all LEDs and LCDs.

(5) All LEDs, LCDs non-active command

MSB															LSB
0	1	0	0	0	0	0	0	*	*	*	*	*	*	*	*
•			Opera	ating o	code		-	-		С	T'NO	CAF	RΕ		-

Temporarily turns off all LEDs and LCDs, while holding the LED and LCD register settings as they are. LCD output changes to low level and the bias current channel is cut.

(6) Register reset command



Resets all LED and LCD resisters to "0".

Clears stand-by mode.

Non-active status of all LEDs and LCDs changes to active status.

- Recommended method for inputting / outputting data
- (1) Control command serial input

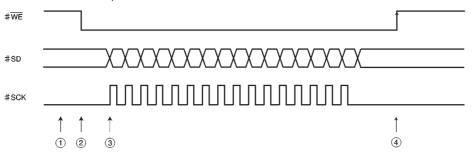


Fig. 5

State	CPU Operation (#)
1	At standby, WE = HIGH, SCK = LOW
2	WE set to LOW (write mode)
3	Serial data is input sequentially to SD at falling edge of SCK
4	After all 16-bit data has been input, $\overline{\text{WE}}$ rising edge is supplied, and data is taken in internally.

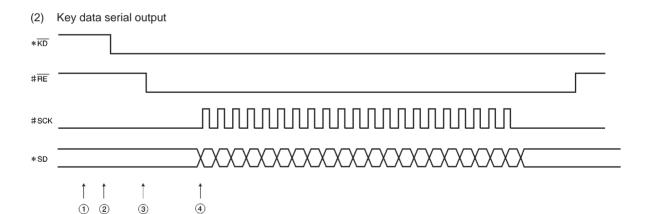


Fig. 6

State	CPU Operation (#)	BU8317KV Series Operation (*)
1	At standby, \overline{RE} = HIGH, SCK = LOW	
2		KD goes LOW when key is pressed.
3	RE set to LOW (read mode)	(Key data setting)
4	Supplied sequentially at rising edge of SCK	Serial data is output from SD in sequential order.

Standby mode

- (1) Setting the standby mode
 - The standby mode is set by setting \overline{RE} to L and \overline{WE} to L.
 - Oscillation stops and the line current falls to an extremely low level.
 - The contents of the LED and LCD registers are reset (all data cleared to 0), and all LEDs and LCDs are turned off.
 - The LCD output goes LOW, and the bias current channel is cut off.
 - The only effective key input is the SR key; no input is accepted from the keypad.

(2) Cancelling the standby mode

- The standby mode is cancelled by executing the register reset command.
- Setting SR to LOW in any state other than RE = LOW and WE = LOW immediately cancels the standby mode.
- Setting SR to LOW when \overline{RE} = LOW and \overline{WE} = LOW initiates oscillation but does not cancel the standby mode. Setting SR to HIGH stops oscillation once again.(If "on debounce" is valid for the SR key and KD has output a LOW level, oscillation continues until an "off debounce" becomes valid.)

Standby mode setting example

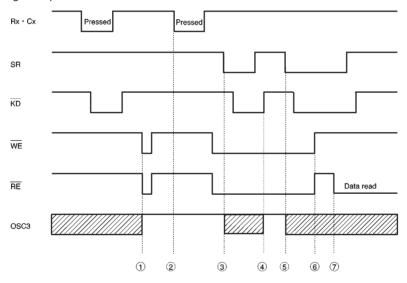


Fig. 7

- 1) At \overline{RE} = LOW, \overline{WE} = LOW, the standby mode is set, and oscillation stops.
- (2) In standby mode, no input is accepted.
- ③ Setting the SR pin to LOW initiates oscillation even in the standby mode. (SR = LOW takes priority over \overline{RE} = LOW, \overline{WE} = LOW.)
- (4) When the SR pin is open (HIGH), \overline{RE} = LOW and \overline{WE} = LOW, so oscillation stops and the standby mode continues to be effective.
- (5) Setting the SR pin LOW initiates oscillation even in the standby mode.
- ⑥ When RE = LOW, WE = LOW is no longer true, the standby mode is cancelled, and oscillation continues even if the SR pin is open (HIGH).
- Data is set in the output serial register at the falling edge of RE and when SR = LOW, and can be read.



Oscillation frequencies

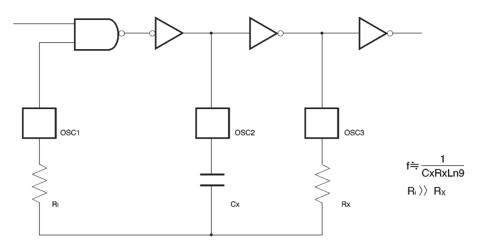


Fig. 8

■LCD drive wave forms

This is a time-shared drive system in which 1 / 3 bias and 1 / 4 duty alternate between two frames.

The figure at the right shows the drive wave forms for the following conditions :

LC01-LSxx: Lighted LC02-LSxx: Not lighted LC03-LSxx: Lighted LC04-LSxx: Not lighted

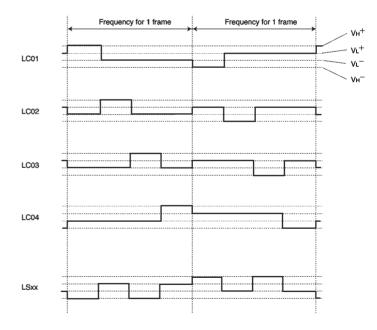


Fig. 9

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Configuring a booster circuit

This shows an example of booster circuit configuration for a VLCD pin, using the CPC and CPCB pins.

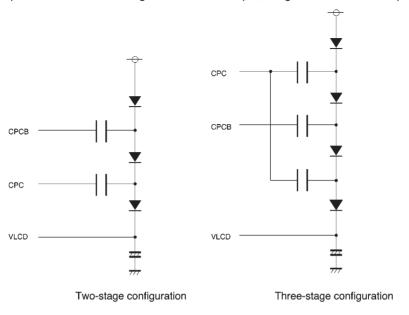


Fig.10

Configuring an LCD bias correction circuit

This shows an example of correction circuit configuration for the LCD output voltage, using the V3 pin.

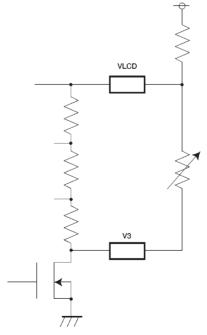


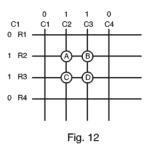
Fig. 11

Precautions when turning on the power supply

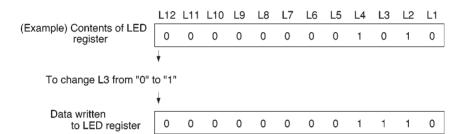
The power supply should be turned on when $\overline{RE} = LOW$ and $\overline{WE} = LOW$, and the registers should then be reset using the register reset command.

- Precautions concerning data input and output
- Serial output of key data when several keys are pressed at the same time is as shown at the right.

The key data when 1. and (1) are pressed at the same time is the same as the key data when 2. and 3. are pressed at the same time.



(2) If the LED and LCD registers are rewritten, all of the bits should be written, and not just the pertinent bits.



Electrical characteristic curve

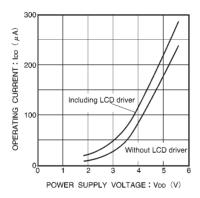


Fig. 13 Operating current vs. power supply voltage characteristic

External dimensions (Units: mm)

