

CMOS logic IC

BU4000B

The BU4000B Series are CMOS ICs featuring low voltage and low power consumption. The wide range of operating power supply voltages is compatible with the general-purpose 4000B Series, and when a 5V power supply voltage is used, the LS-TTL IC can be driven directly.

These ICs are available in SOP and SSOP packages as well as the standard DIP package.

●Features

- 1) Low power dissipation.
- 2) Wide range of operating power supply voltages.
- 3) High input impedance.
- 4) High fan-out.
- 5) Direct drive of 2 L-TTL inputs and 1 LS-TTL input.

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	$-0.3 \sim +18^{*1}$	V
Input voltage	V_{IN}	$-0.3 \sim V_{DD} + 0.3^{*2}$	V
Power dissipation ^{*3}	P_d	Please refer to specifications for individual package	mW
Storage temperature	T_{stg}	$-55 \sim +150$	°C

*1 For the BU4XXXBC type, $V_{DD} = -0.5 \sim +20V$.

*2 For the BU4XXXBC type, $-0.5 \sim V_{DD} + 0.5$.

*3 The values for the SOP and SSOP packages are the values when mounted on a glass epoxy PCB (50mm × 50mm × 1.6mm).

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	$3 \sim 16^{*}$	V
Input voltage	V_{IN}	$0 \sim V_{DD}$	V
Operating temperature	T_{opr}	$-40 \sim +85$	°C

* For the BU4XXXBC type, $V_{DD} = 3$ to 18V.

●Electrical characteristic curves

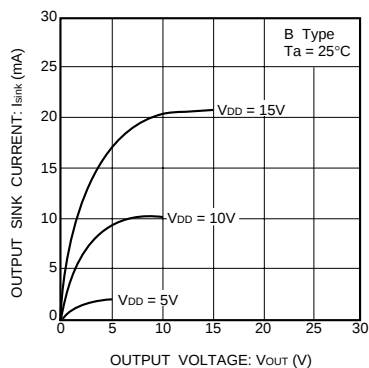


Fig.1 Output sink current vs. output voltage

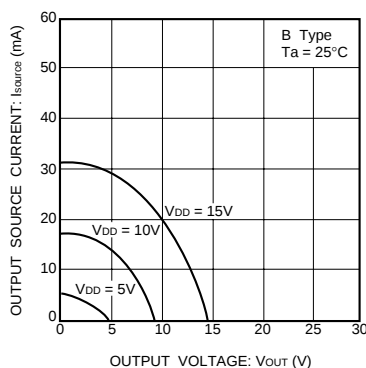


Fig.2 Output source current vs. output voltage

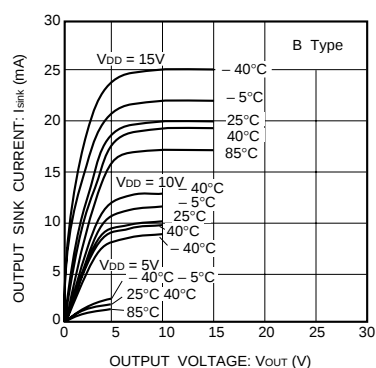


Fig.3 Output SINK current vs. output voltage

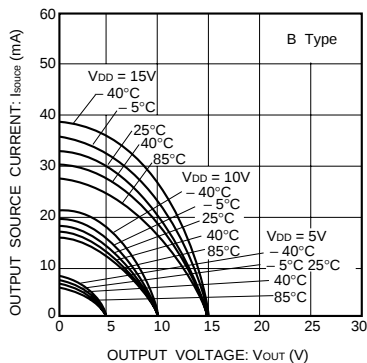


Fig.4 Output source current vs. output voltage

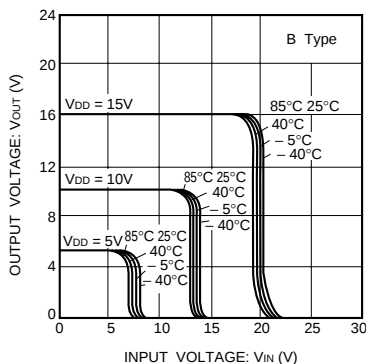


Fig.5 Output voltage vs. input voltage

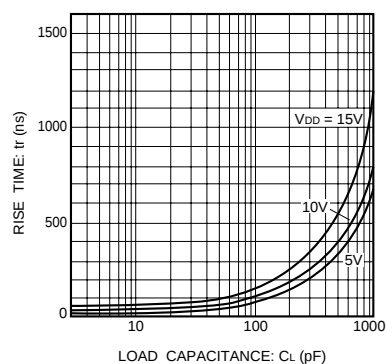


Fig.6 Rise time vs. load capacitance

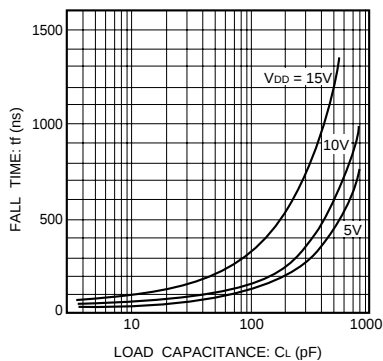


Fig.7 Fall time vs. load capacitance

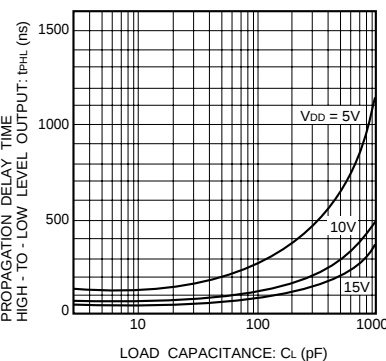


Fig.8 "H" to "L" propagation delay time vs. load capacitance

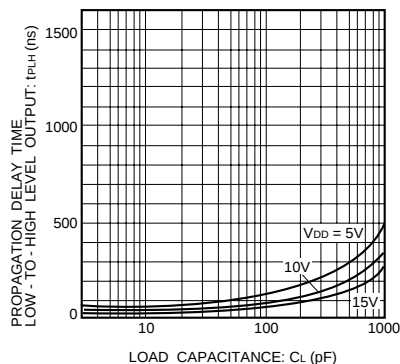


Fig.9 "L" to "H" propagation delay time vs. load capacitance

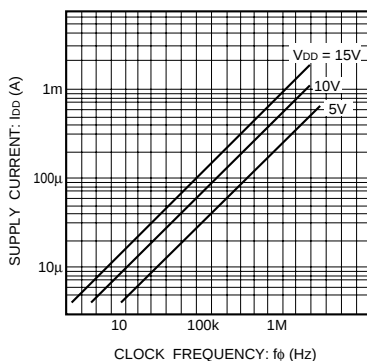


Fig.10 Supply current vs. clock frequency

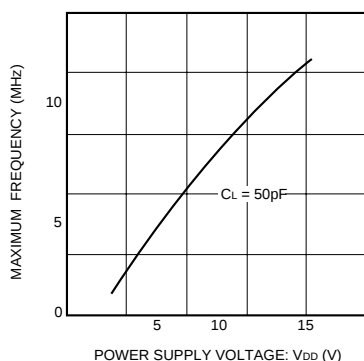


Fig.11 Maximum clock frequency vs. power supply voltage