SIEMENS

Power Semiconductors

TRILITHIC

High Current Motor Driver

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Contents

1 TrilithIC

1.1 New Components for DC Motor Control are Capturing the Market

With the onward march of electronics in the automotive sector and virtually every part of everyday life, power integrated circuits (PICs) are acquiring ever greater importance for system optimization. New semiconductor technologies are providing replacements for an increasing number of electromechanical components such as switches or relays, and the trend towards higher current values has prompted the development of new driver devices.

*) **Tri|lith** [*gr.;* "Stone Triangle"] Prehistoric Stone Monument (Bronze Age and Early Stone Age)

A group of these devices is employed in reversible DC motor drives. For this application, the supply voltage must be able to be applied to the motor in both directions.

As shown in **Figure 1,** this requires 4 switches, one switch to ground and one to the supply voltage, for each motor terminal. Clamping diodes are connected in parallel with the switching transistors for commutation of inductive loads and above all for active motor braking. This arrangement is known as an H-bridge by virtue of its topology, one branch of this circuit being known as a half-bridge.

As the result of innovative technologies, H-bridges are becoming ever more prevalent in high-current applications and are increasingly replacing relays on PCBs.

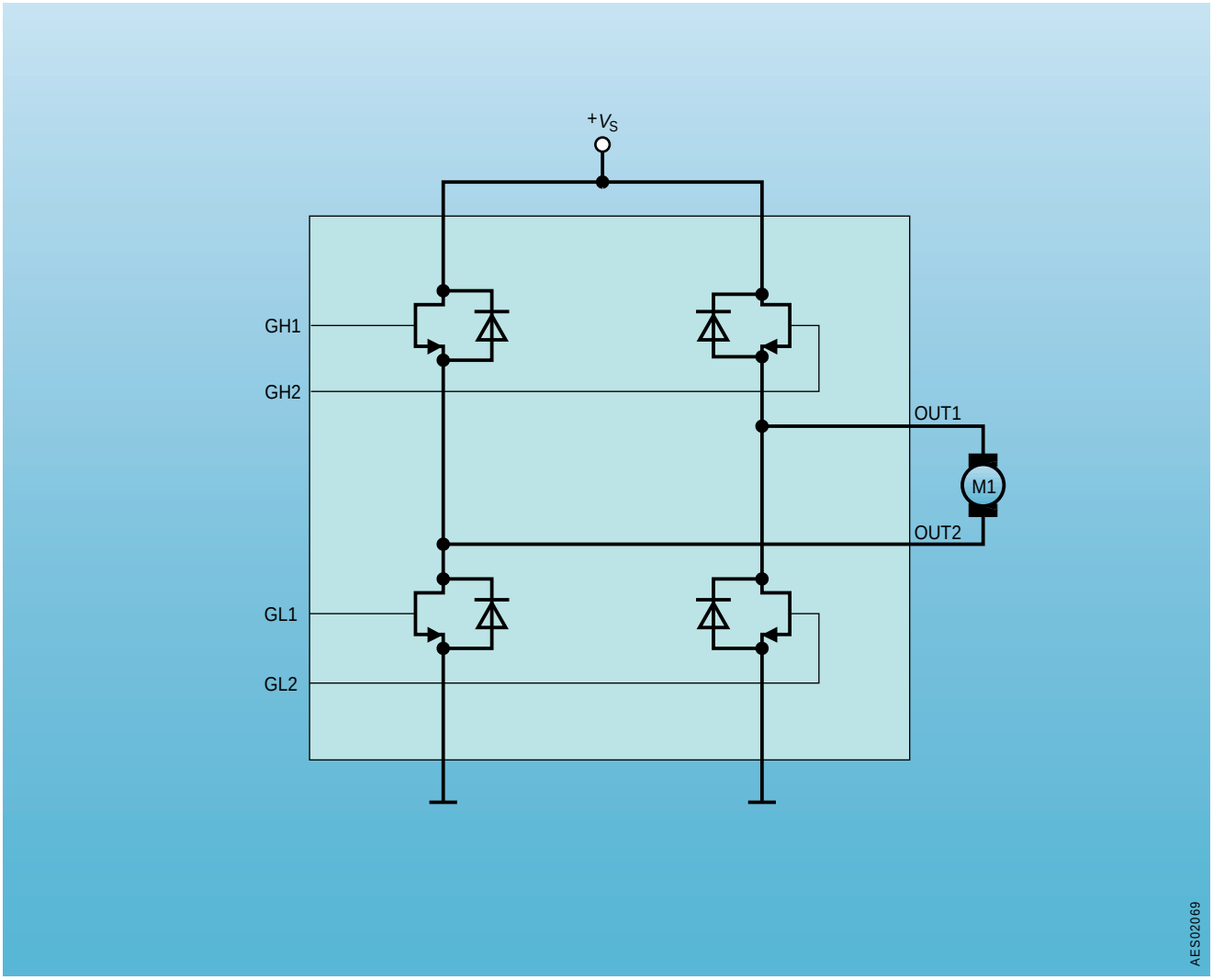

Figure 1
Principle of an H-Bridge Circuit

1.2 Requirements Placed on H-Bridges

The ideal bridge contains 4 switches and 4 clamping diodes without internal resistance which can be actuated with no power and without turn-on delays.

In practical applications the following parameters are therefore of critical importance:

1. The ON-state resistance of the switches; generally bipolar or power-MOS transistors.
2. The peak current rating of the switches must be as high as possible, as DC motors are effectively large capacitive loads because of their inertia.
3. The quiescent current of the device must be as low as possible.

A bridge must also have “diagnostic” capability, i.e. a status output (flag) signals to the drive system (microcontroller) the status of the motor drive. In addition, it is desirable for the outputs to be provided with short-circuit and overtemperature protection. Individual switches that can be configured as required (i.e. able to be used as a bridge, half-bridge or individual high-side or low-side switch and, of course, connectable in parallel) are expanding the possible applications of the device. Increasingly large-scale production is bringing down costs.

These parameters result in reduced power dissipation, lower assembly costs and hence lower system costs.

Particular attention has been paid to reducing the power dissipation, because low on-state resistance values are essential for using semiconductors in small, inexpensive standard packages (for PICs this means preferably SMD plastic packages such as the P-DSO-28). This reduces system costs in several respects, and assembly costs are considerably lower, as no heatsinks or even screw or clamp connections are required. Less space is taken up on the PCB and a lower profile is achieved. In addition, SMDs can be mounted on both sides.

Thanks to the latest generation of semiconductors, loss of electrical energy as heat is virtually eliminated on the PCB. Consequently, the package containing the electronics can be of small and light design. Moreover, as the power required for the drives can be supplied almost without energy loss, the entire power budget is more favorable. As a direct consequence of this, the DC generator of a vehicle can in turn be made smaller, lighter and therefore produced more cheaply.

This weight saving will help significantly in lowering the fuel consumption of modern automobiles. All these considerations have prompted SIEMENS Semiconductors to come up with the slogan:

“Silicon instead of heatsink”

and have led to the development of the

TrilithIC Family.

The first representatives are the **BTS 770** and the **BTS 771**.

2 Technical Specifications

2.1 Choice of Technologies; Lateral or Vertical?

To implement an H-bridge with minimal switch ON-state resistances, it is necessary to compare the technologies employing lateral and vertical power-MOS structures.

Figure 2 shows a lateral power-MOS structure in cross-section. The current flows here from the drain lead of the package via the bond wire to the drain of the MOS structure, through the n-channel to the source and via the second bond wire to the package's source contact.

Disadvantages:

- Large lateral spread of the power MOS structure
- Current flow via two relatively high-resistance bond contacts

Advantages:

- Both power connections can be brought out in isolated form (monolithic integration of an H-bridge possible)
- Only one cooling surface at ground potential required
- Typical representatives of these PICs are the **TLE 5205G** or **TLE 5206G** (see chip photo in **Figure 3**).

These contain an H-bridge with a branch resistance of max. 1200 mΩ for currents up to 5 A with short-circuit protection and diagnostic circuitry. The technology required for producing this device enables bipolar, C-MOS and D-MOS structures to be implemented on the same chip. It is known as: **SIEMENS Power Technology**, or SPT for short.

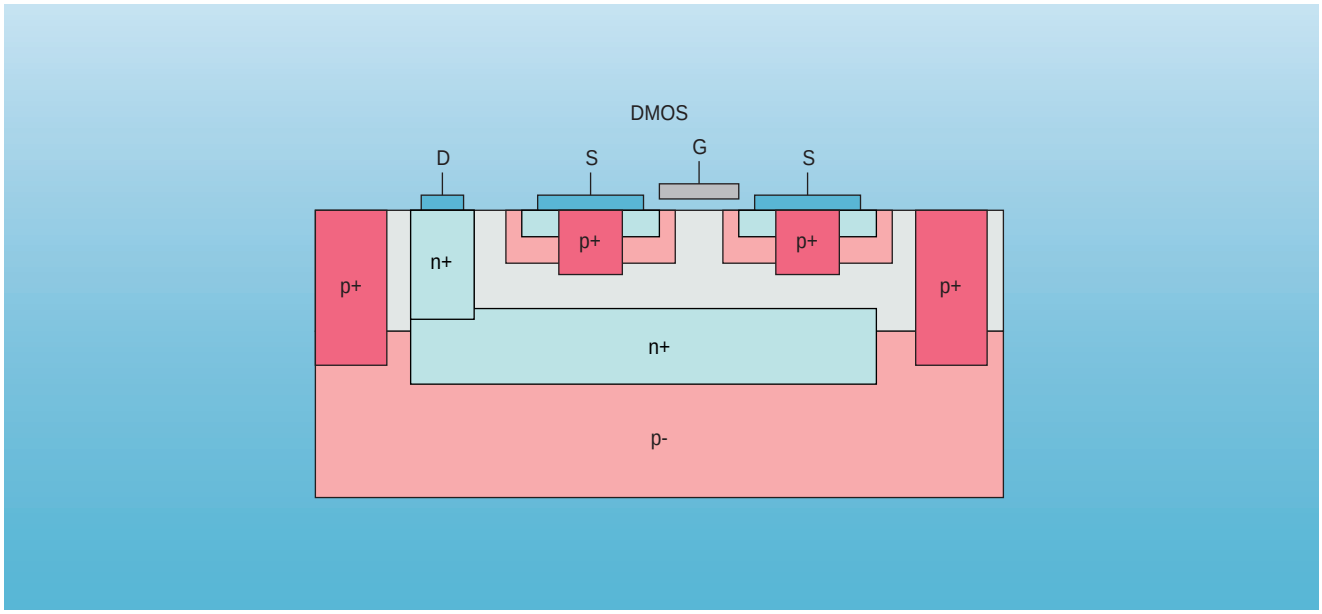

Figure 2
Lateral Power MOS Structure

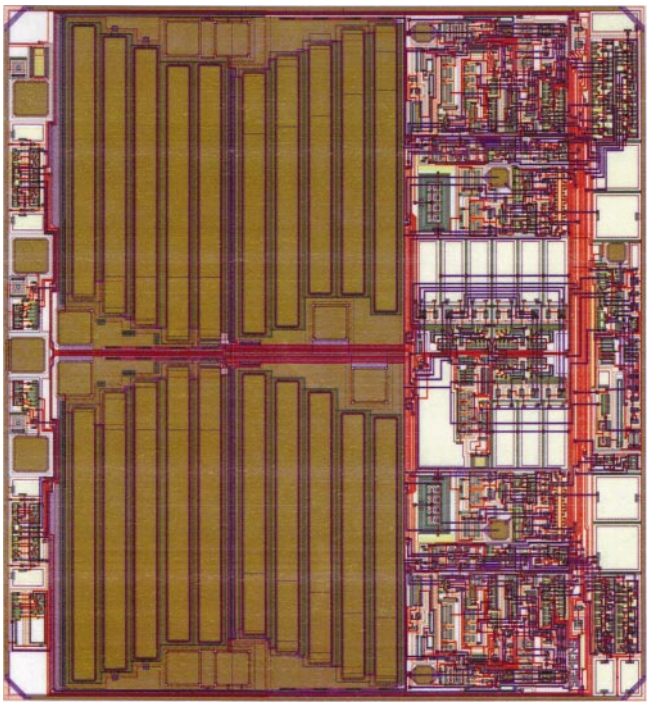

Figure 3
Chip Photo of the TLE 5205

The basic design for a **vertical** technology is shown in **Figure 4**. Here the current flows from the drain contact, which in this case is always on the backside of the chip, i.e. from the heatsink through the chip to the source contact (i.e. vertically).

From there it flows via a single bond wire to the package source lead. The ON-state resistance is therefore much lower than with the lateral structure.

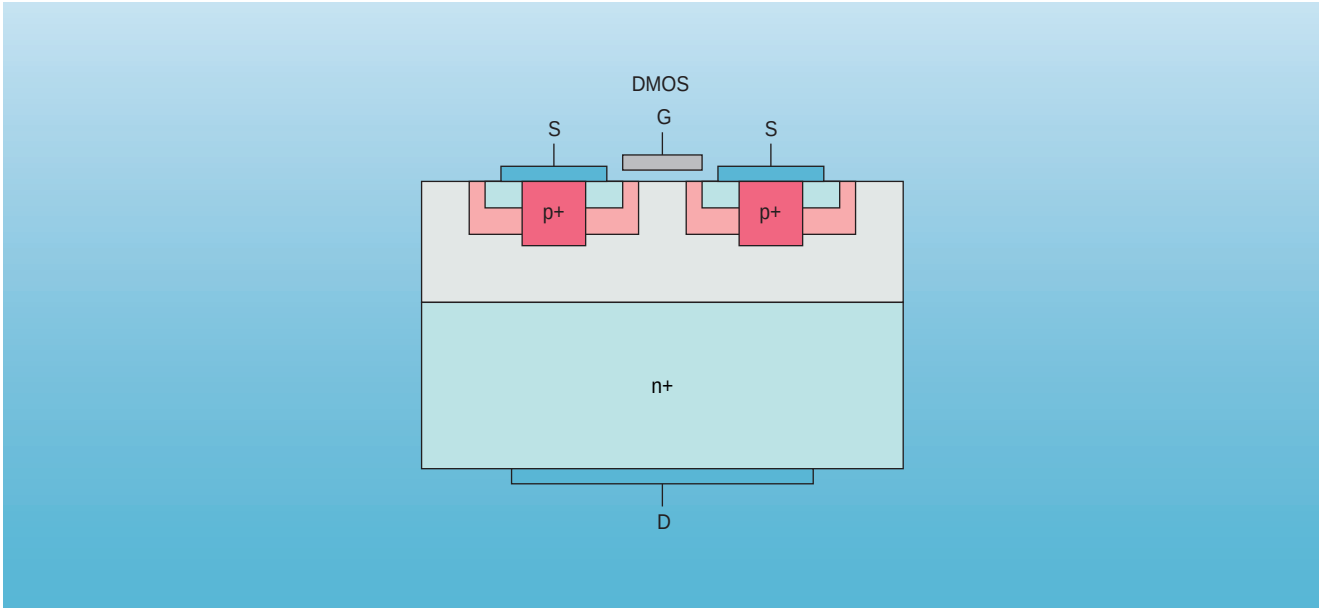

Figure 4
Vertical Power-MOS Structure

The **BTS 611L1** as a typical representative of this technology is shown in the chip photo in **Figure 5**.

This chip contains two high-side switches (HSS for short) whose source contacts have been brought out. The drain leads are permanently connected to the chip backside (heatsink).

These components can be fabricated in **SIEMENS Milli-Smart** Technology with complete on-chip drive and diagnostic circuitry, or alternatively in **Milli-FET** Technology as a power-MOS transistor with minimal ON-state resistance.

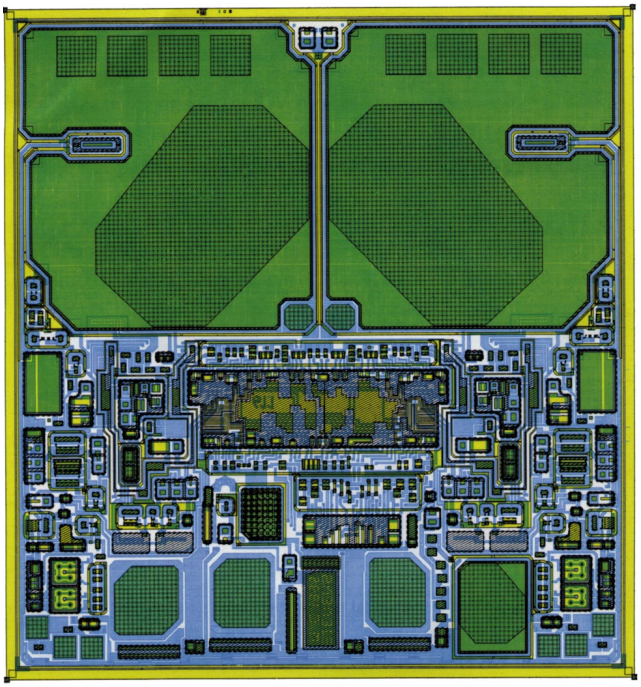

Figure 5
Chip Photo of the BTS 611L1

2.2 The Trilith

If we compare the ON-state resistances per unit area, the picture is as follows:

An H-bridge circuit comprising vertical chips can be fabricated with considerably lower ON-state resistance than using lateral structures with the same chip surface area.

It is not implemented as a monolithic, however, but as a **TrilithIC**.

The device consists of a chip for the two high-side switches with the drain lead connected to the supply voltage, and two other chips for the low-side switches (LSS). As the drain contacts form the chip backside in each case, it is possible to employ a package with three electrically isolated leadframes. This produces a “Trilithic IC” or **TrilithIC** for short, as shown in **Figure 6**.

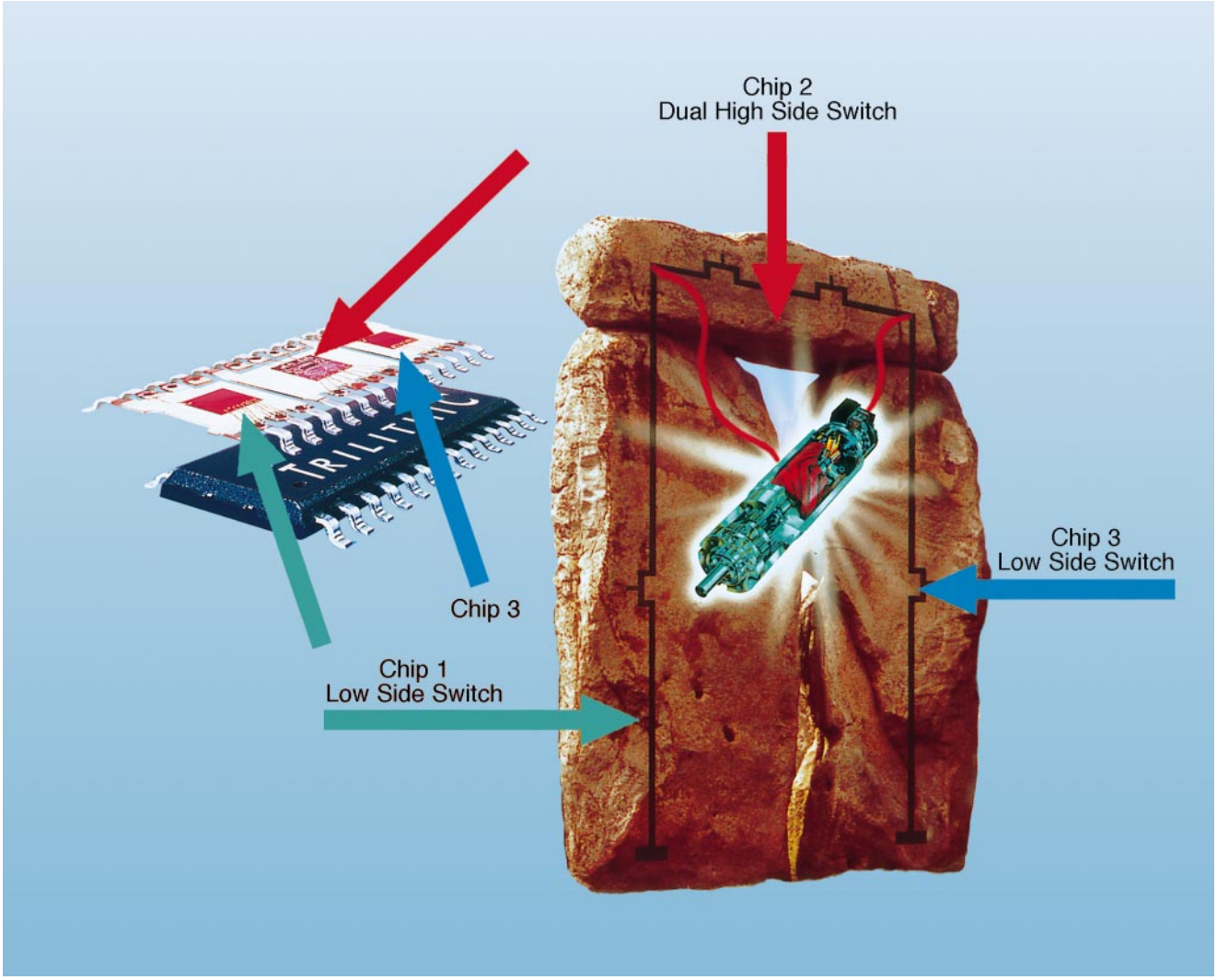

Figure 6
Principle of the TrilithIC

2.3 The Package

The optimum package for meeting these requirements is the P-DSO-28 whose internal layout is shown schematically in **Figure 7**. The two high-side switches are in the center, with the two low-side switches above and below. The power bond contacts required for the four source leads are implemented using multiple bondings of 50 µm diameter gold wire.

For the high-side switches, a total of four 50 µm diameter wires are bonded to two leads, and for the low-side switches a total of 8 wires of the same diameter are likewise bonded to two leads. The reason for this multiple bonding is to keep the bond wire resistance as low as possible (max. 10 mΩ and max. 5 mΩ respectively) and to ensure a high degree of reliability in the high-current region. **Figure 8** shows the bonding arrangement for a selectively opened **BTS 770**.

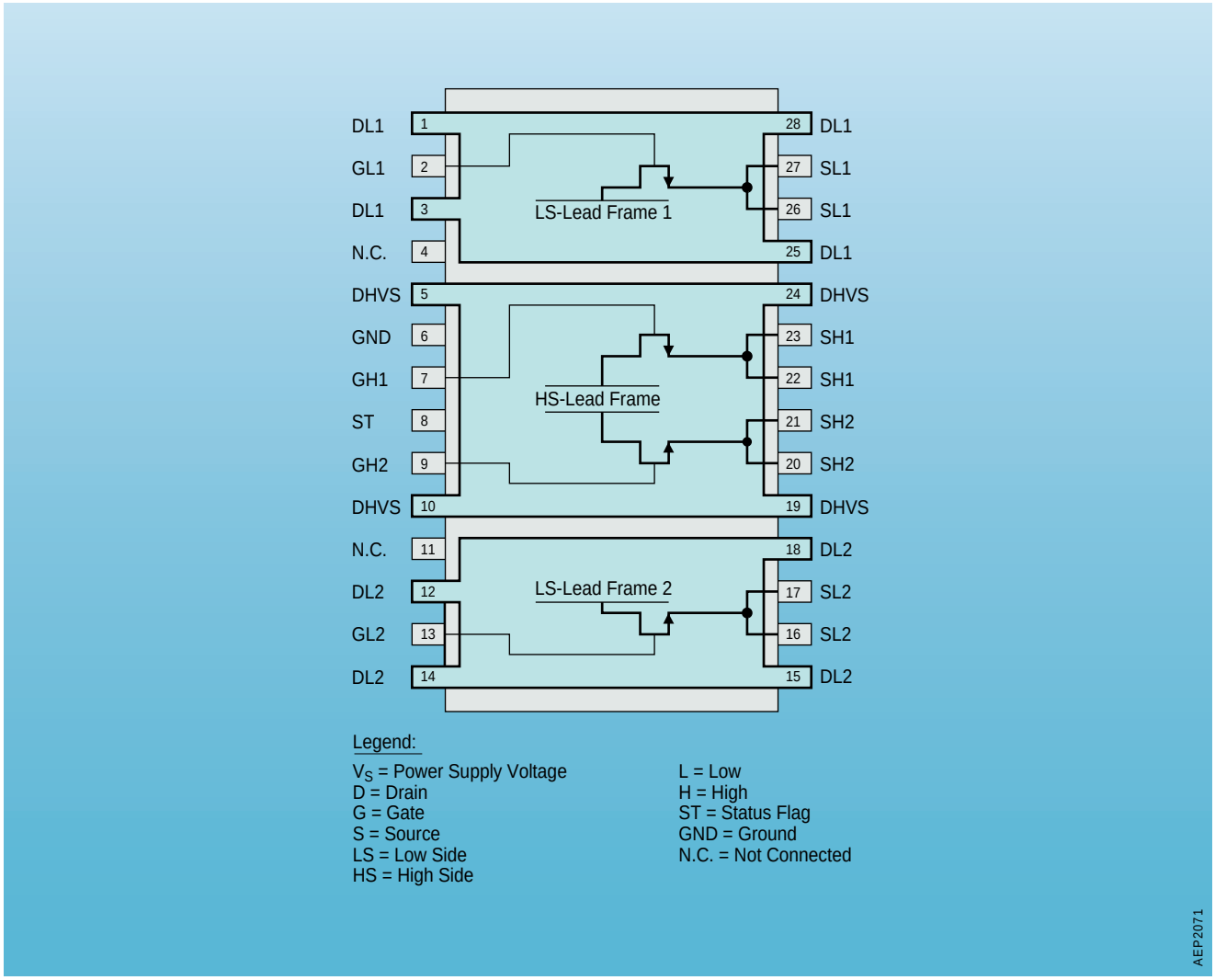

Figure 7
Pin Assignment and Internal Layout of a TrilithIC

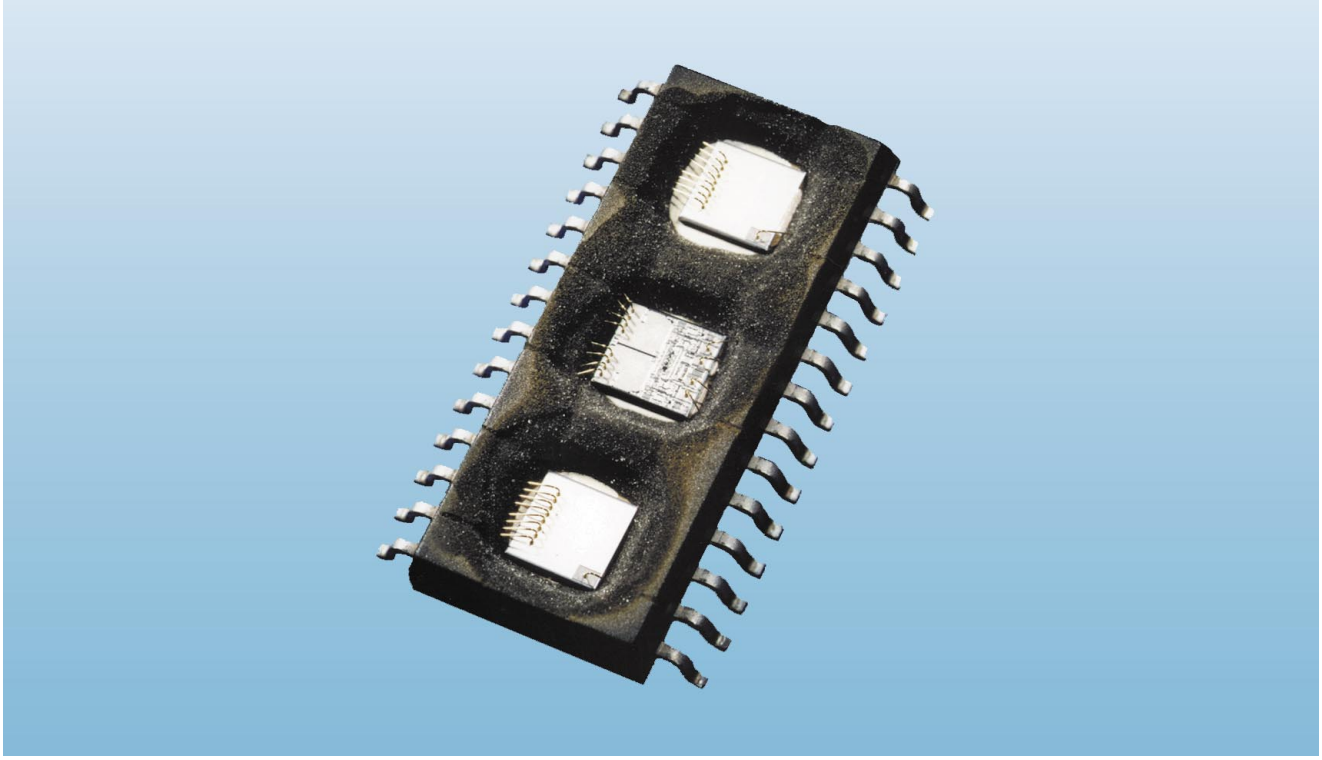

Figure 8
Selectively Opened TrilithIC BTS 770

2.4 Design of the TrilithIC

The exacting requirements placed on the bridge circuit, such as overload and ground short protection, diagnostics capability, inputs with TTL-C-MOS compatibility, overtemperature protection, etc. make it necessary to implement at least the high-side switches in **Milli-Smart** Technology, as the charge pump and diagnostic circuit require a higher degree of manufacturing complexity (see chip photo of the **BTS 611L1**; in this case approx. 50% of the surface area is taken up with these functions). **Milli-FET** Technology optimized for minimum ON-state resistance is employed for the low-side switches. This requires only about half as many mask steps for chip production as Smart SIPMOS Technology.

Consequently, the high-current low-side switch always has much lower resistance yet is less expensive than the associated high-side switches in the bridge arm. In the event of overload and short-circuits to ground, the intelligent high-side switch protects the entire bridge by virtue of its relatively higher ON-state resistance and protection circuitry.

A short circuit to the supply voltage (as a solder splash during PCB production, etc.) is detected by the high-side switch even in the passive state and notified to the drive circuit via the status flag. It is therefore possible to ensure by means of software that the low-side switches are never switched on in response to a short circuit to the supply voltage. For short circuits occurring during operation there is even a solution using simple external circuitry. Further details are given below.

In order to achieve the protection functions already mentioned, an ON-state resistance ratio (HS/LS) of about approximately 2 or more is desirable. The following combinations of standard products has been selected for this purpose:

For the **BTS 770**: **BTS 611L1** and 2× **BUZ 103AL**

For the **BTS 771**: **BTS 621L1** and 2× **BUZ 101AL**

This results in the block diagram shown in **Figure 9**. The associated pin assignment is as given earlier in **Figure 7**. It applies equally to the BTS 770 and BTS 771. The three leadframes are indicated schematically.

Each leadframe is connected to the leads of the standard package via four metal straps.

- For low-side switch 1 this would be pins 1, 3, 25 and 28,
- for low-side switch 2, pins 12, 14, 15 and 18
- and for the two high-side switches, pins 5, 10, 19 and 24.

In bridge mode (one high-side and one low-side switch active) there is a favorable power distribution over two leadframes and therefore a relatively low thermal impedance.

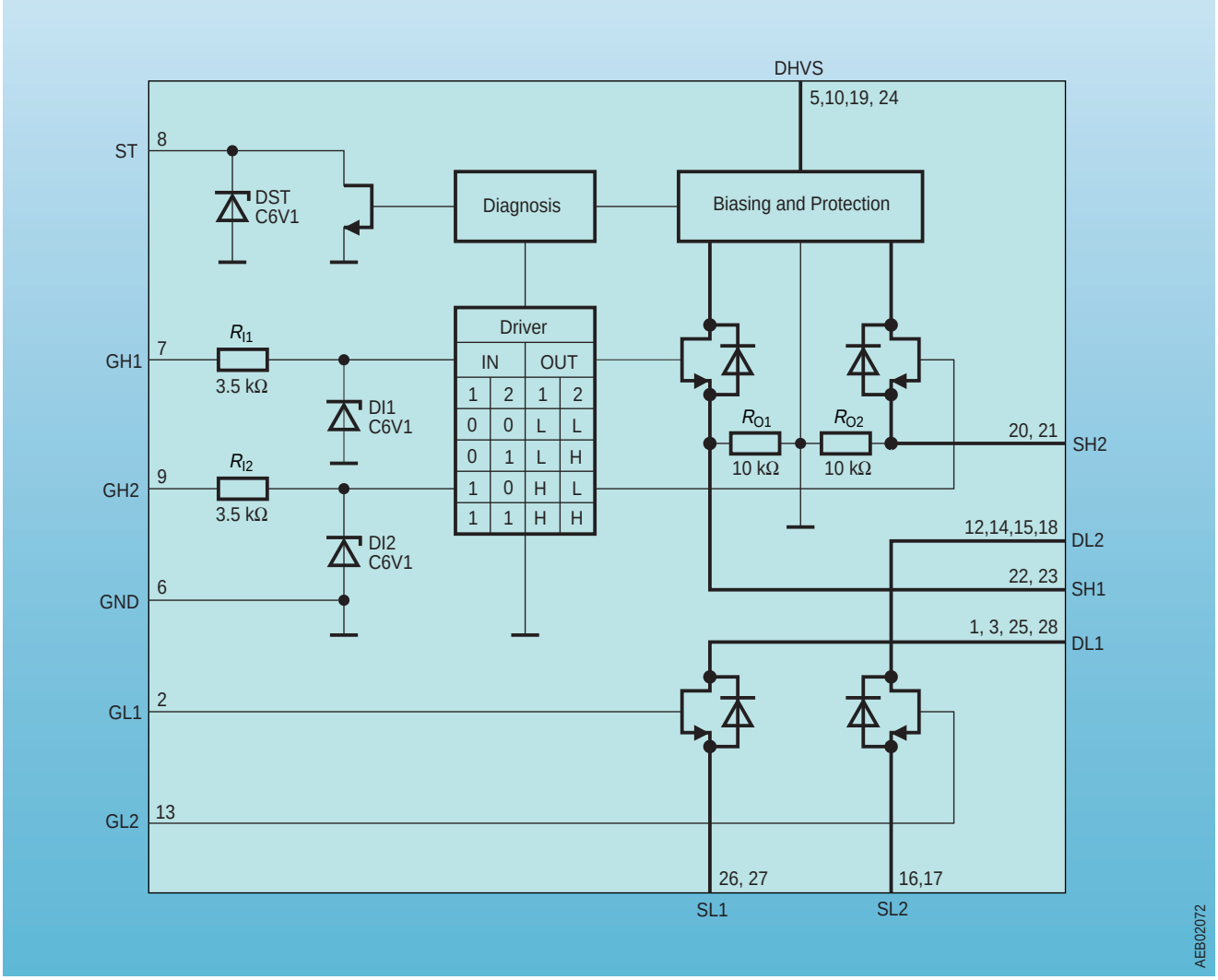

Figure 9
Block Diagram of TrilithIC BTS 770 and BTS 771

2.5 Thermal Resistance of the TrilithIC

An FEM (finite element method) simulation was used to determine the thermal behavior. The model is shown in **Figure 10**. The molding compound encapsulating the device has been omitted for the sake of clarity, but was taken into account in the simulations. The internal design of the **TrilithICs** is shown in some detail.

A reference PC board is used to verify the simulation.

The test results on this board are explained subsequently.

For the application, it is important first of all to know the steady-state thermal resistance $R_{\text{ths-Pinx}}$ between the chip and the a pin of the **P-DSO-28** package.

For this purpose, the footprint of the package was kept at a constant + 85 °C for each simulation. The resulting temperature distribution during bridge operation for a power dissipation of 2 W and 5 W proportional to the resistance is given in **Figure 11** and **Figure 12**.

It is interesting to note that about 10% of the dissipation takes place in the bond wires.

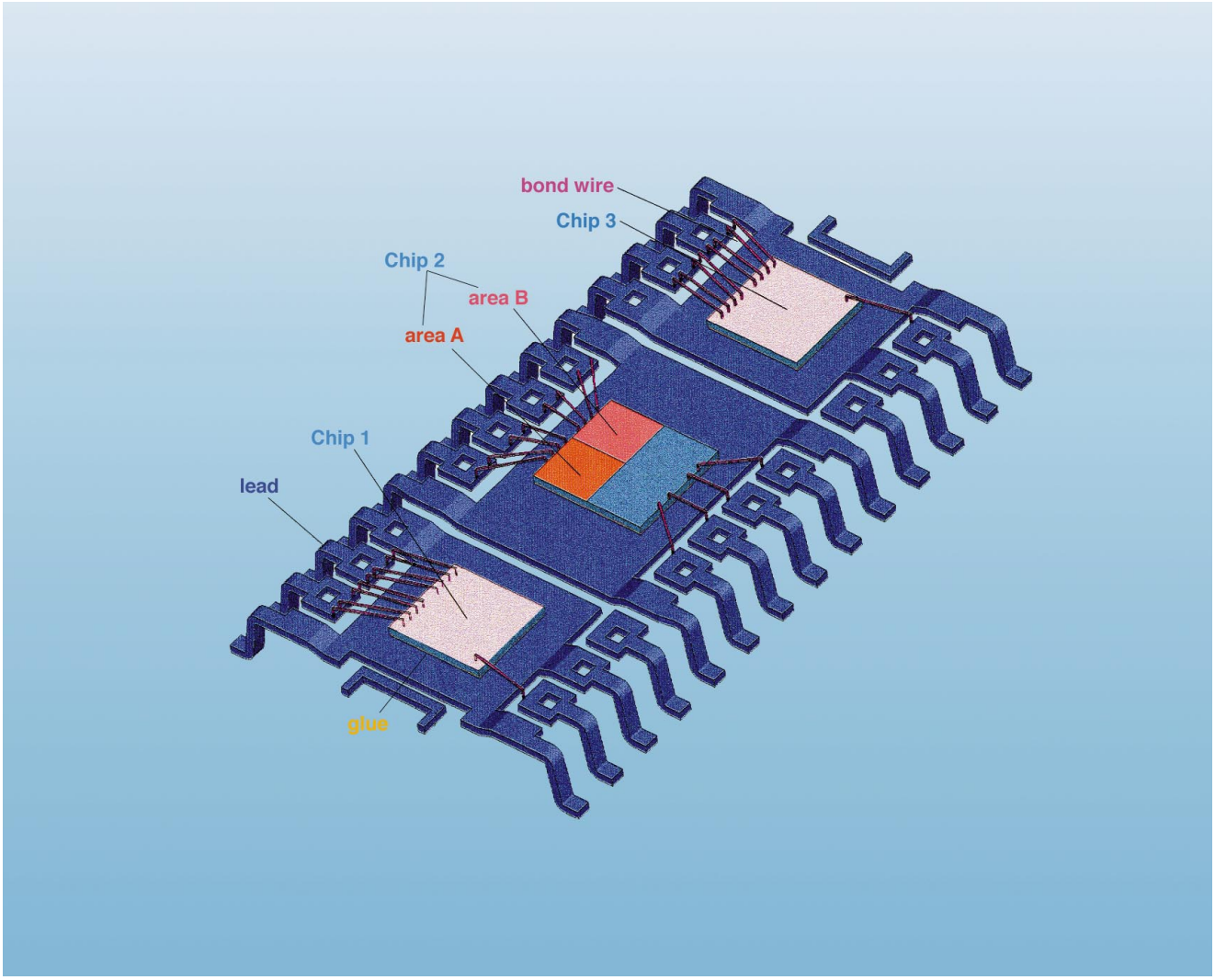

Figure 10
Finite Element Model for Simulating the Temperature Response

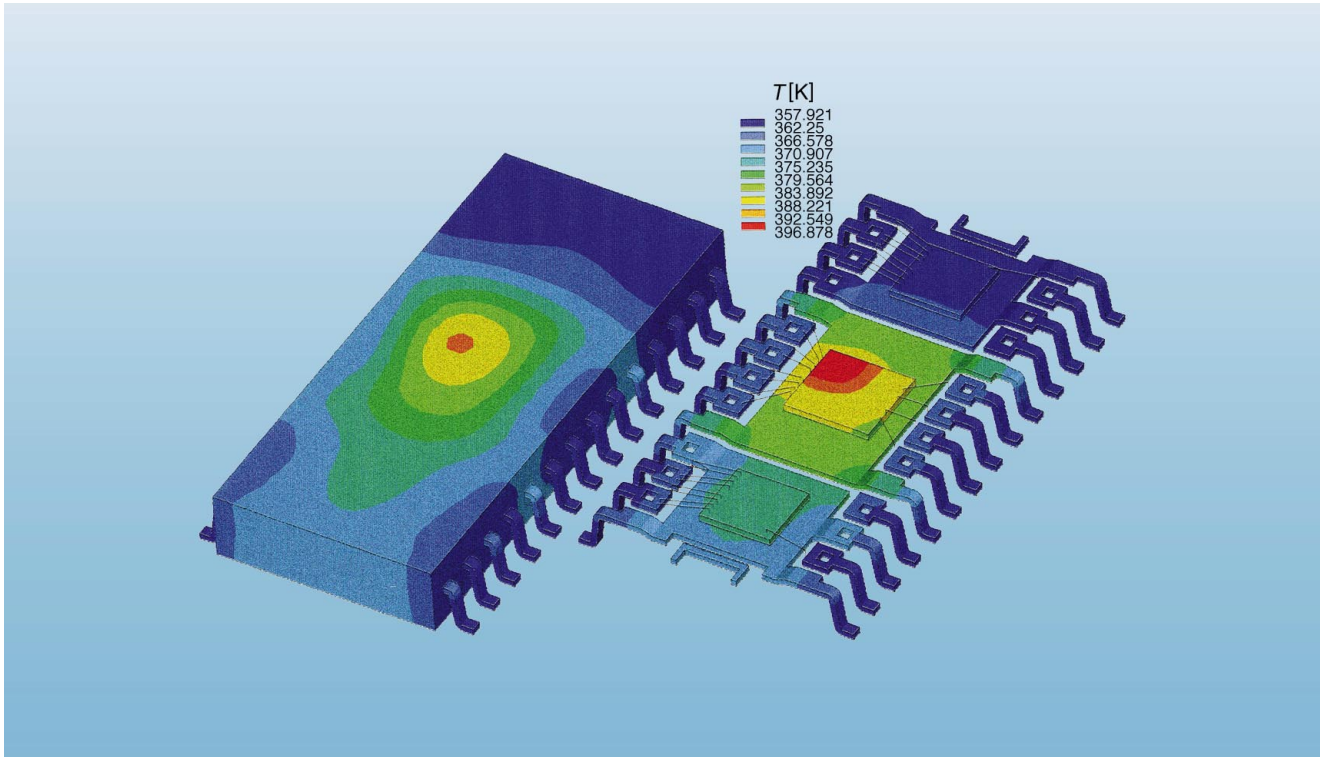

Figure 11
Temperature Response for a Steady-State Power Dissipation of 2 W during Bridge Operation

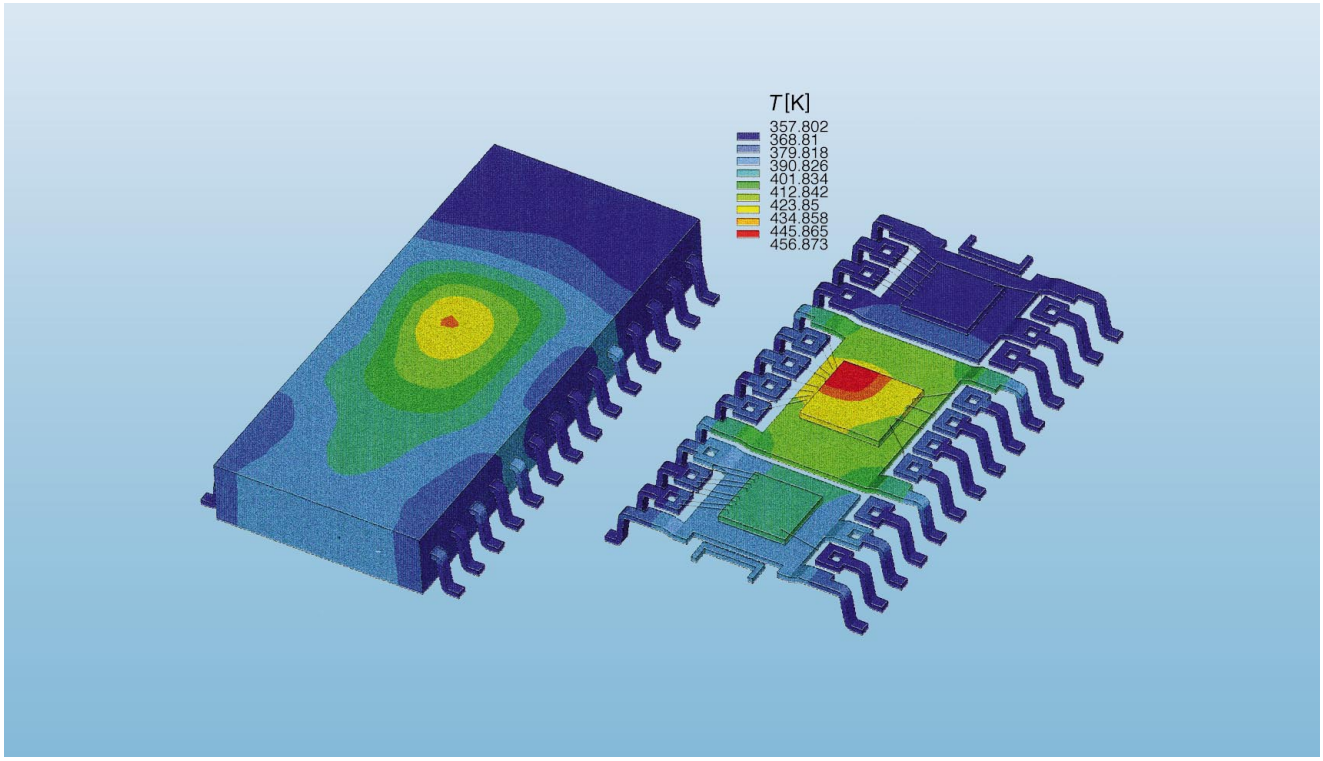

Figure 12
Temperature Response for a Steady-State Power Dissipation of 5 W during Bridge Operation

The heat flow is shown in **Figure 13**. The steep gradients are found on the pins close above the PCB and also in the corner of the loaded high-side chip. A solder fillet directly on the pins therefore helps significantly to reduce the thermal resistance.

$R_{ths\text{-}Pinx}$ is calculated as the temperature difference $T_{ChipMax}$ and T_{Pinx} = 85 °C divided by the applied power dissipation.

Result: $R_{ths\text{-}Pinx}$ = 20 K/W approx for the high-side switch, and the value is only slightly different for the low-side switch.

If the complete application is taken into account, the thermal resistance of the PC board to ambient (RPCB) is added to $R_{ths\text{-}Pinx}$. This gives max. 40 K/W. These relatively high values permit steady-state dissipations of a few watts. Due to the very low ON-state resistances of the **TrilithICs**, this is sufficient to deliver relatively high currents. This is impressively demonstrated below (**Figure 27** and **28**).

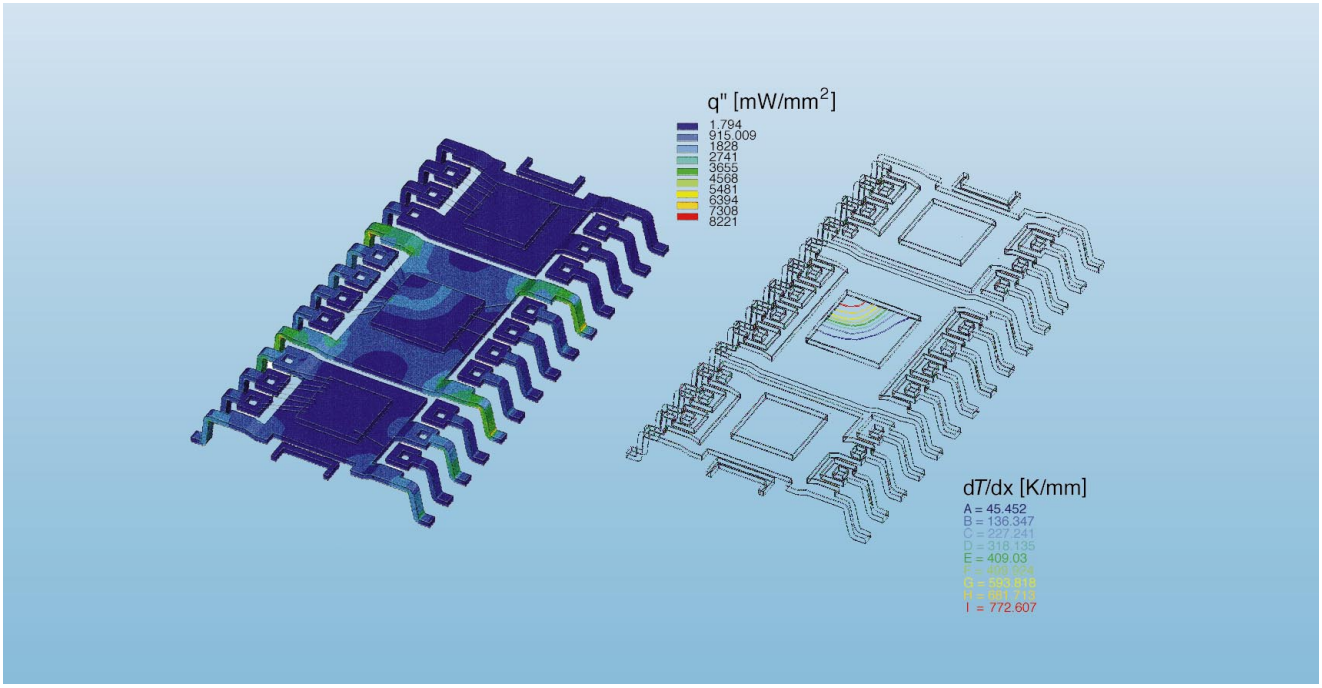

Figure 13
Heat Flow Behavior for Steady-State Power Dissipation of 5 W during Bridge Operation

2.6 Transient Thermal Resistance of the TrilithIC

The possible dissipations under transient conditions for times in the seconds range are, however, much higher. As the majority of DC motor drives with average load inertia come up to rated speed in a few 100 ms, the response of the system in this time range is of critical importance and will now be examined in greater detail.

The thermal impedance Z_{th} was determined as follows:

An initial simulation of the TrilithIC during bridge operation yielded the peak temperature characteristic of the high-side and low-side chip over time. The temperature attained at time t_p divided by the total dissipation (here 5 W) gives the thermal resistance Z_{th} under transient conditions, shown separately in **Figure 14**; for the high-side and low-side chip.

Result: The Z_{th} of the high-side chip remains below 10 K/W for times of up to 100 ms, that of the low-side switch being even less than 2 K/W.

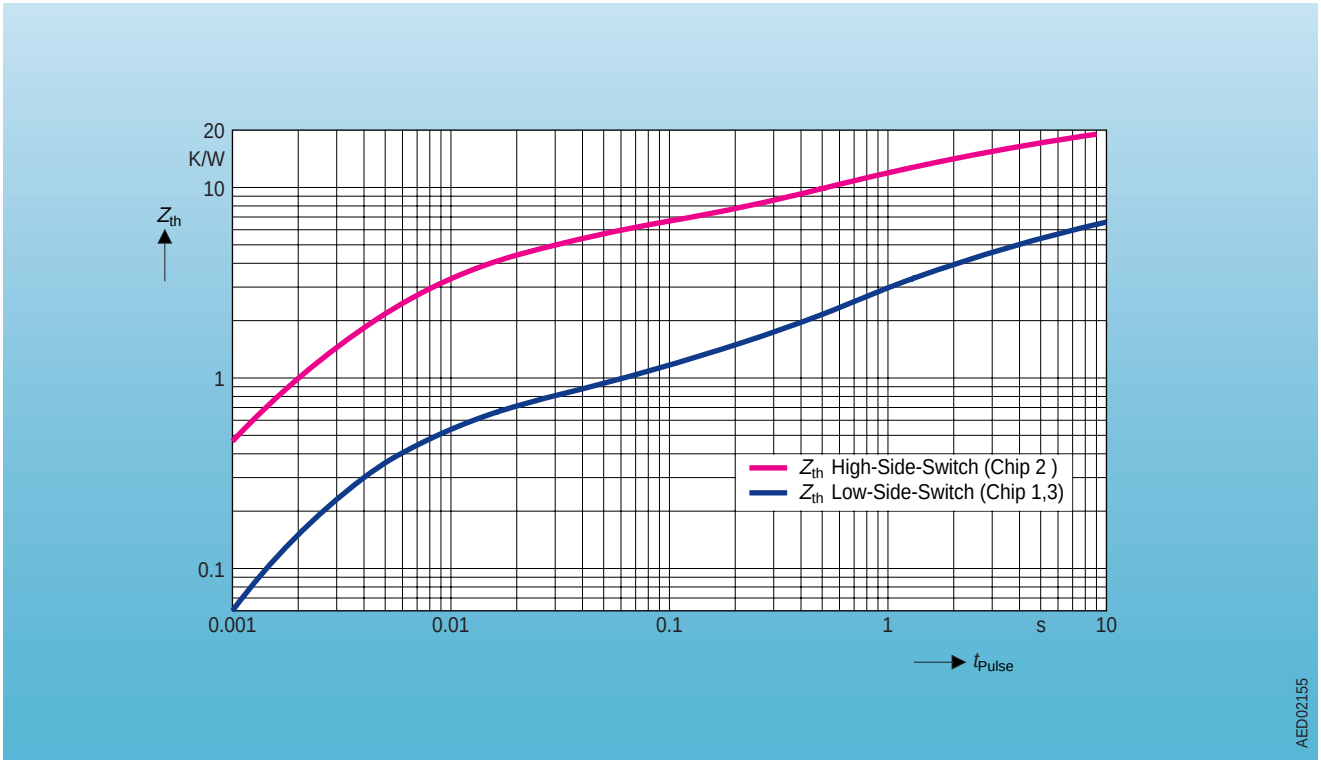

Figure 14
Thermal Impedance or Transient Thermal Resistance for High-Side Chip and for Low-Side Chip

2.7 The Strengths of the TrilithICs in Typical Applications

The advantages of the TrilithICs come strongly to the fore in applications where high starting currents are required for relatively short periods.

Typical of such applications is the electrical doorlock in vehicles with a DC motor system, where currents of up to 8 A are required for periods of up to one second. In practice, of course, this not only involves single pulse operation, but the drive has to function with a particular duty factor for a defined number of operations without being shut down due to overtemperature. Doorlock systems typically employ 50 pulses of 500 ms pulse width with a duty factor of 50% (i.e. 500 ms space between pulses).

This mode of operation was simulated for the frequently recurring pulse periods of 500 ms and 250 ms with pulse powers of 5 W and 10 W respectively. **Figure 15** to **18** show the relevant chip temperature characteristics (high and low side with T_{Lead} = 85 °C).

The period until steady state was achieved was simulated in each case (after 100 s), corresponding to the right-hand side of the diagram. The time axis has been truncated for the sake of clarity. It is apparent that the chip temperature and also the temperature changes of the high-side chip are markedly greater than those of the low-side chip. The peak temperatures increase exponentially to the final value. The fit function indicated contains the parameters for the high-side chip as the “worst-case” scenario.

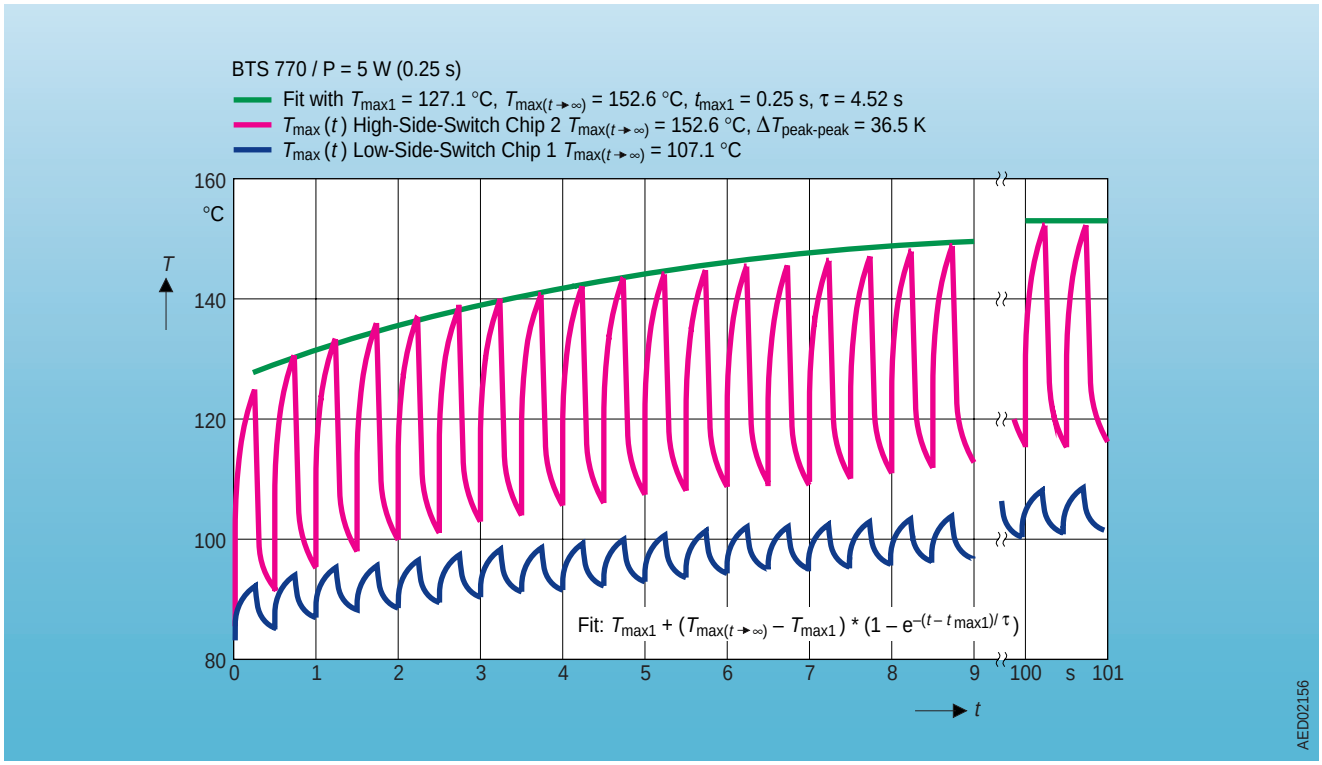

Figure 15
Chip Temperatures in Pulsed Mode with P_v = 5 W for t_p = 250 ms and 50% Duty Factor

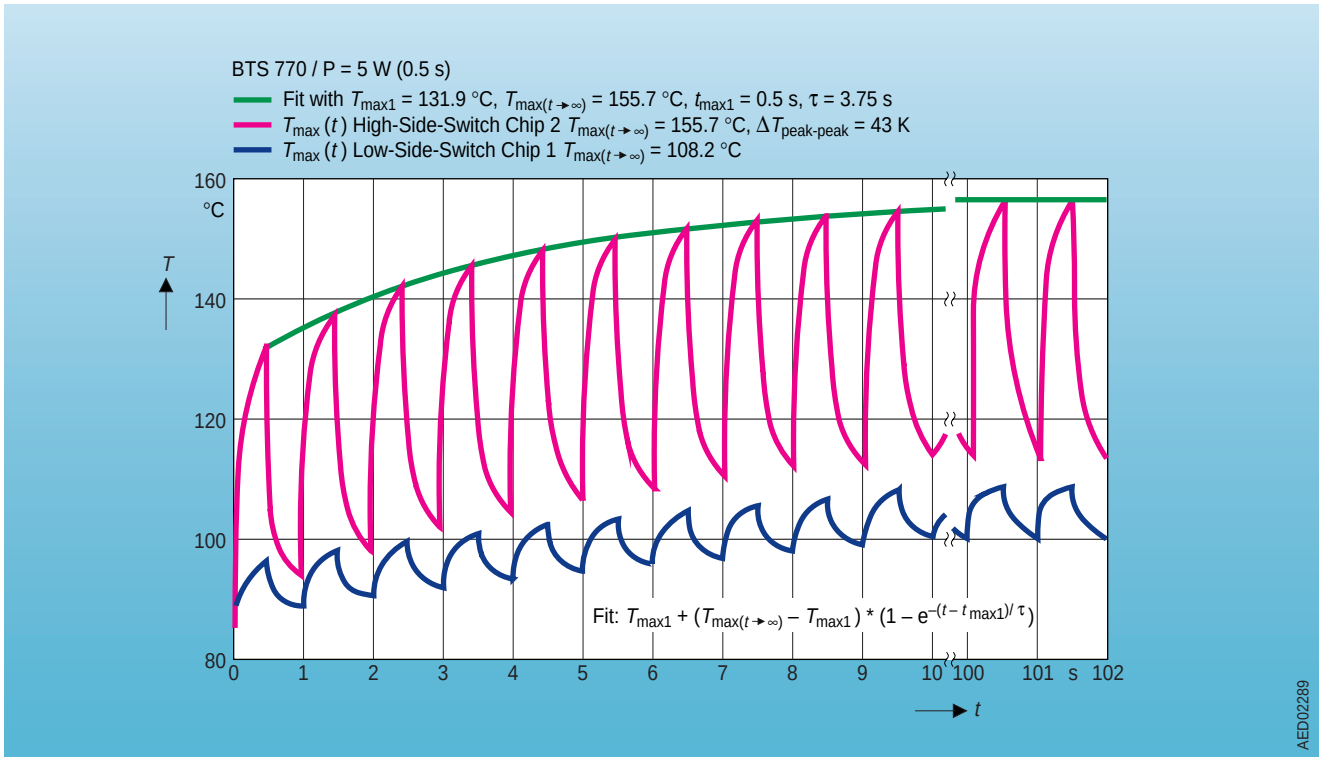

Figure 16
Chip Temperatures in Pulsed Mode with P_v = 5 W for t_p = 500 ms and 50% Duty Factor

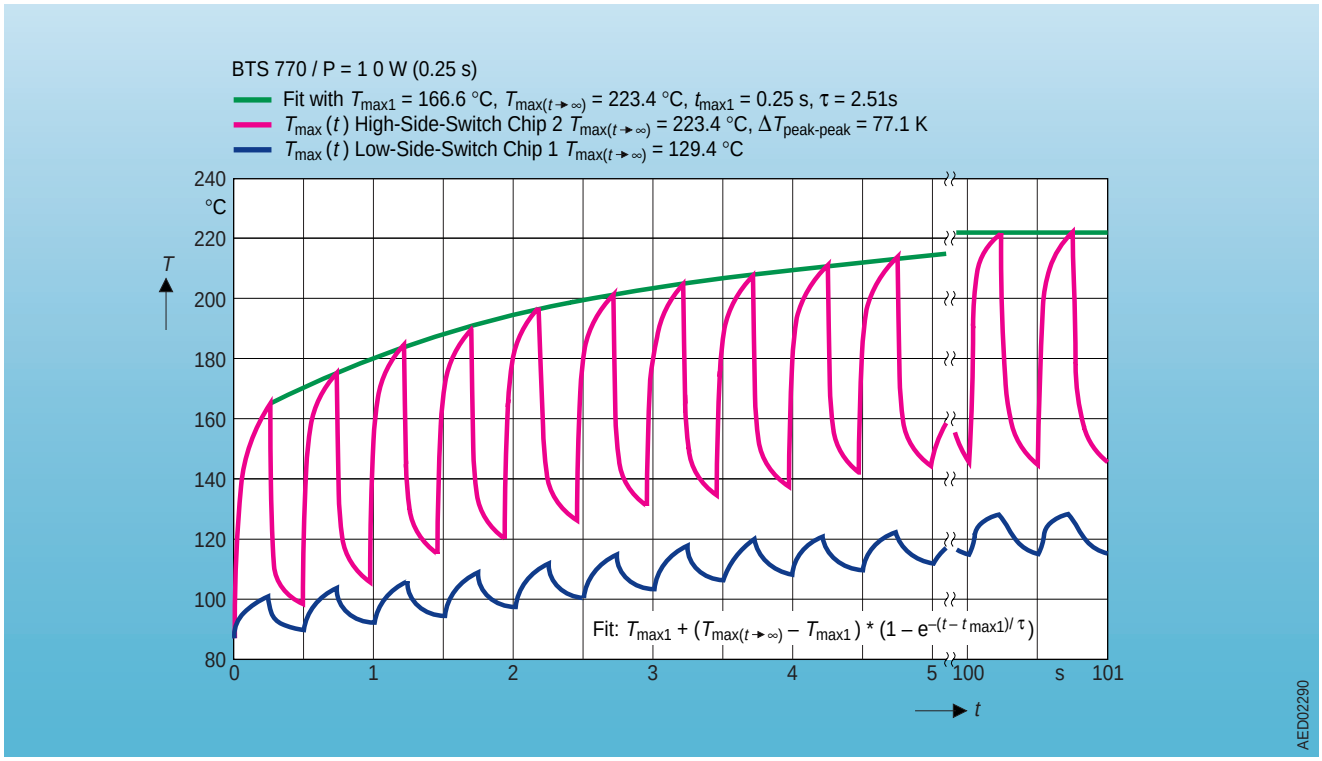

Figure 17
Chip Temperatures in Pulsed Mode with P_v = 10 W for t_p = 250 ms and 50% Duty Factor

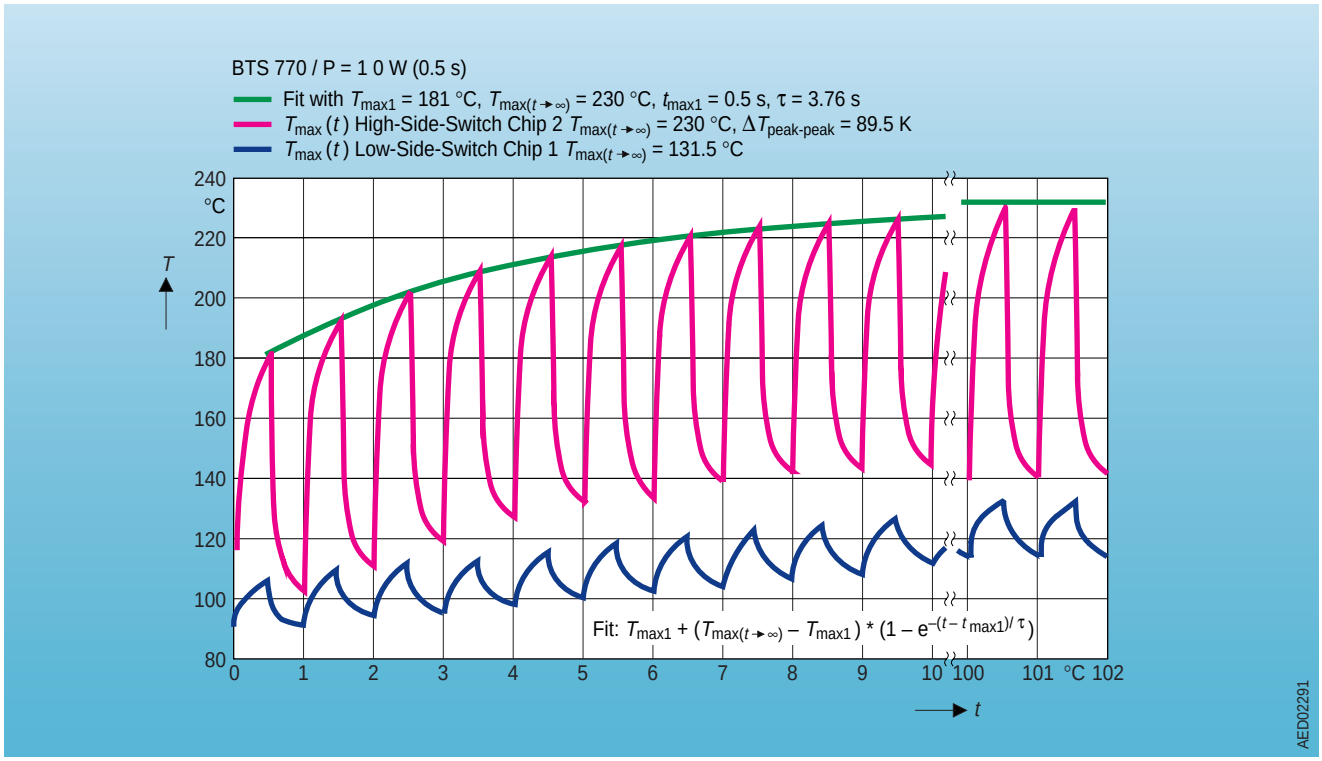

Figure 18
Chip Temperatures in Pulsed Mode with P_v = 10 W for t_p = 500 ms and 50% Duty Factor

2.8 Determining $R_{ths\text{-}a}$ for any Given Application

How will even the best theory stand up in practice? To find out, the simulation was verified using as reference standard PCB (see **Figure 19**) mounted on 1.5 mm thick FR4 material and clad on one side with a 70 µm Cu coating. Clearly visible are the “cooling surfaces” whose areas were made proportional to the ON-state resistance of the switch being cooled and therefore to the power produced.

To determine $R_{ths\text{-}a}$ the chip temperature is measured for various power dissipations. The chip temperature minus the ambient temperature divided by the dissipation gives the required thermal resistance.

The chip temperature was measured as follows:

First the forward voltage of an on-chip diode at low current is measured as a function of the chip temperature (e.g. 1 mA); preferably the substrate diode of the status output (diode to ground with cathode at status output). The measurement can easily be performed in any controlled-environment chamber. Assumption: The ambient temperature is equal to the chip temperature, because little power conversion occurs in the chip. The resulting temperature calibration curve $V_{FST} = f_{(Tj)}$, applicable to BTS 770 and BTS 771 is shown in **Figure 20**.

Power is now applied to a bridge circuit. The status output is used as before to measure clamping diode forward voltage V_{FST}. This yields the function $T_j = f(P_v)$ shown in **Figure 21** whose gradient is the required thermal resistance.

For the reference board, this value is between 20 and 25 K/W in moving air. It is sufficient always to determine the high-side chip temperature, as it is the highest in the system.

In order to obtain approximate values for smaller cooling surfaces, simulations were performed using smaller surface areas. **Figure 22** shows the thermal resistance determined in this way as a function of the cooling surface area. As this function is dependent on a large number of parameters, it is only valid for the reference board.

For applications with a different geometry and any given additional features, the thermal resistance of the system to ambient may easily be determined using the above method.

A further application-supporting step is being taken by providing a thermoelectrical model for P-SPICE. Separate models are available for **BTS 770** and **BTS 771**. This enables the electrical behavior of the power MOS transistors to be taken into account. The relevant chip temperatures are output as voltage equivalents. The performance of the model and the advantages for the user will be demonstrated with the aid of an example.

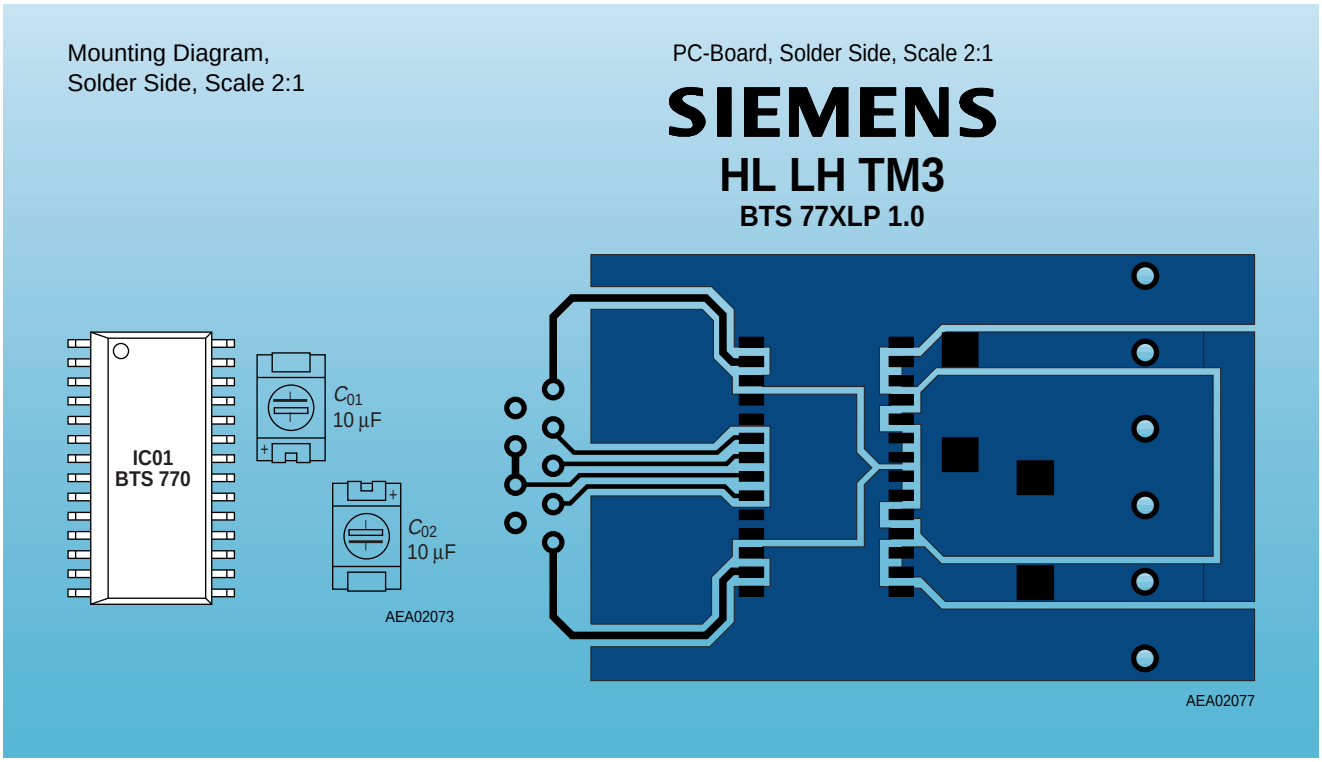

Figure 19
Layout of the Standard PCB for BTS 770 and BTS 771

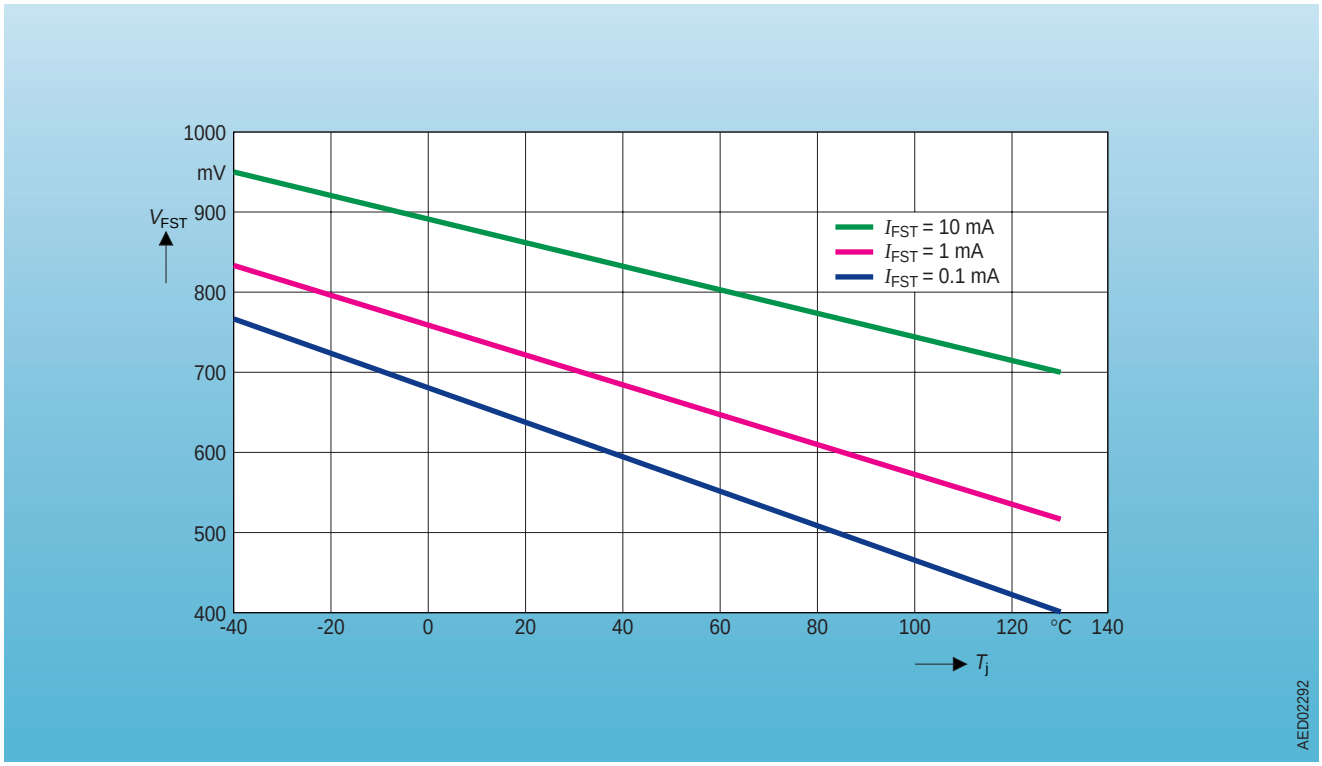

Figure 20
Calibration Curve $V_{FST} = f_{(Tj)}$ for Determining the Chip Temperature of the High-Side Chip

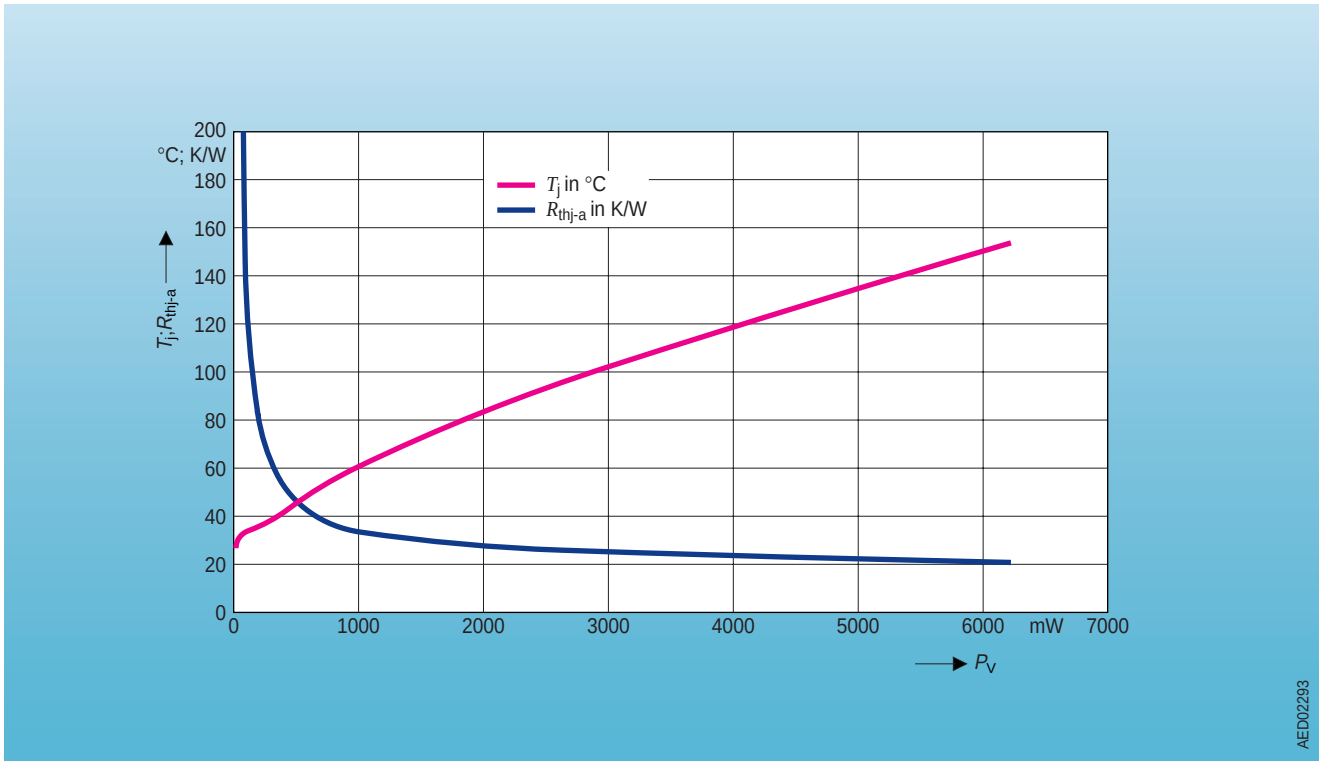

Figure 21
Chip Temperature and Thermal Resistance of the TrilithIC in the Reference Board as a Function of the Dissipation

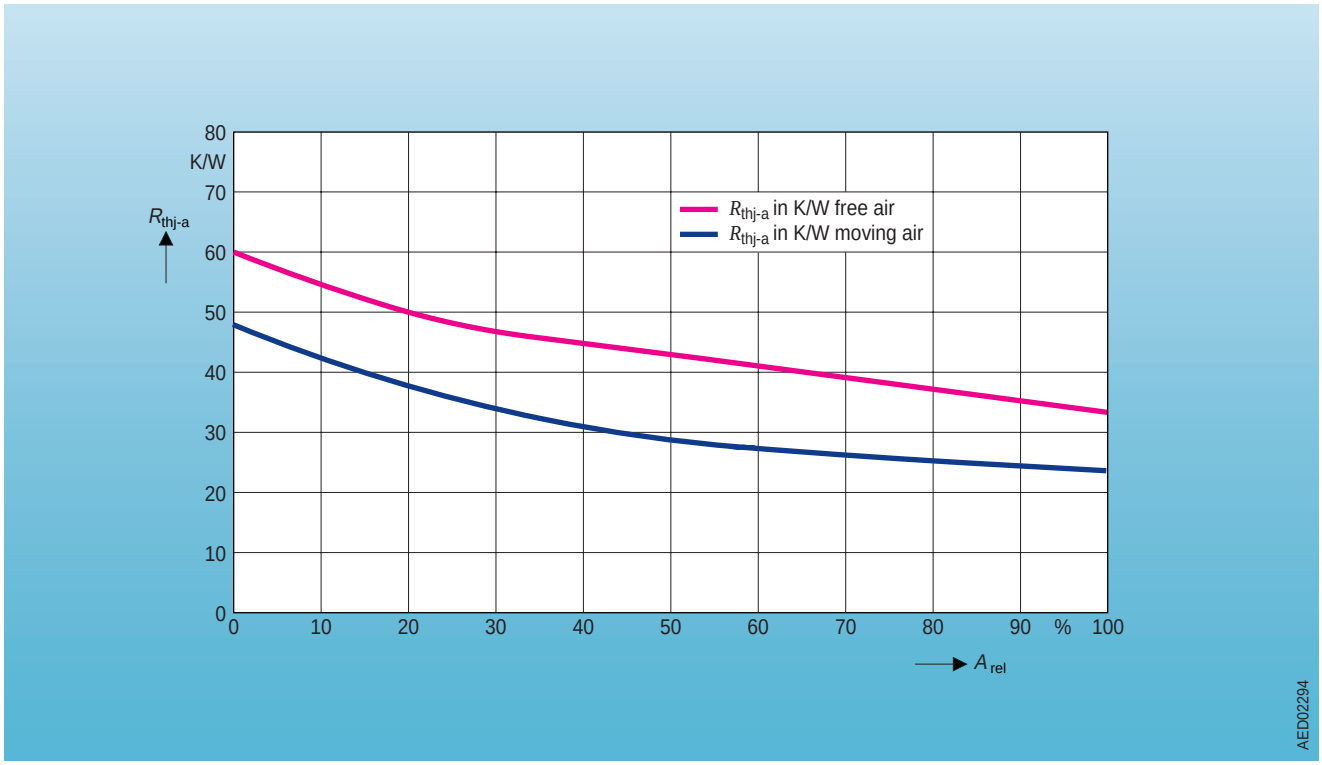

Figure 22
Thermal Resistance of the TrilithIC in the Reference Board as a Function of PCB Cooling Surface

2.9 Basic Data for the TrilithICs

Table 1 summarizes the basic data for TrilithICs **BTS 770** and **BTS 771**.

Table 1

Parameter	BTS 770	BTS 771
Package	P-DSO-28	P-DSO-28
Supply voltage operating range	4 V to 40 V	4 V to 40 V
Peak output current at 85 °C	min. 5.5 A	min. 7.5 A
Current flowing in standby state	max. 35 µA	max. 35 µA
R_{DSON} HSS at 25 °C	typ. 165 mΩ	typ. 85 mΩ
R_{DSON} HSS at 150 °C	max. 360 mΩ	max. 200 mΩ
R_{DSON} LSS at 25 °C	typ. 55 mΩ	typ. 40 mΩ
R_{DSON} LSS at 150 °C	max. 110 mΩ	max. 100 mΩ
Diagnostics: Overload	Yes	Yes
Diagnostics: Overload	Yes	Yes
Diagnostics: Overtemperature	Yes	Yes
Diagnostics: Short to GND	Yes	Yes
Diagnostics: Short to V_S	Yes; passive[1)]	Yes; passive[1)]

1) Each output is monitored for prohibited potentials when the high-side switches are in the passive state. If the output voltage rises to more than about 3 V due to leakage or short circuit to supply voltage V_S, the status output is switched to LOW. This feature can be usefully employed to protect the low-side switches.

The key parameters $R_{DSON} = f_{(Tj)}$ and peak output current $I_{SC} = f_{(Tj)}$ are shown in **Figure 23** to **26**. Note the very low branch resistance of less than 500 mΩ for the **BTS 770** and even less than 300 mΩ for the **BTS 771**. These are unrivaled values. The same applies to the high peak currents and not least to the extremely low currents flowing in the standby state.

For all drives requiring continuous operation, the current which the **TrilithIC** can supply for any given thermal resistances is a critical parameter. If $R_{thj\text{-}a}$ is known for a particular application, this current value can be determined as follows:

T_{jmax} = 150 °C (max. chip temperature)

$R_{thj\text{-}a}$ = 35 K/W (thermal resistance junction to ambient)

T_{amax} = 85 °C (max. ambient temperature)

we obtain via the relation:

$P_{vmax} = (T_{jmax} - T_{amax}) / R_{thj\text{-}a}$ (max. dissipation)

and

$P_{vmax} = (I_{out})^2 \times R_{path}$

by equating the function:

$I_{outmax} = f_{(Ta)}$, the maximum possible continuous output current

These functions are given in **Figure 27** and **28** for the **BTS 770** and the **BTS 771**. Parameter $R_{thj\text{-}a}$ of these curves is dependent on the external cooling arrangements and can be determined for each application as described above.

Result: With the **BTS 770**, applications with continuous currents of up to 2.5 A are possible under the above conditions.
For the **BTS 771**, applications up to 3.2 A are possible.

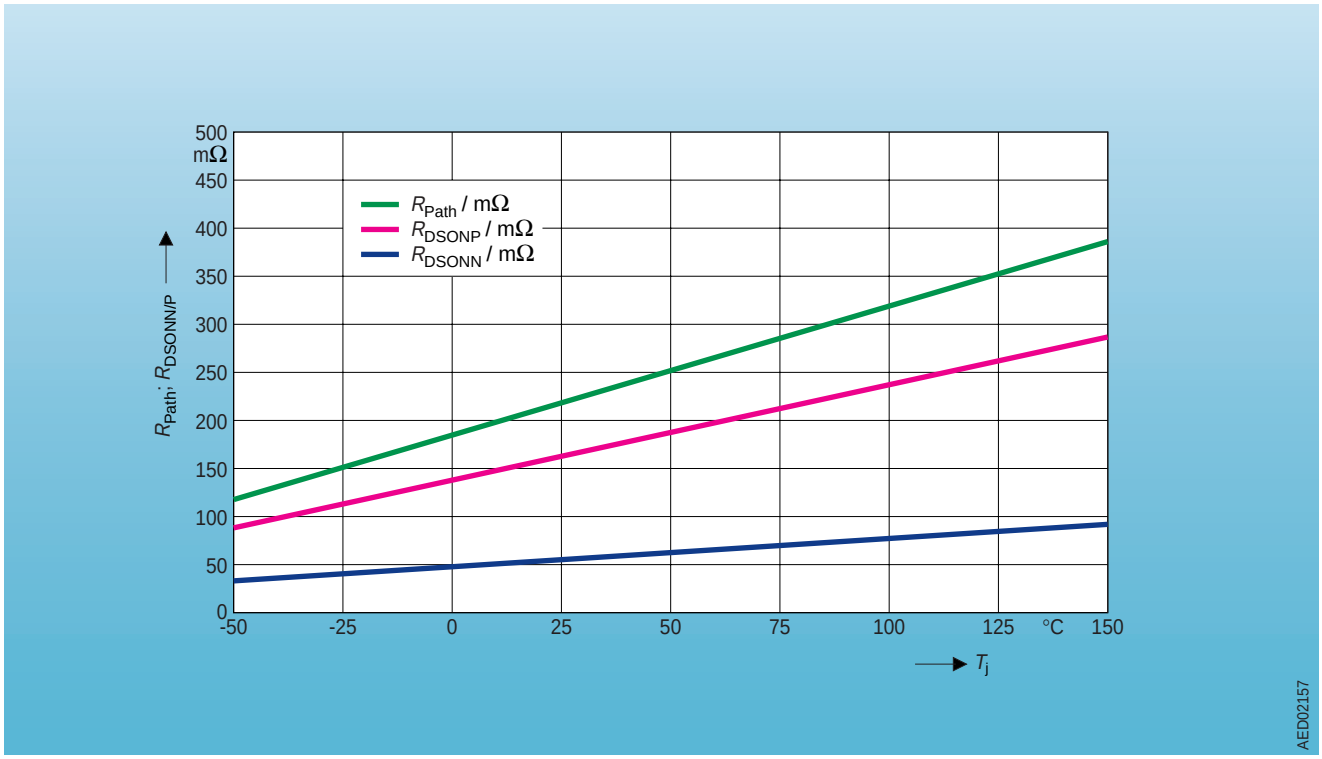

Figure 23
High- and Low-Side ON-State Resistances of the BTS 770 as a Function of Chip Temperature, the Sum of the Two as Path Resistance being Additionally Given

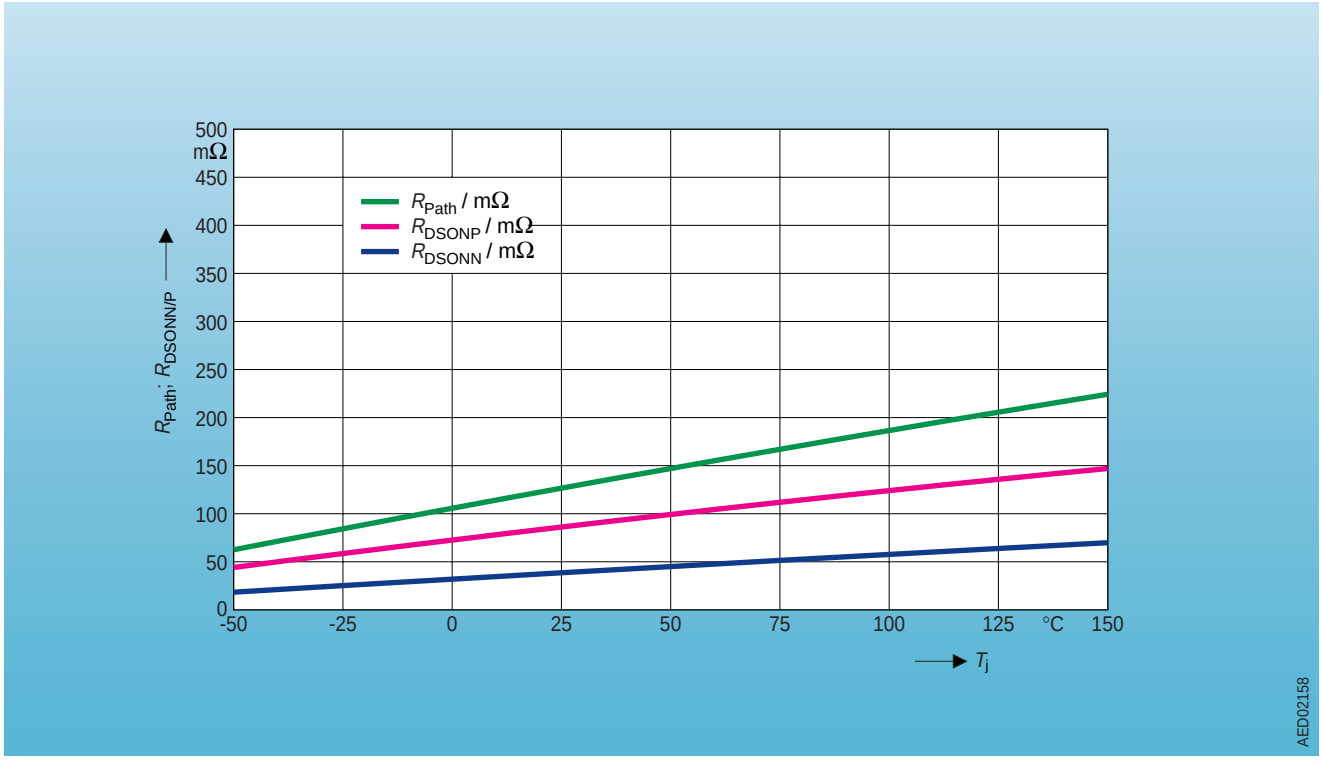

Figure 24
High- and Low-side ON-state Resistances of the BTS 771 as a Function of Chip Temperature, the Sum of the Two as Path Resistance being Additionally Given

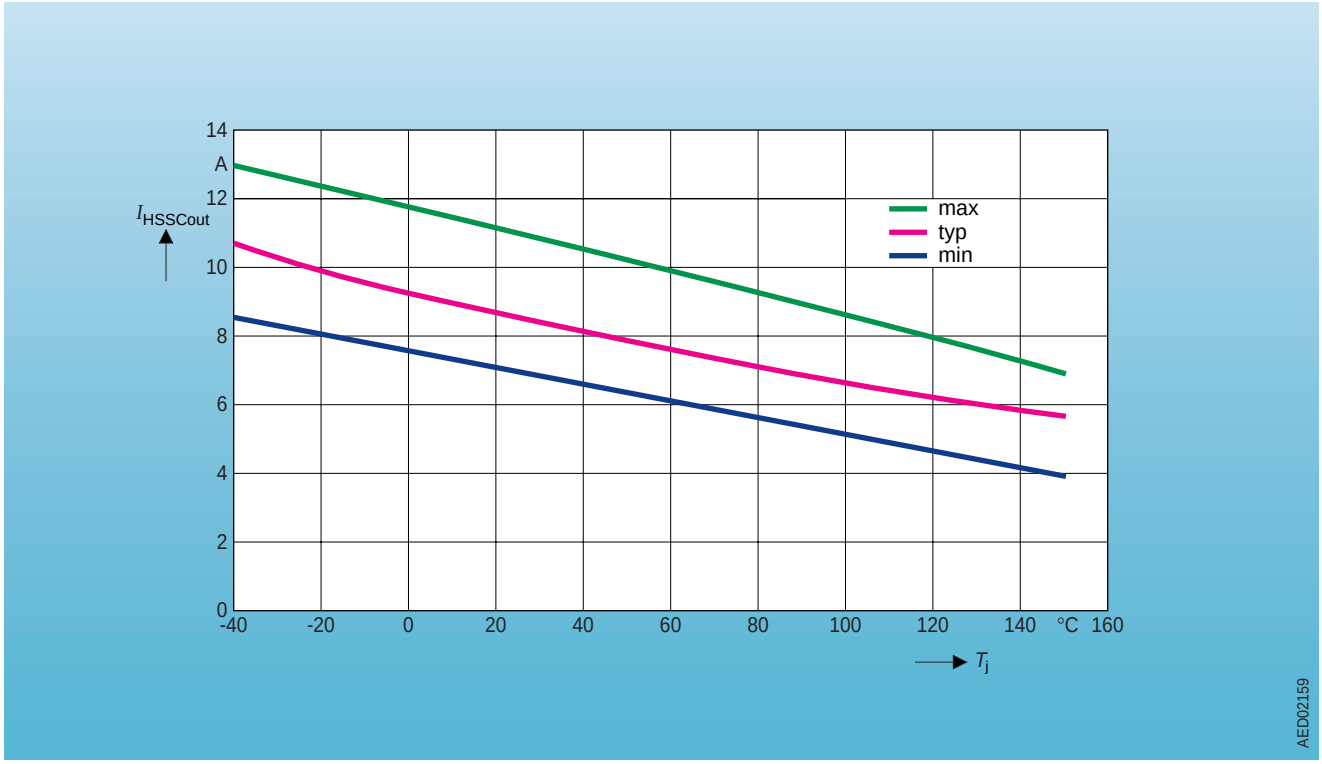

Figure 25
Short-Circuit Output Current of the BTS 770 as a Function of Chip Temperature

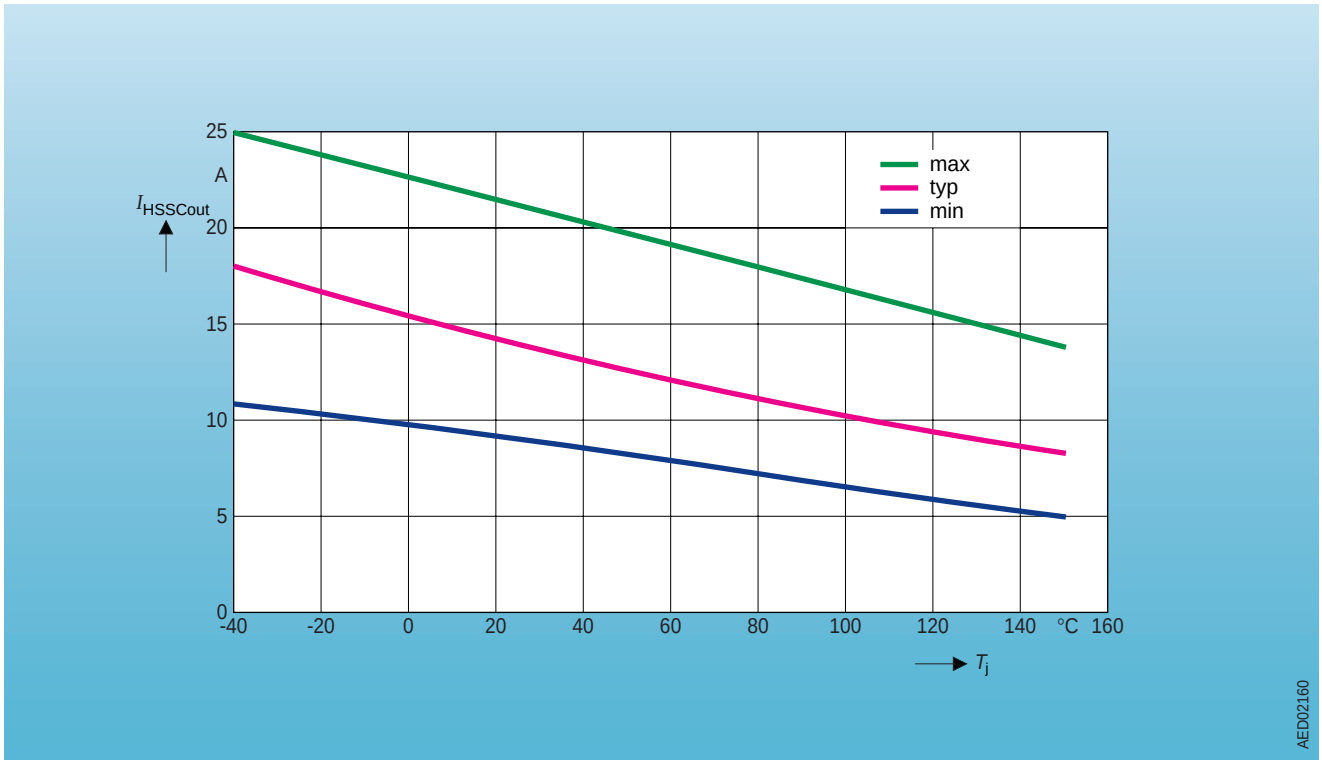

Figure 26
Short-circuit Output Current of the BTS 771 as a Function of Chip Temperature

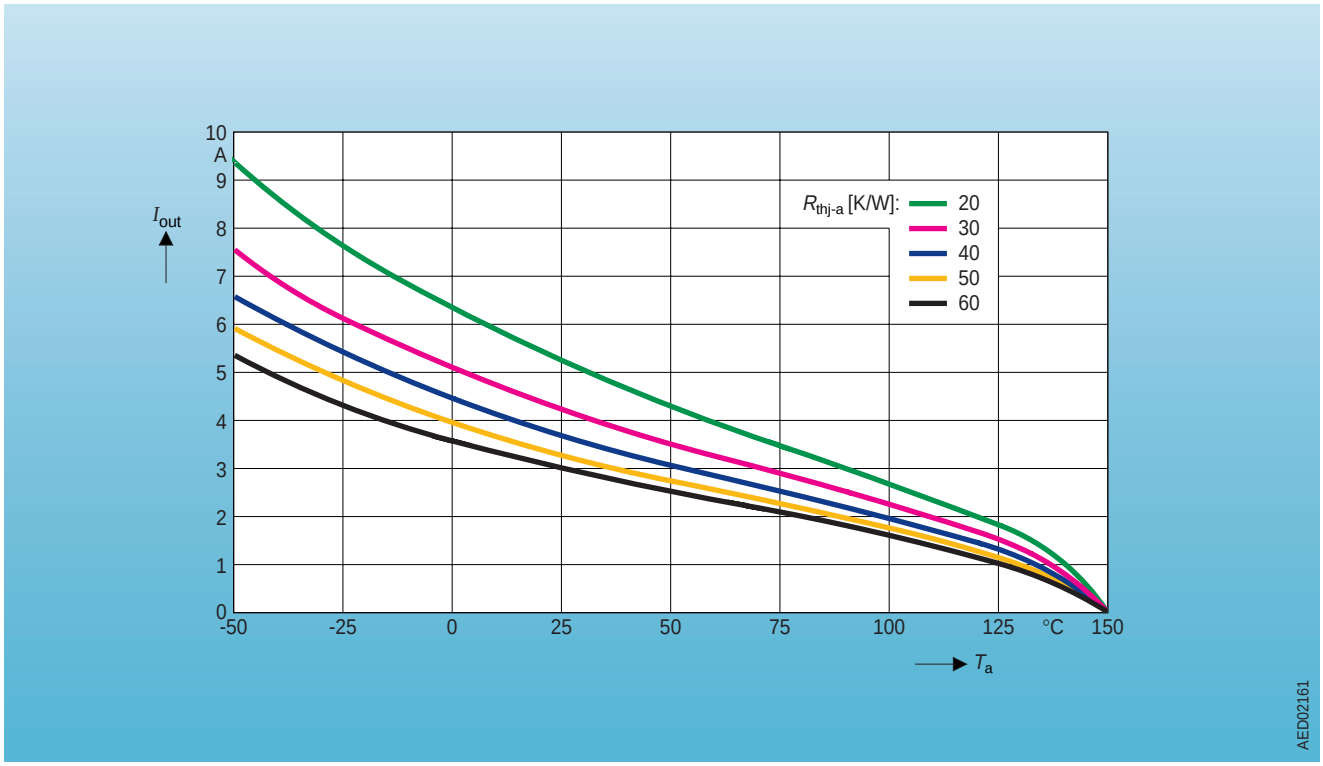

Figure 27
Maximum Permissible Continuous Current of the BTS 770 in Bridge Configuration as a Function of Chip Temperature (with the junction-to-ambient thermal resistance as parameter)

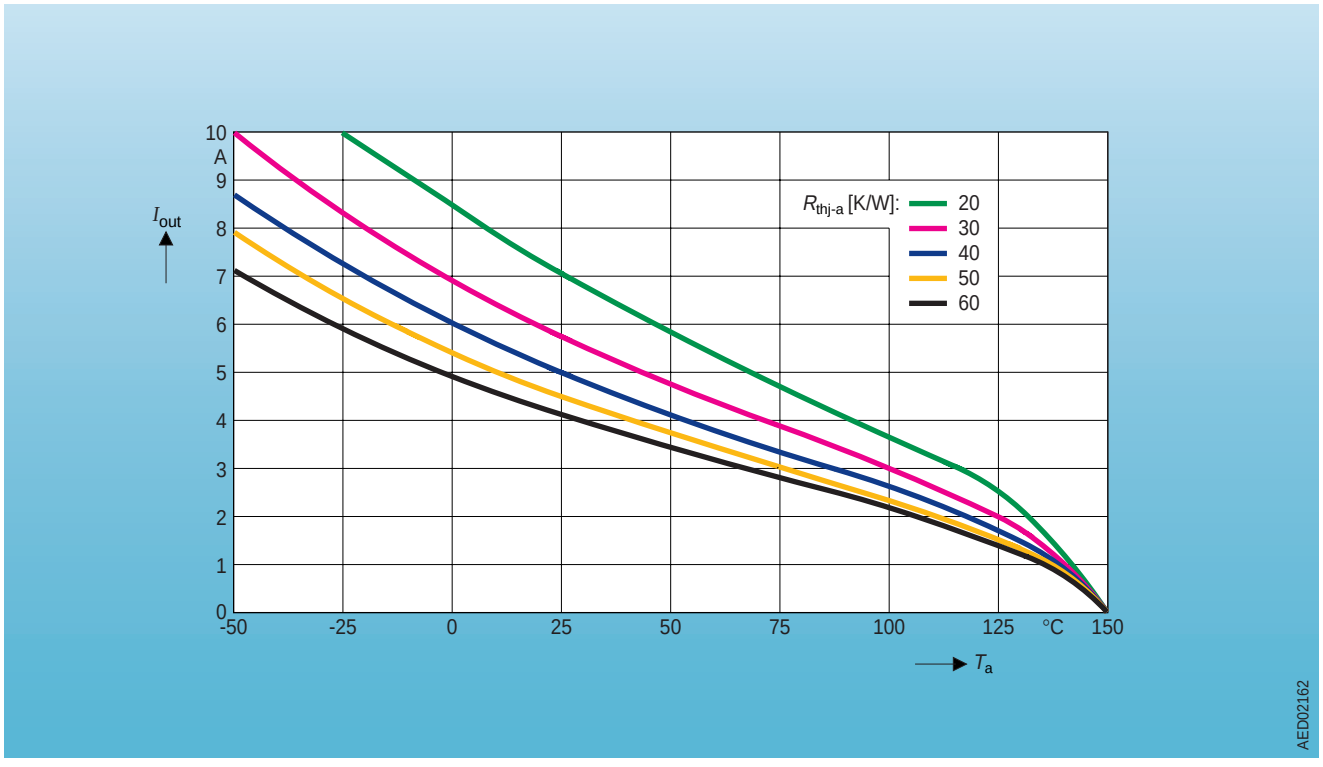

Figure 28
Maximum Permissible Continuous Current of the BTS 771 in Bridge Configuration as a Function of Chip Temperature (with the junction-to-ambient thermal resistance as parameter)

3 Application

A typical application is illustrated in **Figure 29**. It shows the **BTS 770** chip as driven by a microcontroller.

The control interface consists of five lines; one for each switch and one for the status signal, thereby providing maximum flexibility. It should be noted that the charge pumps of the high-side switches require a relatively long time (approx. 400 µs) for turning on/off compared to the extremely fast low-side switches. When the bridge reverses direction with simultaneous control signals, high- and low-side switches would briefly become conducting, producing a transverse current through the half-bridge arm. Although this cannot damage the device, as it is controlled by the high-side switch, it may cause an unwanted power dissipation pulse. In addition, the current pulse produces electromagnetic emissions. The simple solution to this problem is to provide suitable timing for the drive system, e.g. by inserting a dead time of approximately 1 ms between high-side switch OFF and low-side switch ON.

The microcontroller is fed by the **SIEMENS TLE 4268G** low-drop voltage regulator and initialized using the watchdog and reset functions of this highly EMI-resistant product designed for standalone systems.

Motor bridge **BTS 770/1** requires no external circuitry apart from the polarity reversal protection diode and a relatively small storage capacitor CS.

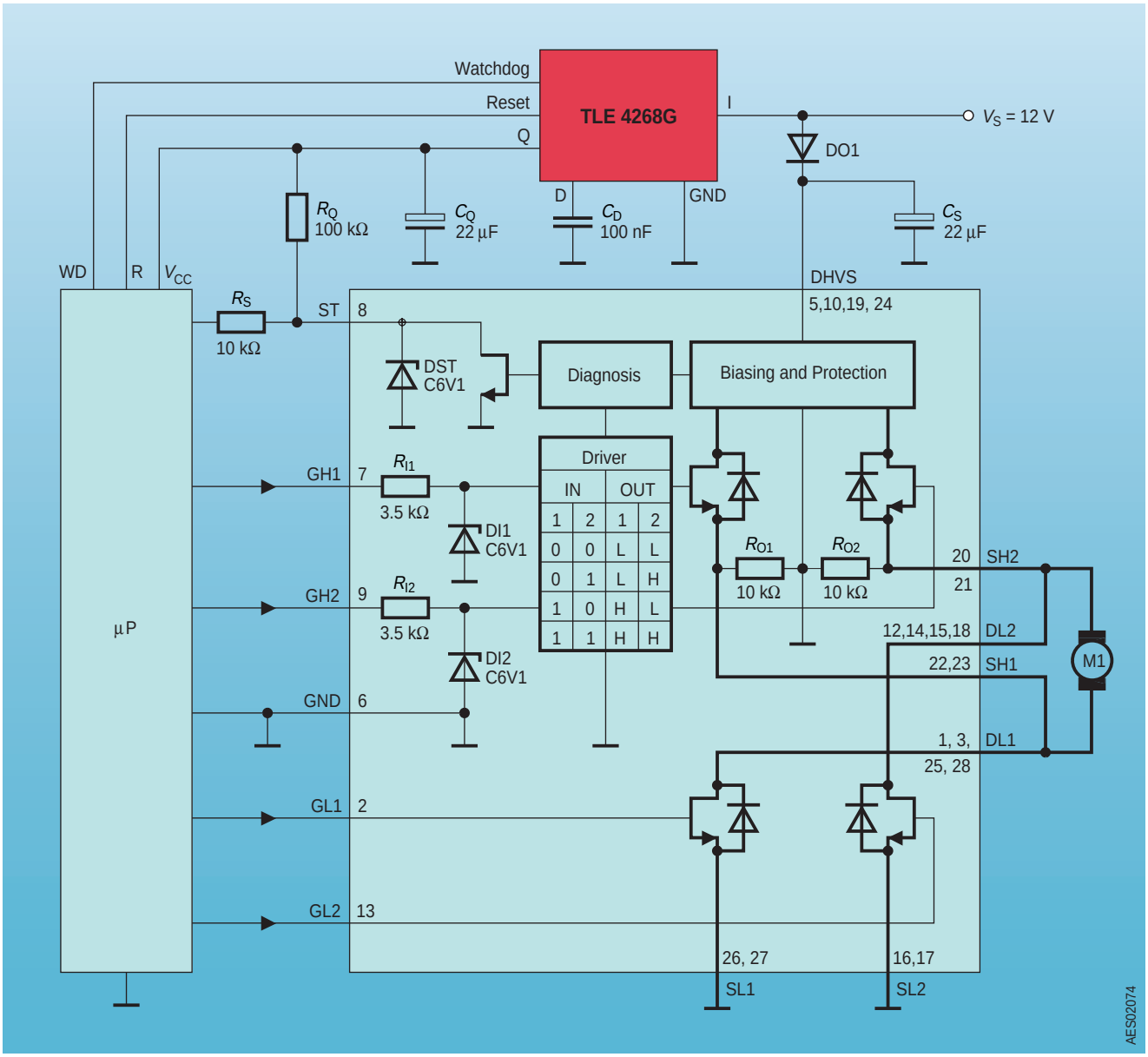

Figure 29
Standard Application Circuit for the TrilithIC

3.1 Short Circuit and Overload

The outputs are protected against overload and short-circuits to ground.

As already mentioned, the output of the two high-side switches in the passive state uses a comparator with an internal reference voltage of about 3 V (output examiner voltage, V_{EO}). If the output voltage exceeds 3 V, a status signal is produced.

This can be usefully employed to protect the low-side switches against shorts to the supply. The output potentials normally will drop to ground potential via two resistors R_{01}, R_{02} incorporated in the high-side switches (see **block diagram**) when the high-side switches are OFF. If they fail to do so, a leakage or short circuit to the supply voltage is present which is reported to the interface via the status signal. An intelligent controller can thus prevent the low-side switches from operating in response to overloads.

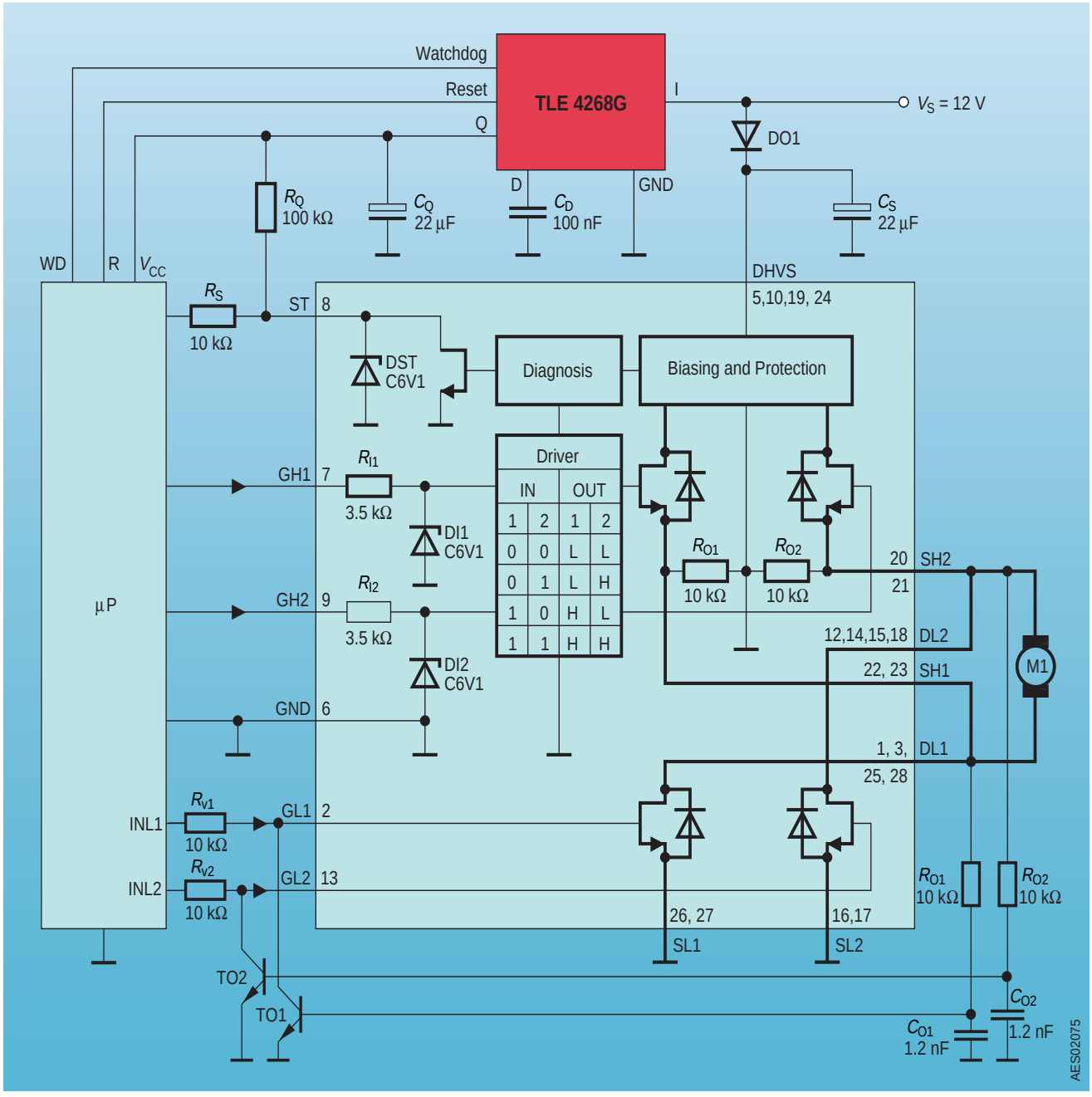

Figure 30
Application Circuit of TrilithIC with Short-Circuit Protection with Respect to Supply Voltage

If short-circuit protection with respect to the supply voltage is additionally required, the circuit shown in **Figure 30** can be used. In this case the output voltages are monitored by the RC networks (R0, C0), isolating resistors R_v and NPN transistors TO1/TO2. The RC combinations are used to suppress transient interference pulses such as may be produced by the motor's brush sparking. The time constant must be approximately 10 to 50 µs, during which time the low-side chip can handle currents of up to 50 A at full voltage. The drive circuit is isolated from the gate via series resistors. For output voltages of below 0.7 V (basis-emitter threshold of the NPN transistor), the circuit remains passive. However, if the output voltage is increased due to a leakage or even a short to the supply, the NPN transistors switch the gate of the power MOS being protected to ground potential. This state remains stored until the leakage or short circuit at the output is removed. The fault flip-flop is reset when the output voltage falls below the holding threshold of about 0.6 V via resistors R_{01}, R_{02} = 10 kΩ incorporated in the high-side switches.

The signal response for passive high-side switch is illustrated in **Figure 31** left (output examiner function). The right-hand side shows the behavior of the additional circuitry with active high-side switch.

As indicated above, each high-side switch contains a so-called output examiner. This circuit monitors the output for impermissibly high potentials while the high-side switch is off.

If the output exceeds the fault threshold of about 3 V due to a fault current being injected into the output, the status output switches to LOW. Appropriate control software detects this and blocks activation of the corresponding low-side switch.

This facility requires no additional circuitry. However, it does not provide protection against hard short circuits during bridge operation. In this case help is provided by the external error memory as follows:

At instant 3, high-side switch 1 is activated. Shortly afterwards (at instant 4), the status output signals “OL = open-load” because LS switch 2 of the bridge was not switched on. The error memory at the gate of low-side switch 2 is already set. The switch-on command supplied from the interface for low-side switch 2 at instant 5 therefore remains ineffective (gate is clamped to ground). To reset the error memory, high-side switch 1 is turned off between instants 6 and 7. The output voltage floats to ground via integrated resistors R_{01}, R_{02} the gate clamping is removed and the bridge assumes rated operation from instant 7 onwards.

At instant 8, output 2 is shorted to the supply. During the dead time t_{sc} of the error memory (approx. 12 µs), the output current rises to high values. Low-side switch 2 is then turned off until the error memory is reset by the high-side switch also being turned off.

This elegant solution provides the BTS motor bridge driver with complete short-circuit protection.

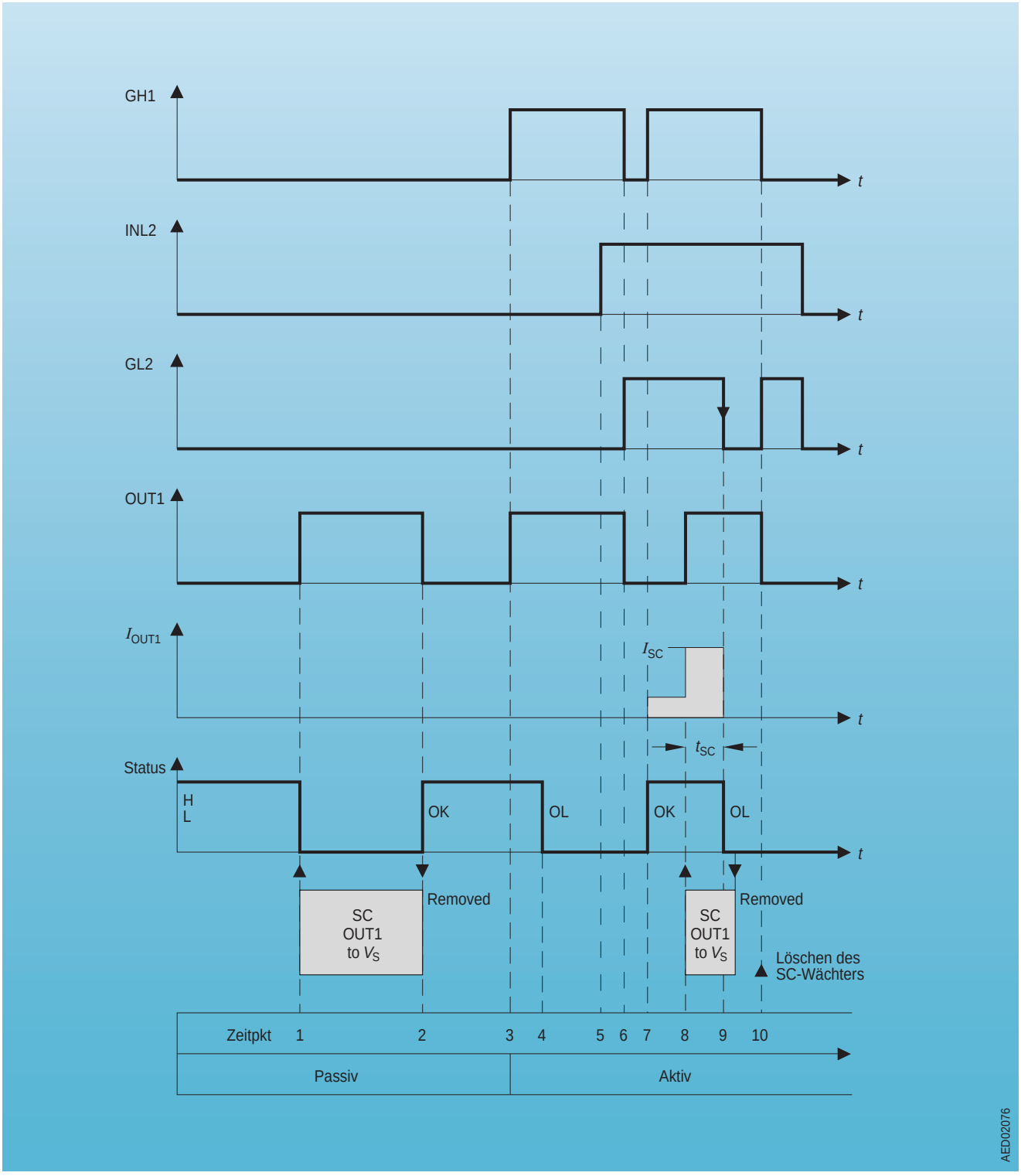

Figure 31
Functional Diagram of Short-Circuit Protection Arrangement in Figure 30

3.2 Measurements in the Application

Let us first consider the short-circuit behavior. If the BTS bridge switches in response to a short circuit, the current rises steeply through the power transistors (retarded only by the parasitic inductance) - see **Figure 32.**

The high-side switch limits the current to a value depending on the relevant chip temperature (instant 1).

Note:

The peak power in the P-DSO-28 package during this instant is
approx. 12 V $\times$ 7 A = 84 W for the **BTS 770** and
as much as approx. 12 V $\times$ 13 A = 154 W for the **BTS 771**.

Controlled by the heat dissipation, the current value falls until the temperature protection threshold is reached (instant 2). The bridge is then clocked at a duty ratio controlled by the chip temperature. Observation of the drop voltages (voltage difference between the output and the supply voltage for the high-side switch and between the output and ground for the low-side switch) indicates that the low-side switch produces little dissipation during this time (peak values of only about 0.4 V $\times$ 7 A = 2.8 W for the **BTS 770** and about 0.7 V $\times$ 13 A = 9.1 W for the **BTS 771**).

In order to maintain the high SIEMENS quality standard, BTS bridges are subjected to this mode of operation for 2000 h in the product qualification life test.

If the motor current is to be controlled, sense resistors can be inserted in the source lines of the low-side switches so that the motor current can be controlled by pulsing the relatively fast low side switches.

Low-frequency current control at approx. 1 kHz is illustrated in **Figure 33**.

The commutation voltage and current peaks are clearly visible. The motor current response for locked motor is likewise shown. We can see that the **BTS 770** is capable of switching currents of 5.5 A, the **BTS 771** correspondingly more.

The “sign-magnitude” control principle is illustrated in **Figure 34**. Here the motor inductance is used to determine the current by higher-frequency switching of the relevant low-side switch, such as in switched-mode power supplies. A chopping frequency of 100 kHz was selected for the above example. As the switching times are extremely low, this mode of operation could also be used with higher frequencies.

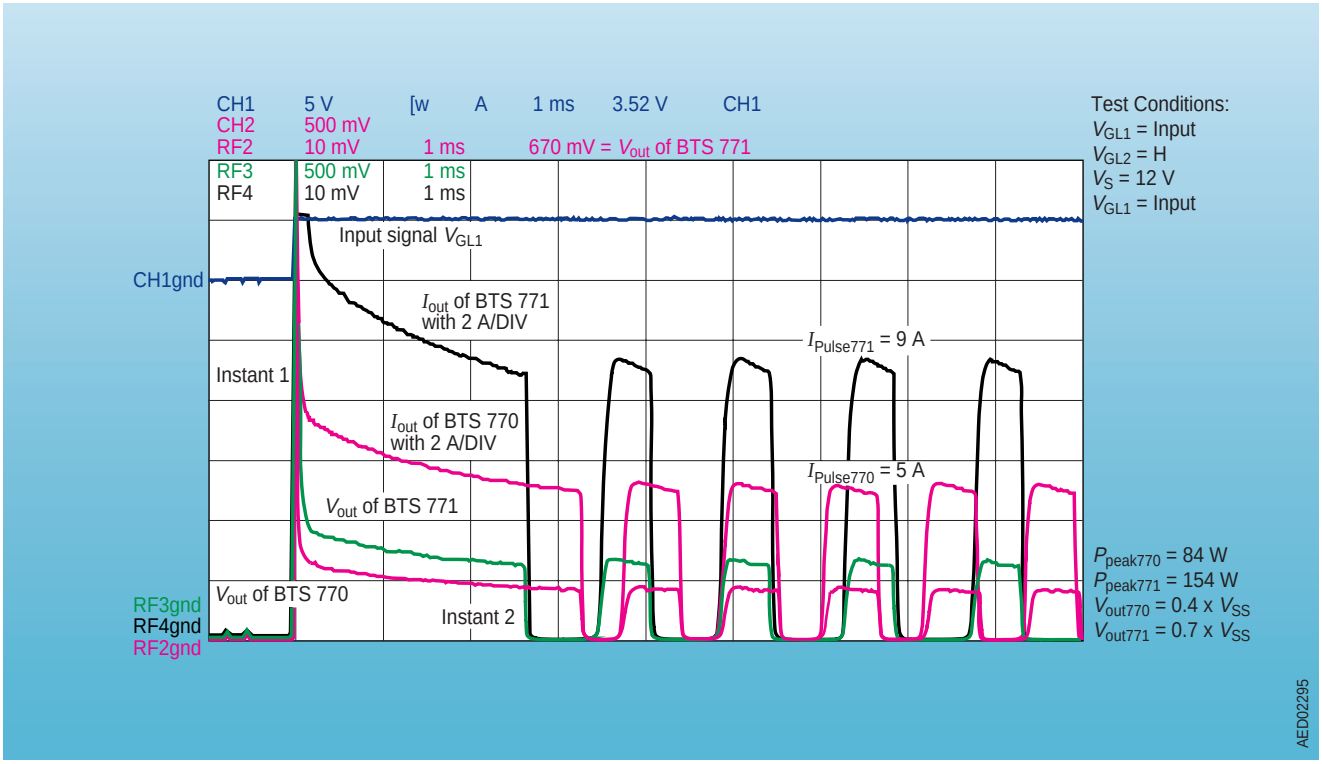

Figure 32
Response of the TrilithIC when Switched on in Response to a Short-Circuited Motor

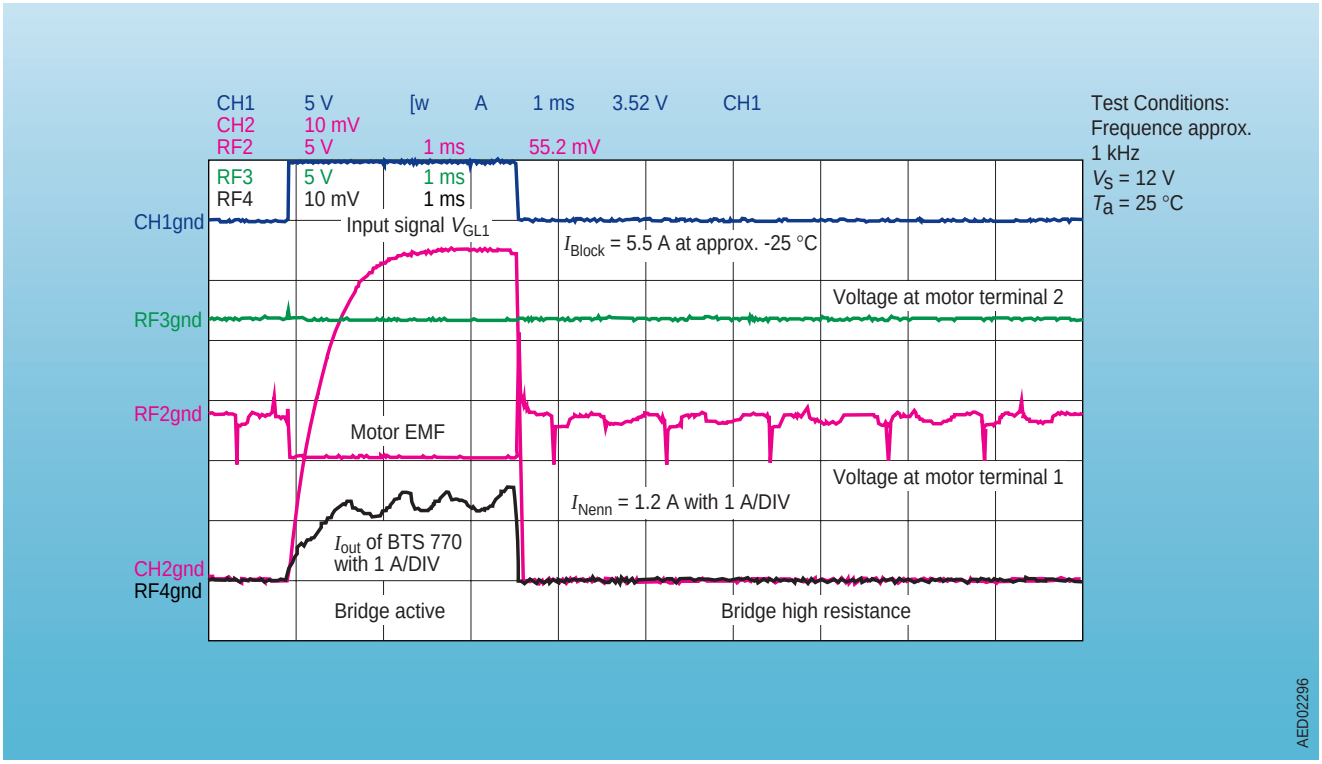

Figure 33
Low-Frequency Motor Current Control with a TrilithIC Using the Low-Side Switch in Switched-Mode

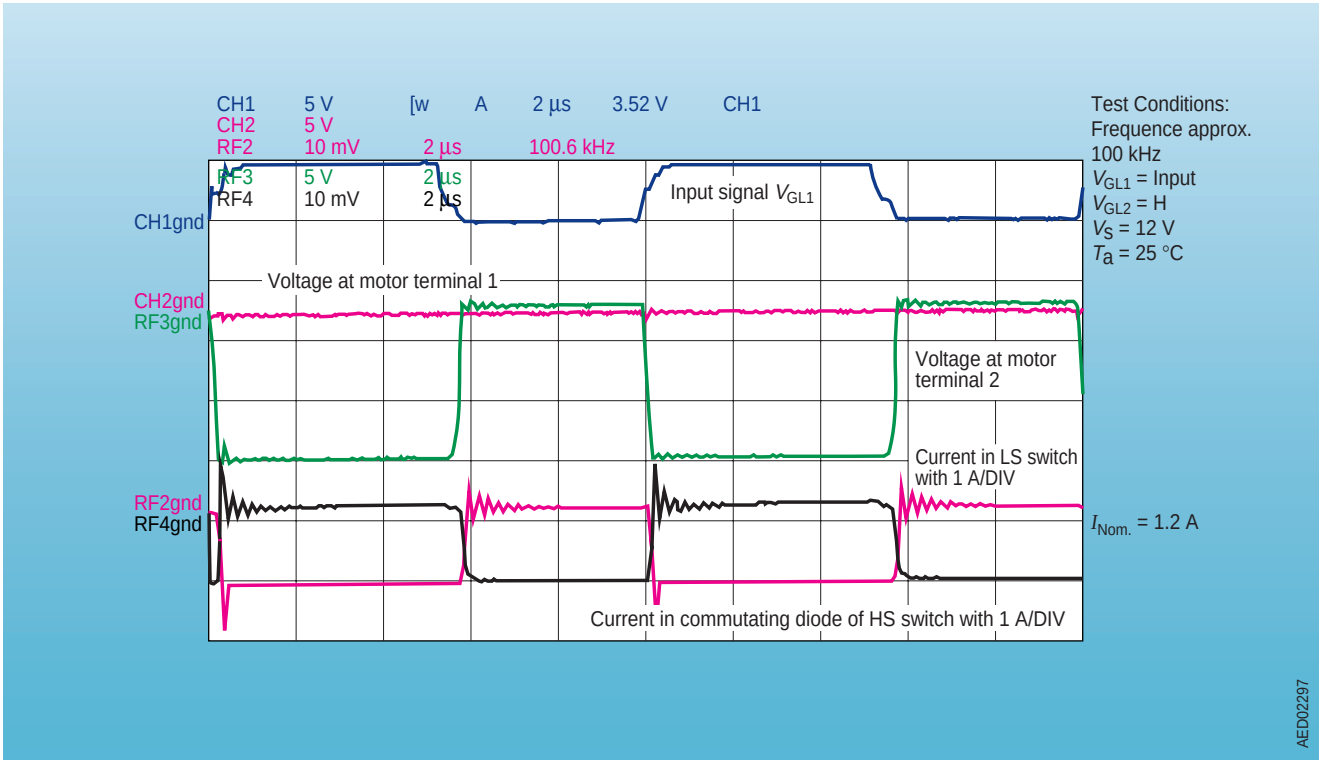

Figure 34
High-Frequency Motor Current Control (sign magnitude) with a TrilithIC Using the Low-Side Switch in Switched-Mode

4 High-Current-Motor Bridge

The BTS 770/1 TrilithICs are limited to applications where relatively small switching performances are required. The reason for this is to be found in the thermal data of the P-DSO-28 package.

As illustrated in **Figure 35**, the automobile offers a host of applications for motor drivers if the output current of the TrilithIC can be increased to approx. 20 to 30 A peak current. The most important applications are likely to be the power window drive (max. 30 A), the sun roof drive (max. 20 A), the power seat drive (max. 30 A) and the windscreen wiper drive (max. 20 A with two-motor drive).

In order to advance into the current class up to 30 A it was first necessary to develop a new package: Starting with the TO220 package with its massive cooling tab, which permits heat to be dissipated vertically from the chip to a heatsink, the developers produced the Power-Package (see **Figure 36**).

This package permits the two low-side chips and the double high-side chip to be mounted in accordance with the TrilithICs. For economical production this pakkage is based on the standard TO220 package.

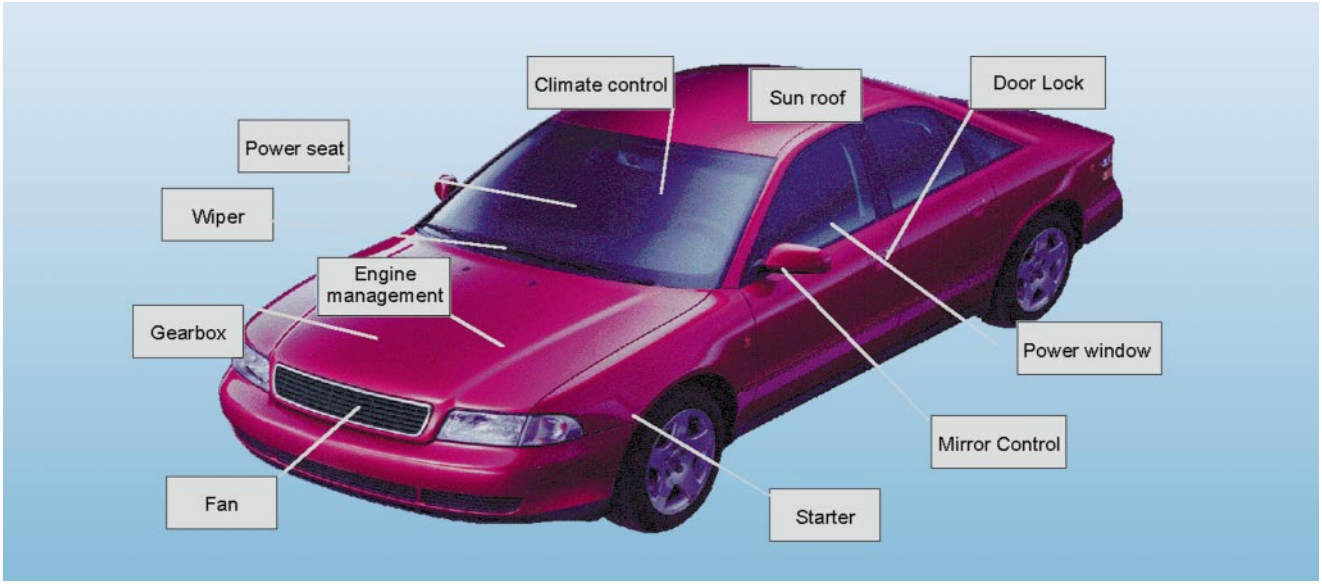

Figure 35
Automotive-Applications for High-Current Motor Bridges

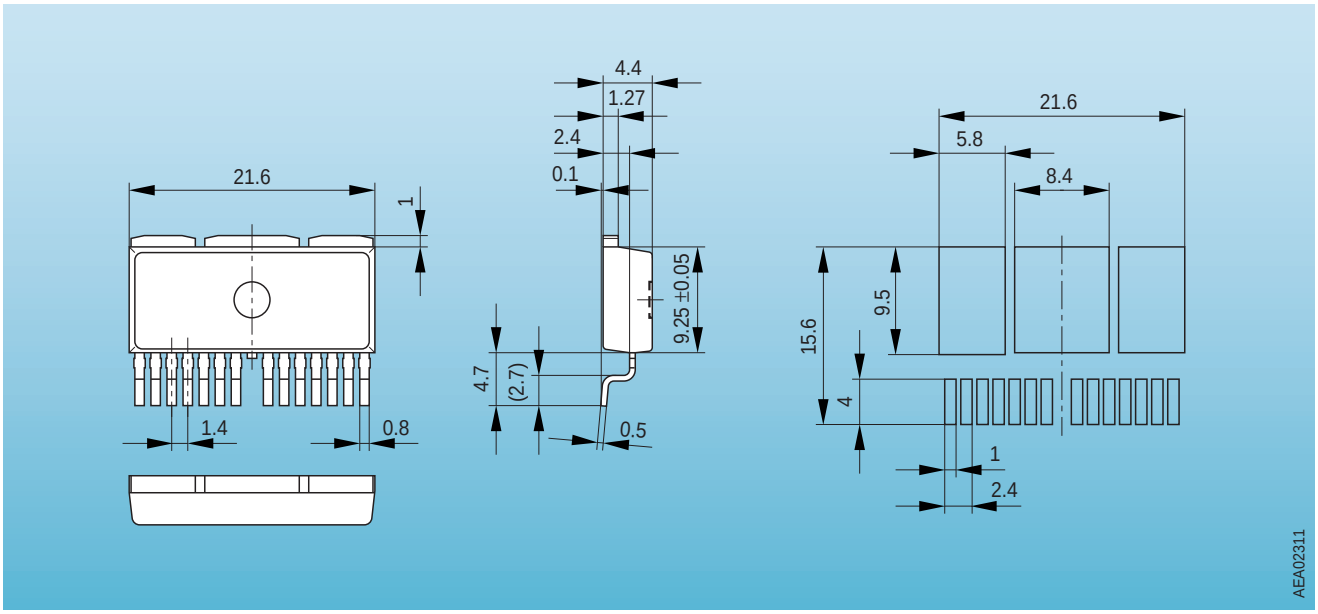

Figure 36
Power-Package and Footprint

Moreover, the latest-generation chip technology has been used:

For the low-side switch, use was made of the brand new S-FET technology. The high-side switches are produced in the “Smart” variant of this technology, i.e. S-Smart technology.

The first high-power TrilithIC is called BTS 780. The most important data and features are illustrated in .

Figure 37 shows an open BTS 780. The high-current bonding wires with 350 µm diameter are clearly recognizable.

Table 2
Main Parameters of BTS 780

Parameter	**Data**
Package	Power Package
Supply voltage functional range	5 V up to 40 V
Very high peak current capability	44 A at T_j = 25 °C; 26 A at T_j = 150 °C
Very low quiescent current	15 µA typ.; 50 µA max.
R_{DSON}-Low-Side-Switch	15 mΩ; 25 °C
R_{DSON}-High-Side-Switch	35 mΩ; 25 °C
Short-Circuit to GND protected	Yes
Overload and Load-Short-Circuit protected	Yes
Overload Diagnosis	Yes
Underload Diagnosis	Yes
Overtemperature Diagnosis	Yes
Short Circuit to + V_S Diagnosis	Yes; in passive state

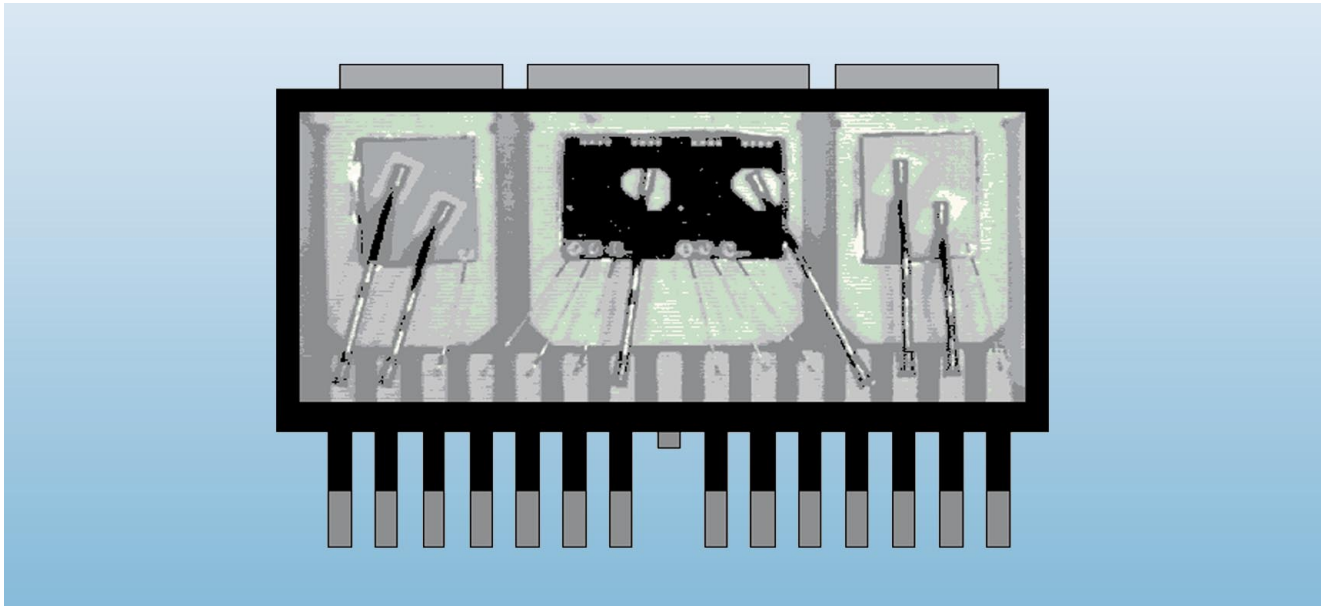

Figure 37
Multi-Chip Construction of BTS 780

An application board as shown in **Figure 38** was assembled together with the BTS 780 as an FEM model. The same board is used for laboratory and application measurements. For small currents (up to approx. 10 A) the BTS 780 can be operated on this board without additional cooling measures. For higher currents, a heatsink, insulated by means of an approx. 300 µm thick polyimide film, can be placed directly under the BTS 780. The FEM simulation of this structure yielded the following results (for model see **Figure 39**).

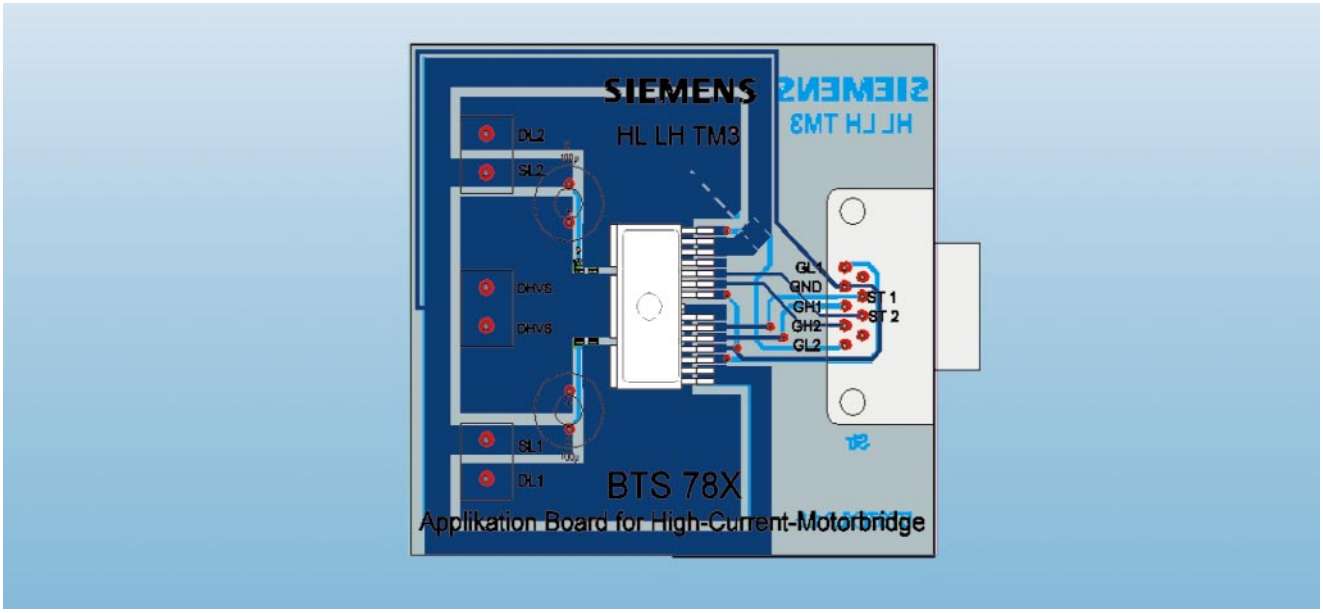

Figure 38
Application Board BTS 780

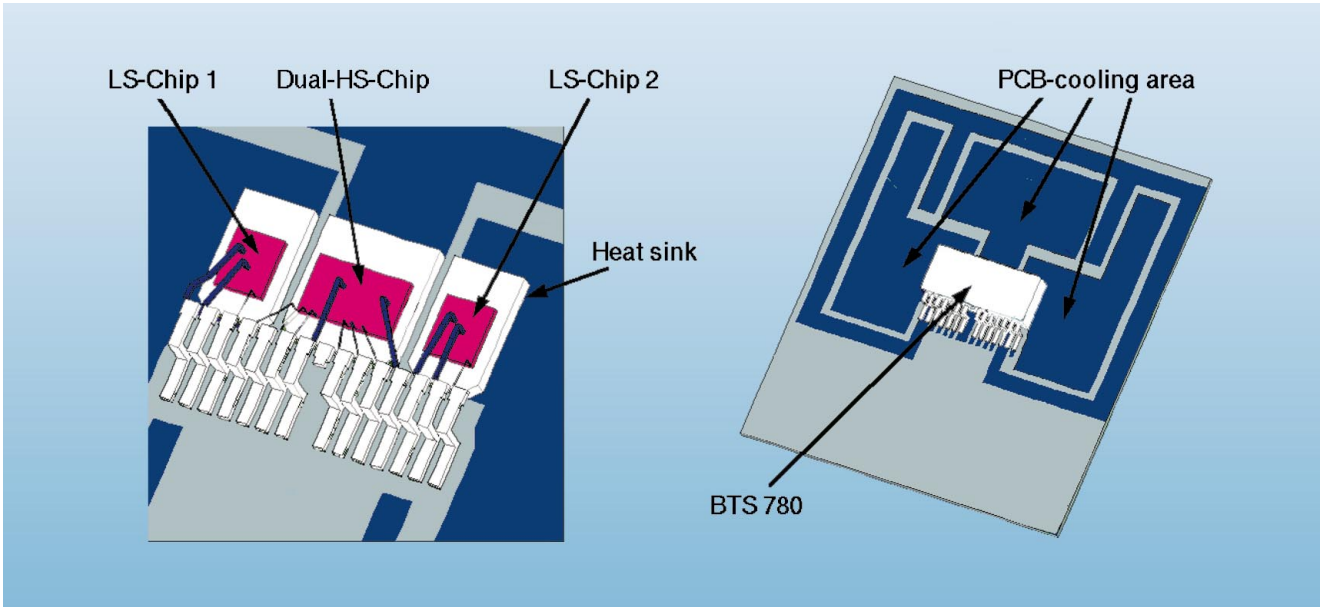

Figure 39
FEM-Model of BTS 780 and Application Board

Figure 40 shows the heat distribution in the BTS 780 at a constant power dissipation of 10 W (corresponds to a current of ~12 A). The thermal resistance to the heatsink is only approx. 4.6 K/W (relative to the hottest point in the system, the active HS switch). The system can cope with considerably higher currents [power] in pulsed mode.

Figure 41 shows the thermal impedances of the system. The value determined for continuous operation, of approx. 4.5 K/W from the chip to the heatsink under the polyimide film, is represented by the green curve (No. 2) at the right-hand edge. The black curve above this (No. 3) indicates the thermal impedance for the application board without additional heatsink. It can be seen that for pulse times up to approx. 1s the Z_{th} values deviate only negligibly from those of the additionally cooled structure.

For the worst-case simulation of an application it was assumed that the device (backside cooled via polyimide film) is under load for 500 ms with a current that results in a dissipation of 20 W (blocked motor at low temperature). At ambient temperature the BTS 780 can deliver approx. 20 A under these conditions.

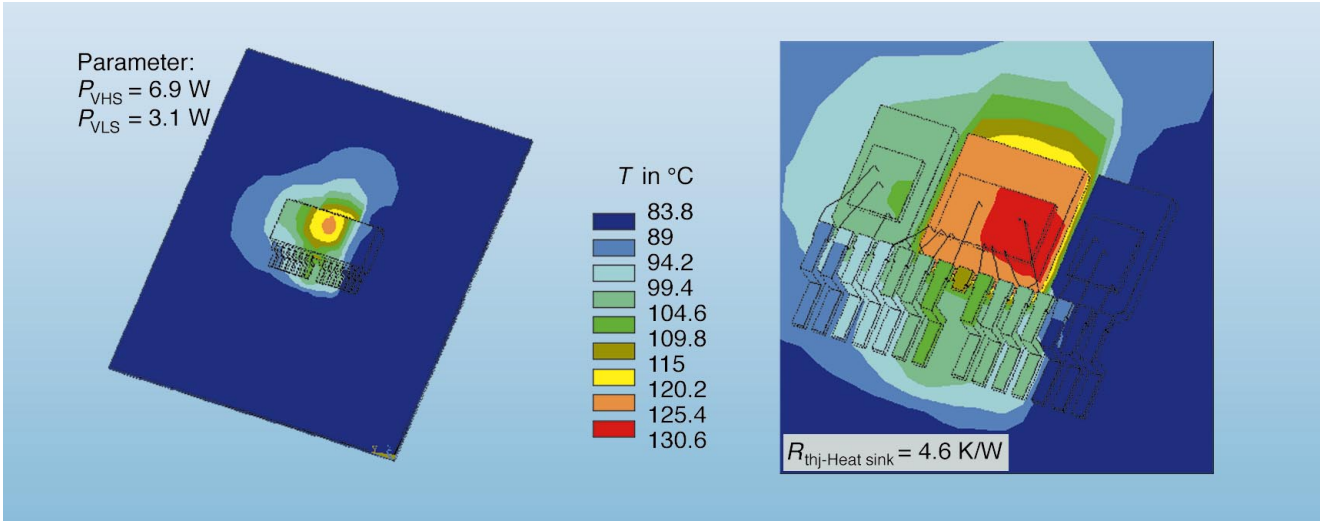

Figure 40
Temperature Distribution for the Case of Cooling via 300 µm Polyimid-Foil and fixed Heatsink of 85 °C

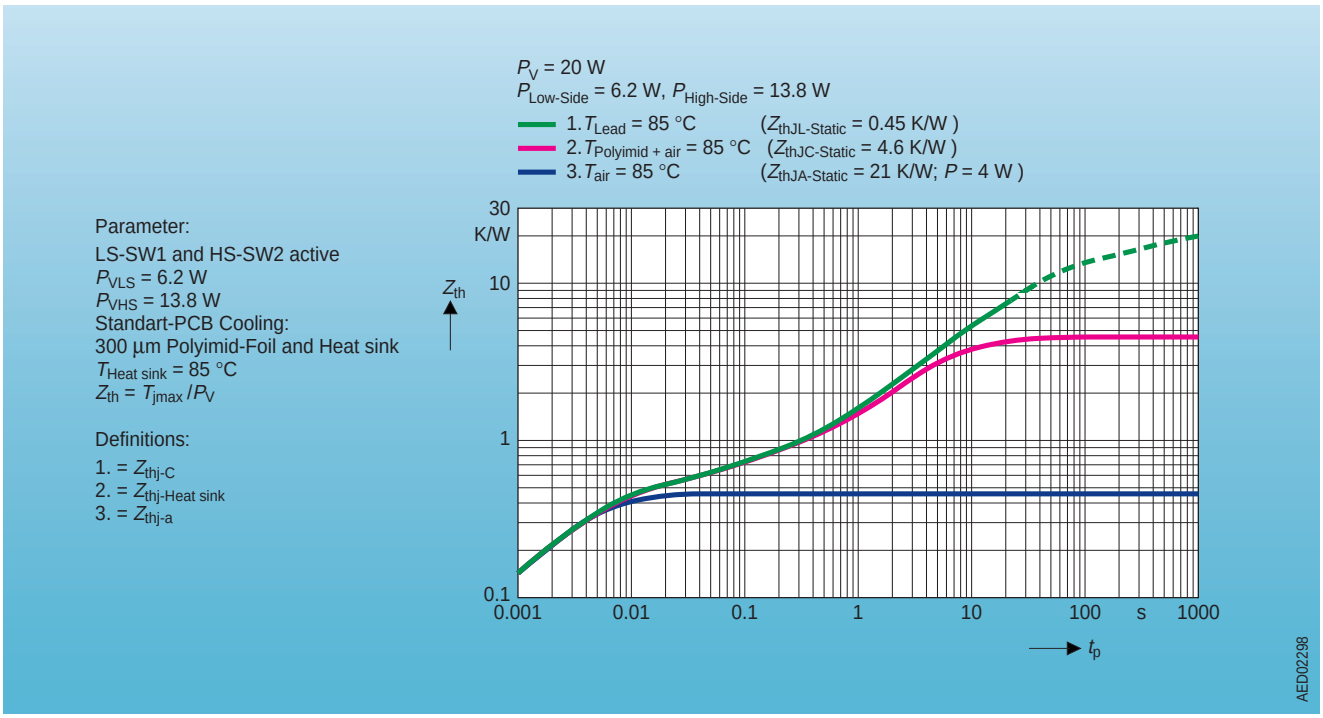

Figure 41
Thermal Impedance of BTS 780

If the BTS 780 is driven at a pulse repetition frequency of 1s (t_{pulse} = t_{pause} = 500 ms), it results in the curve shown in **Figure 42** for the chip temperatures for HS and LS switches over time. Result:

The low Z_{th} (approx. 1.3 K/W for the HS switch and approx. 0.5 K/W for the LS switch) enables repeated switch-ons under worst-case conditions (blocked motor).

For continuous operation, as can also be seen in **Figure 42**, the HS chip with integrated temperature monitoring will regulate the load current with thermal pulse width modulation (cf. **Figure 32**). The low-side switch is not at risk at any time.

Figure 43 shows the startup behavior of a commercially available power window motor. The red curve indicates the current pattern in the motor. The commutation ripple clearly shows how the motor runs up to its rated speed. The startup operation is completed after approx. 50 ms. The current drops to under 10 A.

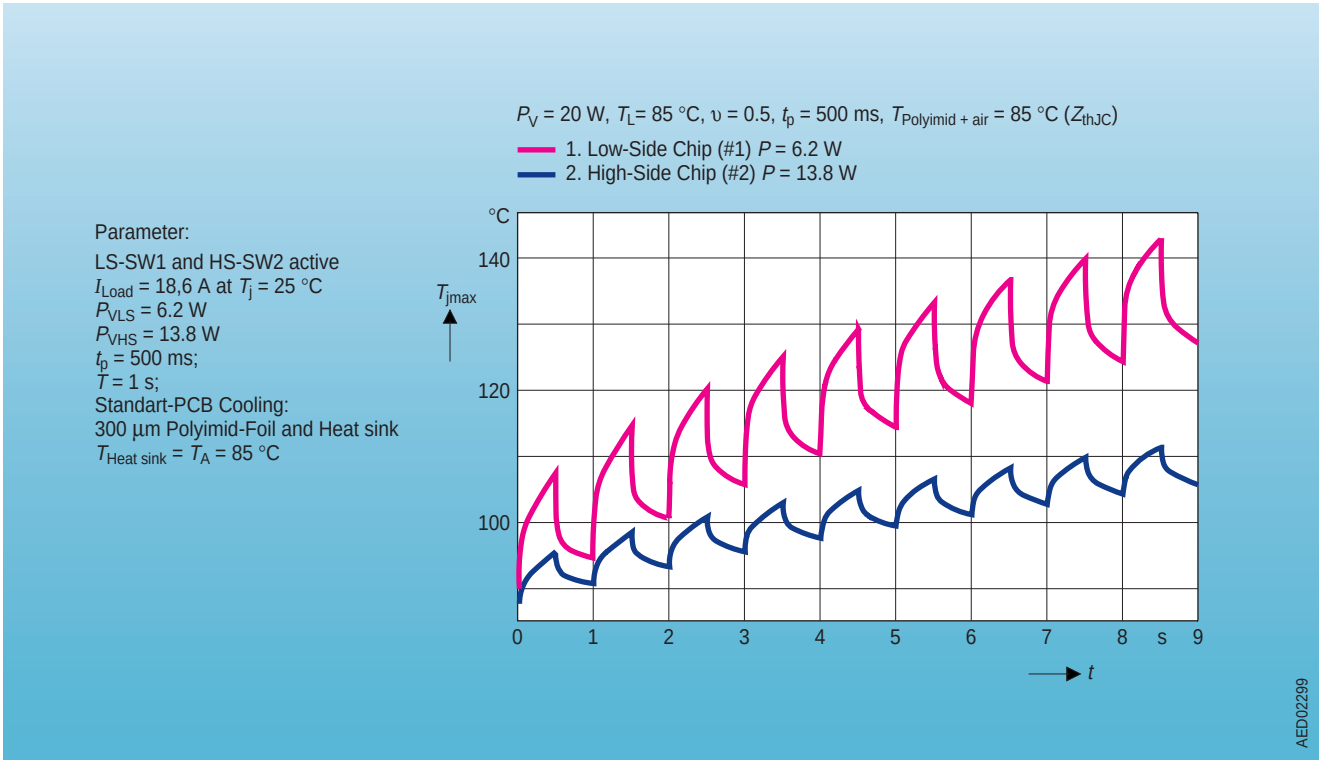

Figure 42
Dynamic Junction Temperature in Full Bridge Operation

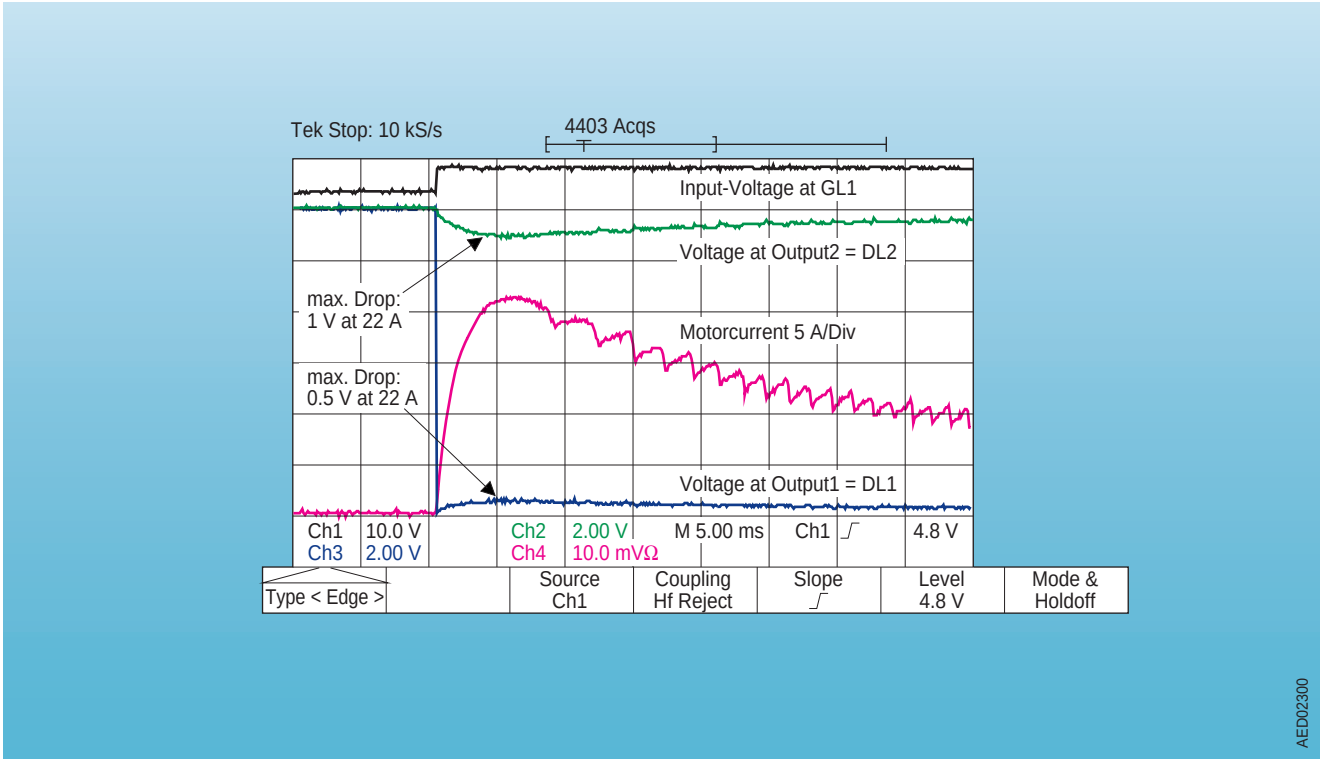

Figure 43
Start of a Power-Window Motor V_s = 12 V

This excellent thermal performance and features such as:

- function from as low as 5 V input voltage; up to max. 40 V
- maximum standby current in OFF state only max. 50 µA
- only 50 mΩ (branch resistance (HS and LS switches together))
- four switches freely configurable
- very high peak currents
- 2-bit diagnosis
- high chop frequency of the low-side switches possible

offer many new opportunities for users.

Many applications currently using electromagnetic relays or discrete transistors can be implemented with just one single SMD device measuring only approx. 22 by 17 mm².

4.1 Further Information

Ordering numbers:

BTS 770	Q67007-A9254
BTS 771	Q67007-A9274
BTS 780	on request

Data sheets are available on the current semiconductor CD-ROM and on the www under **http://www.siemens.de/Semiconductor/products/36/364.htm** or via our sales agencies.