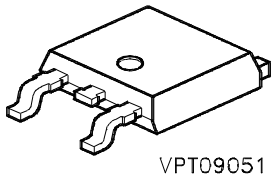
Smart Lowside Power Switch

Features

- Logic Level Input
- Input Protection (ESD)
- Thermal shutdown with auto restart
- Overload protection
- Short circuit protection
- Overvoltage protection
- Current limitation
- Analog driving possible

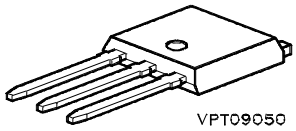
Product Summary

Drain source voltage	V_{DS}	42	V
On-state resistance	$R_{DS(on)}$	50	mΩ
Nominal load current	$I_{D(ISO)}$	3.3	A
Clamping energy	E_{AS}	3	J


VPT09051

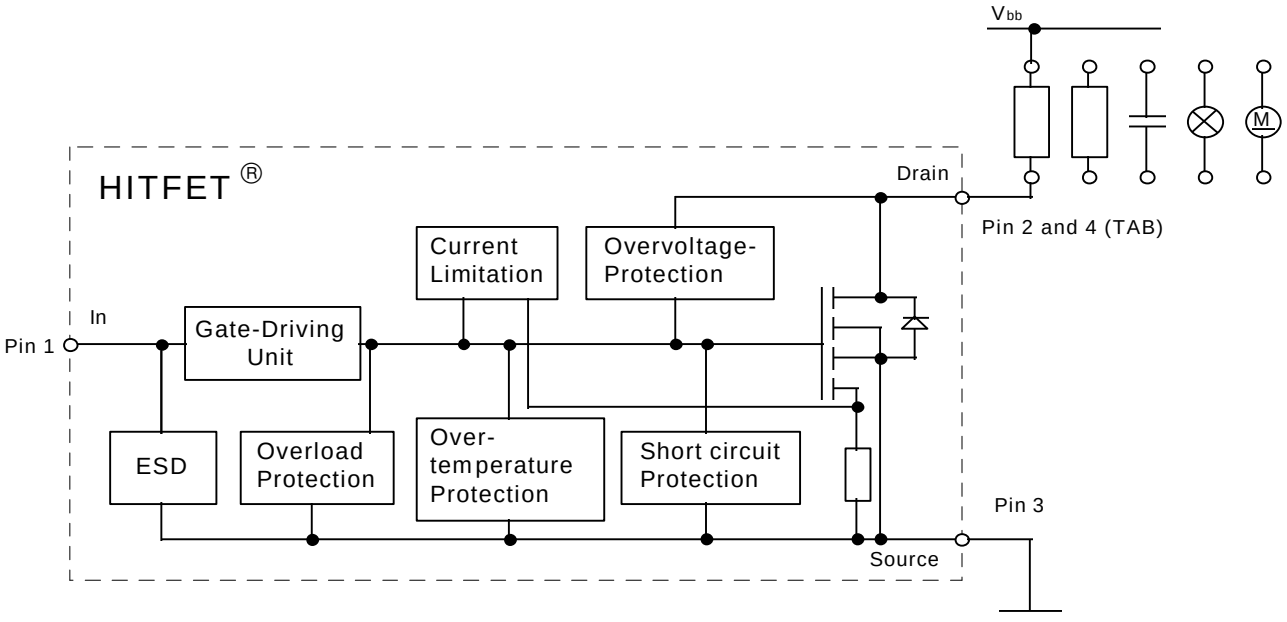
Application

- All kinds of resistive, inductive and capacitive loads in switching or linear applications
- µC compatible power switch for 12 V and 24 V DC applications
- Replaces electromechanical relays and discrete circuits


VPT09050

General Description

N channel vertical power FET in Smart SIPMOS® technology. Fully protected by embedded protection functions.



Maximum Ratings at T_j = 25°C, unless otherwise specified

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	42	V
Drain source voltage for short circuit protection	$V_{DS(SC)}$	42	
Continuous input voltage	V_{IN}	-0.2 ... +10	
Peak input voltage ($I_{IN} \leq 2$ mA)	$V_{IN(peak)}$	-0.2 ... V_{DS}	
Operating temperature	T_j	-40 ...+150	°C
Storage temperature	T_{stg}	-55 ... +150	
Power dissipation T_C = 85 °C 6cm² cooling area , T_A = 85 °C	P_{tot}	 43 1.1	W
Unclamped single pulse inductive energy [1]	E_{AS}	3	J
Load dump protection $V_{LoadDump}$[2] = V_A + V_S V_{IN} = 0 and 10 V, t_d = 400 ms, R_I = 2 Ω, R_L = 4.5 Ω, V_A = 13.5 V	V_{LD}	65	V
Electro**s**tatic **d**ischarge voltage (Human Body Model) according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993	V_{ESD}	2	kV
DIN humidity category, DIN 40 040		E	
IEC climatic category; DIN IEC 68-1		40/150/56	

Thermal resistance

junction - case:	R_{thJC}	1.5	K/W
junction - ambient:			
SMD: junction - ambient @ min. footprint @ 6 cm² cooling area [3]	R_{thJA}	 115 55	

[1] Not tested, specified by design.

[2] $V_{Loaddump}$ is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

[3] Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thick) copper area for drain connection. PCB mounted vertical without blown air.

Electrical Characteristics

Parameter at T_j = 25°C, unless otherwise specified	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics					
Drain source clamp voltage T_j = - 40 ...+ 150, I_D = 10 mA	$V_{DS(AZ)}$	42	-	55	V
Off-state drain current T_j = -40 ... +150°C V_{DS} = 32 V, V_{IN} = 0 V	I_{DSS}	-	1.5	10	µA
Input threshold voltage I_D = 0.7 mA, T_j = 25 °C I_D = 0.7 mA, T_j = 150 °C	$V_{IN(th)}$	 1.3 0.9	 1.7 -	 2.2 -	V
On state input current	$I_{IN(on)}$	-	10	30	µA
On-state resistance I_D = 3 A, V_{IN} = 5 V, T_j = 25 °C I_D = 3 A, V_{IN} = 5 V, T_j = 150 °C	$R_{DS(on)}$	 - -	 45 75	 60 100	mΩ
On-state resistance I_D = 3 A, V_{IN} = 10 V, T_j = 25 °C I_D = 3 A, V_{IN} = 10 V, T_j = 150 °C	$R_{DS(on)}$	 - -	 35 65	 50 90	
Nominal load current V_{IN} = 10 V, T_j < 150°C, T_A = 85 °C, SMD 6 cm² cooling area V_{IN} = 10 V, V_{DS} = 0.5 V, T_C = 85 °C, T_j < 150°C	$I_{D(ISO)}$	 3.3 7.1	 - -	 - -	A
Current limit (active if V_{DS}>2.5 V)[1)] V_{IN} = 10 V, V_{DS} = 12 V, t_m = 200 µs	$I_{D(lim)}$	18	24	30	

[1]Device switched on into existing short circuit (see diagram Determination of $I_{D(lim)}$. Dependant on the application, these values might be exceeded for max. 50 µs in case of short circuit occurs while the device is on condition

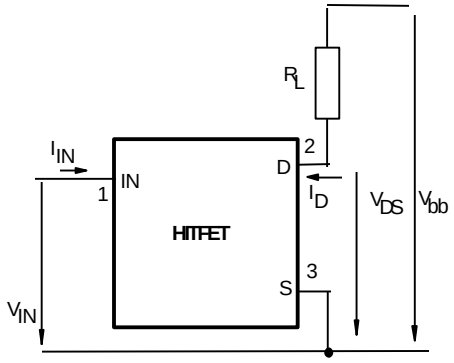
Electrical Characteristics

Parameter at T_j = 25°C, unless otherwise specified	Symbol	Values			Unit
		min.	typ.	max.	
Dynamic Characteristics					
Turn-on time V_{IN} to 90% I_D: R_L = 4.7 Ω, V_{IN} = 0 to 10 V, V_{bb} = 12 V	t_{on}	-	60	150	µs
Turn-off time V_{IN} to 10% I_D: R_L = 4.7 Ω, V_{IN} = 10 to 0 V, V_{bb} = 12 V	t_{off}	-	60	150	
Slew rate on 70 to 50% V_{bb}: R_L = 4.7 Ω, V_{IN} = 0 to 10 V, V_{bb} = 12 V	$-dV_{DS}/dt_{on}$	-	0.3	1	V/µs
Slew rate off 50 to 70% V_{bb}: R_L = 4.7 Ω, V_{IN} = 10 to 0 V, V_{bb} = 12 V	dV_{DS}/dt_{off}	-	0.7	1	
Protection Functions					
Thermal overload trip temperature	T_{jt}	150	165	-	°C
Thermal hysteresis	ΔT_{jt}	-	10	-	K
Input current protection mode	$I_{IN(Prot)}$	-	140	300	µA
Unclamped single pulse inductive energy [1)] I_D = 3 A, T_j = 25 °C, V_{bb} = 12 V	E_{AS}	3	-	-	J
Inverse Diode					
Inverse diode forward voltage I_F = 15 A, t_m = 250 µs, V_{IN} = 0 V, t_P = 300 µs	V_{SD}	-	1.0	-	V

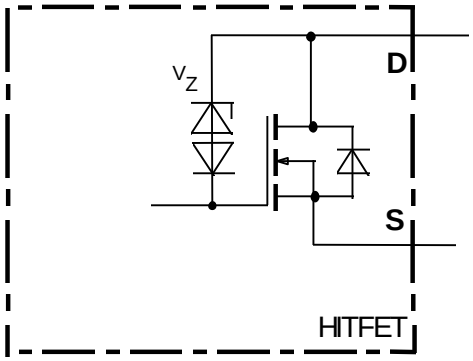
1 Not tested, specified by design.

Block diagram

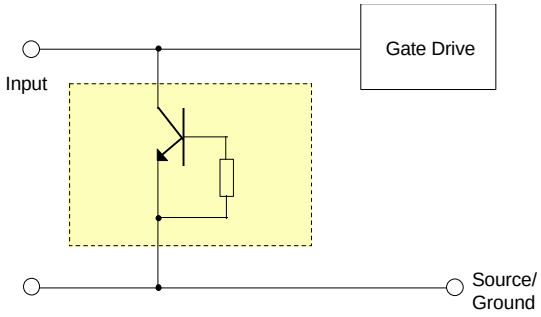
Terms



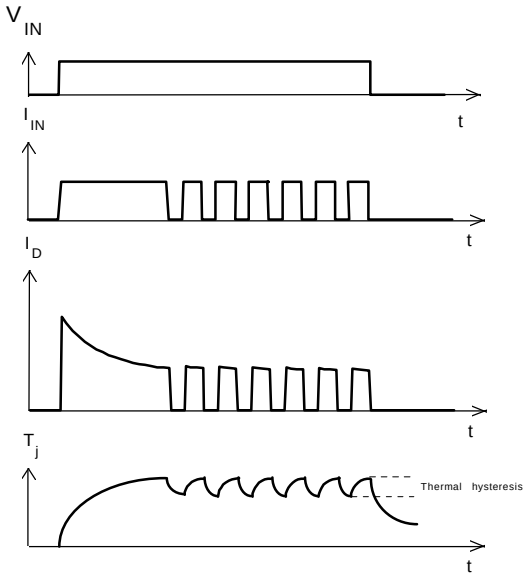
Inductive and overvoltage output clamp



Input circuit (ESD protection)



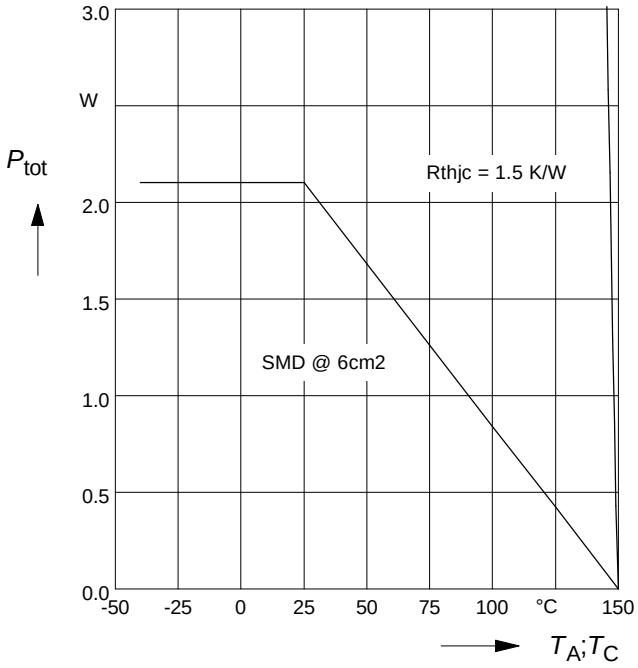
Short circuit behaviour



Maximum allowable power dissipation

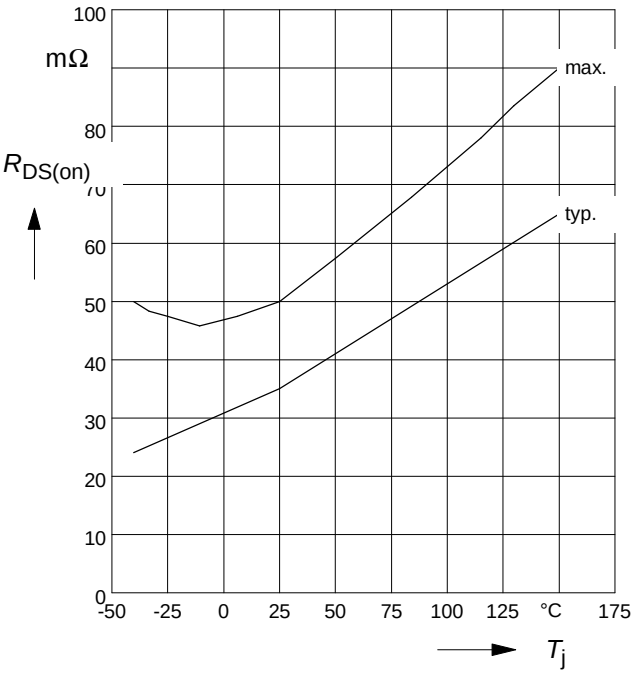
P_{tot} = f(T_C) resp.

P_{tot} = f(T_A) @ R_{thJA}=60 K/W



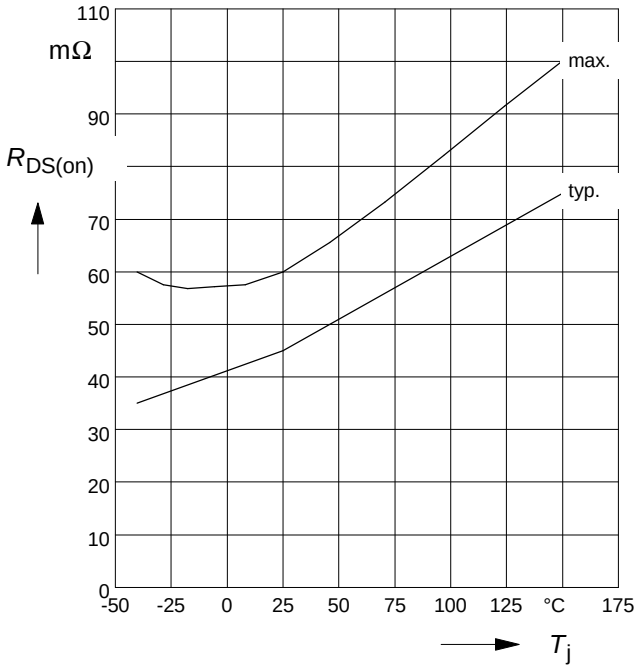
On-state resistance

R_{ON}=f(T_j); I_D=3A; V_{IN}=10V



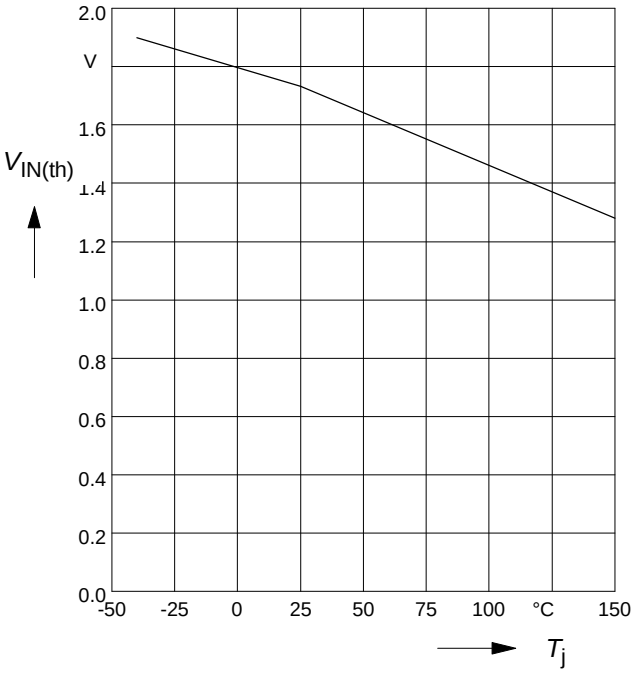
On-state resistance

R_{ON}=f(T_j); I_D=3A; V_{IN}=5V



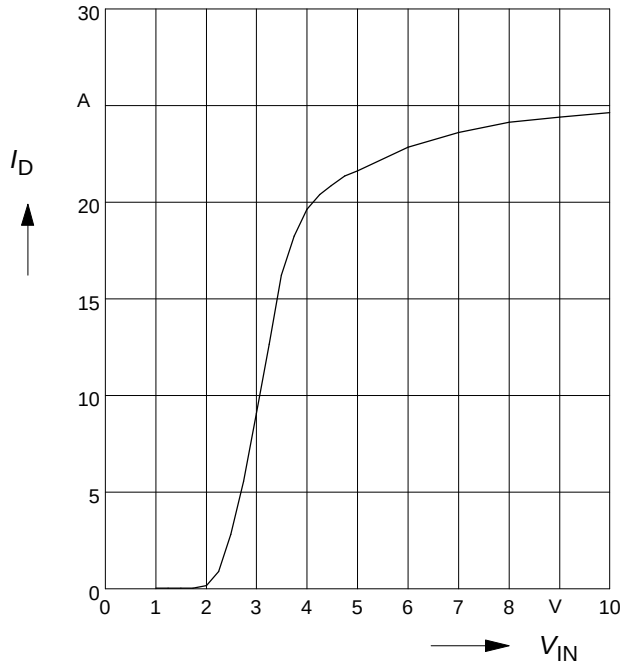
Typ. input threshold voltage

$V_{IN(th)}$ = f(T_j); I_D = 0.7 mA; V_{DS} = 12V



Typ. transfer characteristics

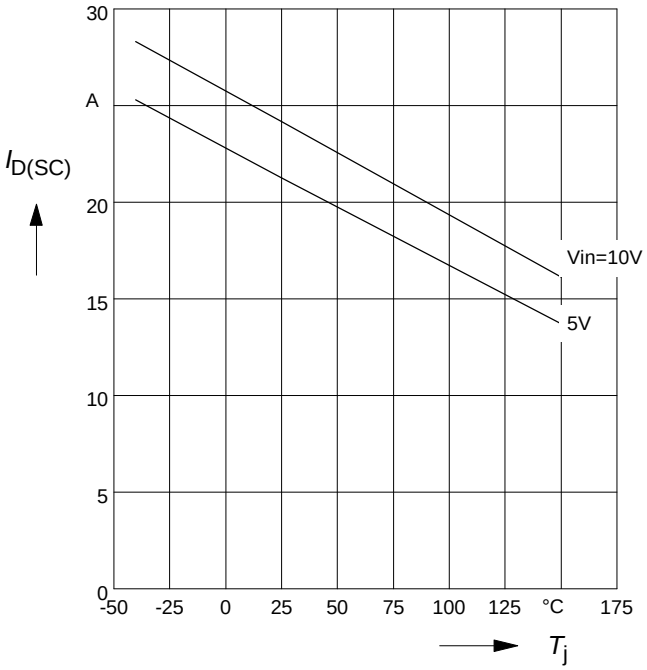
$I_D=f(V_{IN})$; V_{DS}=12V; T_{Jstart}=25°C



Typ. short circuit current

$I_{D(lim)} = f(T_j)$; V_{DS}=12V

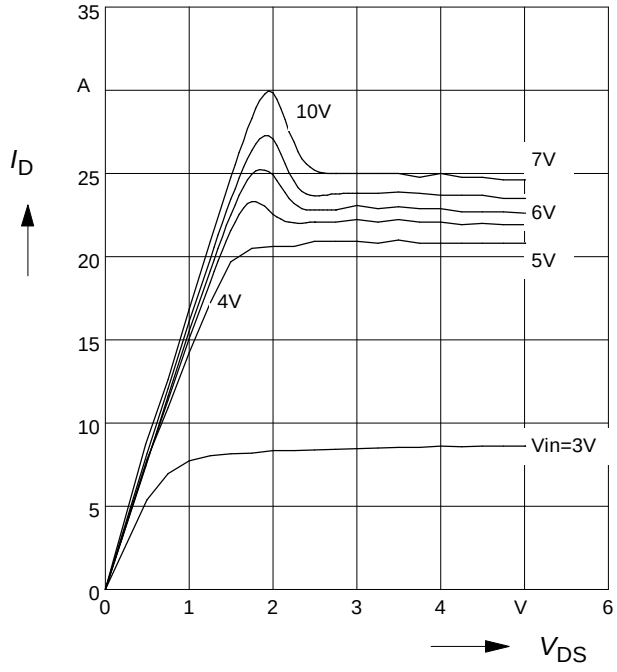
Parameter: V_{IN}



Typ. output characteristics

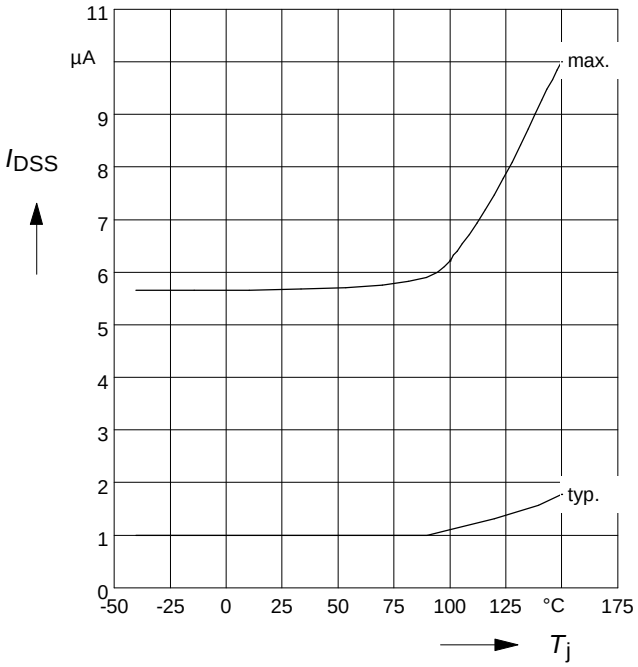
$I_D=f(V_{DS})$; T_{Jstart}=25°C

Parameter: V_{IN}



Typ. off-state drain current

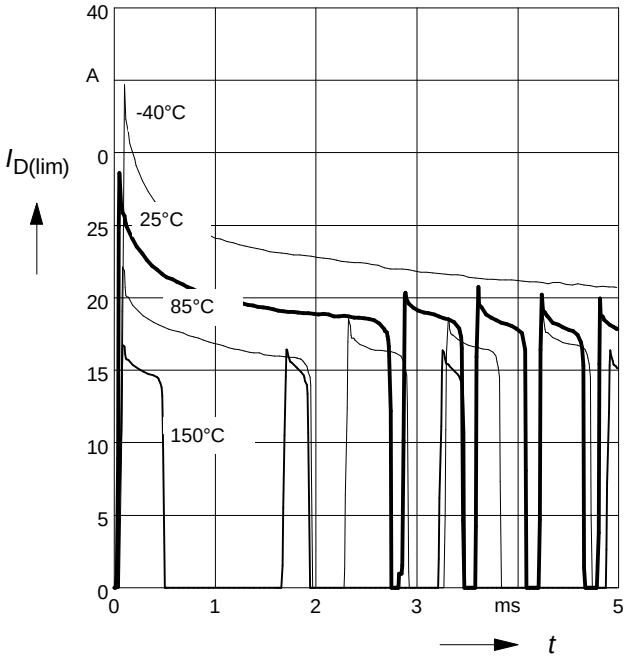
$I_{DSS} = f(T_j)$



Typ. overload current

$I_{D(lim)}$ = f(t), V_{bb}=12 V, no heatsink

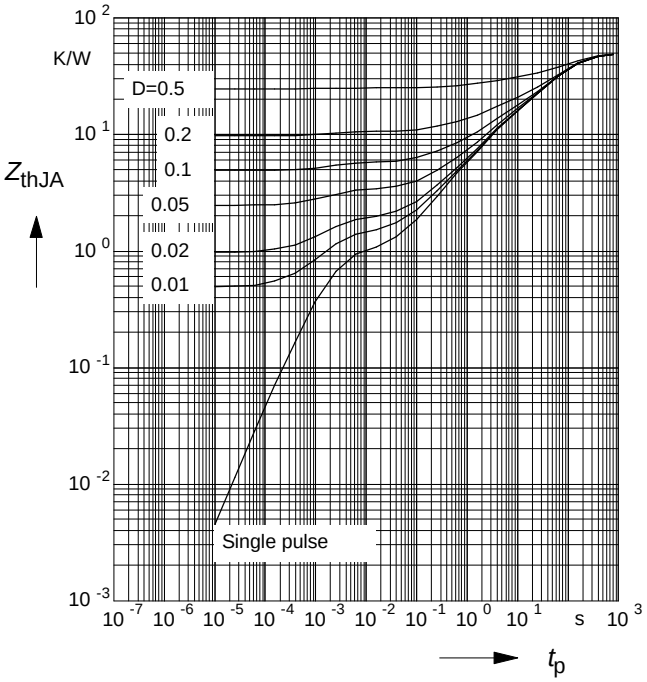
Parameter: T_{jstart}



Typ. transient thermal impedance

Z_{thJC}=f(t_p) @ 6 cm² cooling area

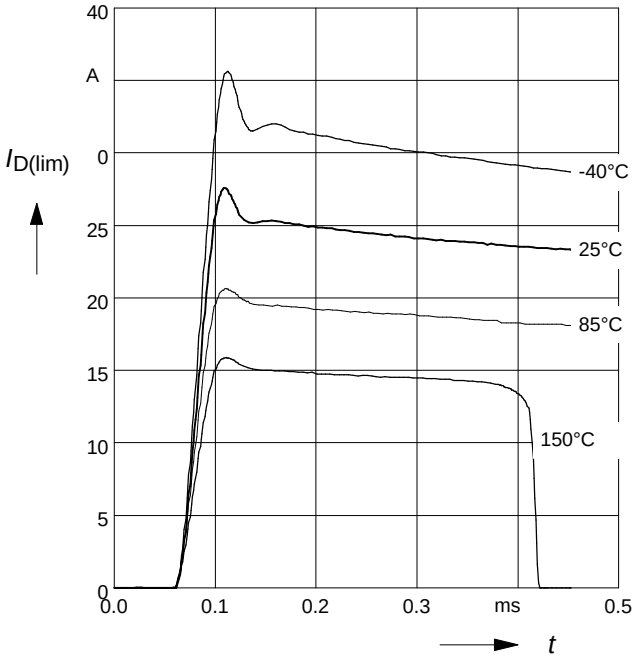
Parameter: $D=t_p/T$



Determination of $I_{D(lim)}$

$I_{D(lim)}$ = f(t); t_m = 200µs

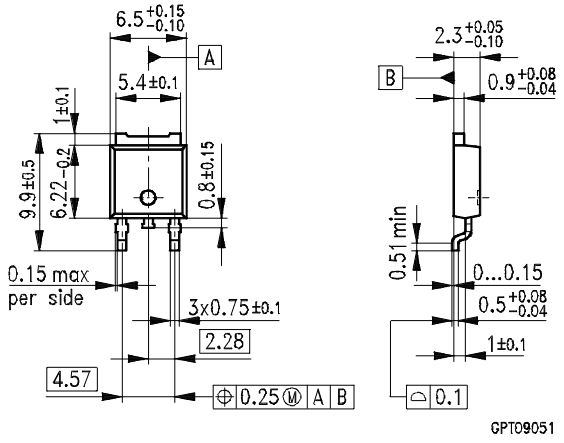
Parameter: T_{Jstart}



Package and ordering code

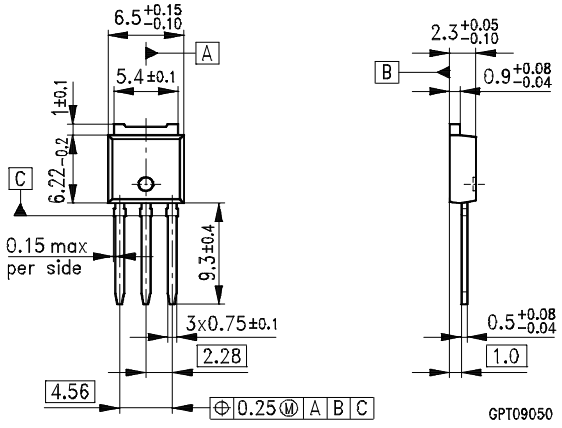
all dimensions in mm

Ordering code: Q67060-S6504-A2



All metal surfaces tin plated, except area of cut.

Ordering code: On request



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