4MEGABIT (512K x 8/ 256K x 16) 5VOLT SECTOR ERASE CMOS FLASH MEMORY

GENERAL DESCRIPTION

The BM29F400 is an 4 Megabit, 5.0 volt-only CMOS Flash memory device organized as a 512 Kbytes of 8-bits each, or 256 Kbytes of 16 bits each. The device is offered in standard 44-pin SOP and 48-pin TSOP packages. It is designed to be programmed and erased in-system with a 5.0 volt power-supply and can also be reprogrammed in standard EPROM programmers.

With access times of 90 nS, 120 nS, and 150 nS, the BM29F400 has separate chip enable $\overline{CE}$, write enable $\overline{WE}$, and output enable $\overline{OE}$ controls. BMI's memory devices reliably store memory data even after 100,000 program and erase cycles.

The BM29F400 is entirely pin and command set compatible with the JEDEC standard for 4 Megabit Flash memory devices. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The BM29F400 is programmed by executing the program command sequence. This will start the internal byte/word programming algorithm that automatically times the program pulse width and also verifies the proper cell margin. Erase is accomplished by executing either the sector erase or chip erase command sequence. This will start the internal erasing algorithm that automatically times the erase pulse width and also verifies the proper cell margin. No preprogramming is required prior to execution of the internal erase algorithm. Sectors of the BM29F400 Flash memory array are electrically erased via Fowler-Nordheim tunneling. Bytes/words are programmed one byte/word at a time using a hot electron injection mechanism.

The BM29F400 features a sector erase architecture. The device memory array is divided into one 16 Kbytes, two 8 Kbytes, one 32 Kbytes, and seven 64 Kbytes. Sectors can be erased individually or in groups without affecting the data in other sectors. Multiple sector erase and full chip erase capabilities add flexibility to altering the data in the device. To protect this data from accidental program and erase, the device also has a sector protect function. This function hardware write protects the selected sector(s). The sector protect and sector unprotect features can be enabled in a PROM programmer.

For read, program and erase operation, the BM29F400 needs a single 5.0 volt power-supply. Internally generated and well regulated voltages are provided for the program and erase operation. A low Vcc detector inhibits write operations on loss of power. End of program or erase is detected by the Ready/Busy status pin, Data Polling of DQ7, or by the Toggle Bit I feature on DQ6. Once the program or erase cycle has been successfully completed, the device internally resets to the Read mode.

The BM29F400 also has a hardware $\overline{RESET}$ pin. Driving the $\overline{RESET}$ pin low during execution of an Internal Programming or Erase command will terminate the operation and reset the device to the Read mode. The $\overline{RESET}$ pin may be tied to the system reset circuitry, so that the system will have access to boot code upon completion of system reset, even if the Flash device is in the process of an Internal Programming or Erase operation. If the device is reset using the $\overline{RESET}$ pin during an Internal Programming or Erase operation, data in the address locations on which the internal state

machine is operating will be erroneous. Thus, these address locations will need rewriting after the device is reset.

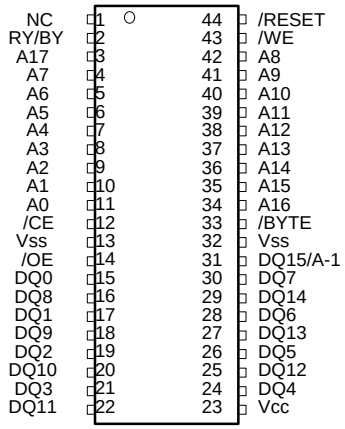
FEATURES

- 5.0 V +/- 10% Program and Erase
  - Minimizes system-level power requirements High performance
  - 90 nS access time
- Compatible with JEDEC-standard Commands
  - Uses software commands, pinouts, and packages following industry standards for single power supply Flash memory
- Typically 100,000 Program/Erase Cycles
- Sector Erase Architecture
  - One 16 Kbytes, two 8 Kbytes, one 32 Kbytes, and seven 64 Kbytes
  - Any combination of sectors can be erased concurrently; also supports full chip erase
- Erase Suspend/Resume
  - Suspend a sector erase operation to allow a data read in a sector not being erased within the same device
- Ready/Busy
  - RY/BY output pin for detection of programming or erase cycle completion
- $\overline{\text{RESET}}$
  - Hardware pin resets the internal state machine to the read mode
- Internal Erase Algorithms
  - Automatically erases a sector, any combination of sectors, or the entire chip
- Internal Programming Algorithms
  - Automatically programs and verifies data at a specified address
- Low Power Consumption
  - 20 mA typical active read current for Byte Mode
  - 28 mA typical active read current for Word Mode
  - 30 mA typical write/erase current
- Sector Protection
  - Hardware method disables any combination of sectors from a program or erase operation
- Boot Code Sector Architecture

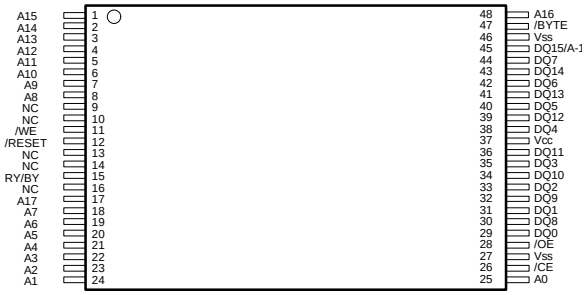
FAMILY PART NO.	-90	-120	-150
Maximum Access Time (nS)	90	120	150
$\overline{\text{CE}}$ (E) Access time (nS)	90	120	150
$\overline{\text{OE}}$ (G) Access time (nS)	35	50	60

*This speed is available with Vcc = 5V +/- 5% variation

PIN CONFIGURATIONS



PSOP

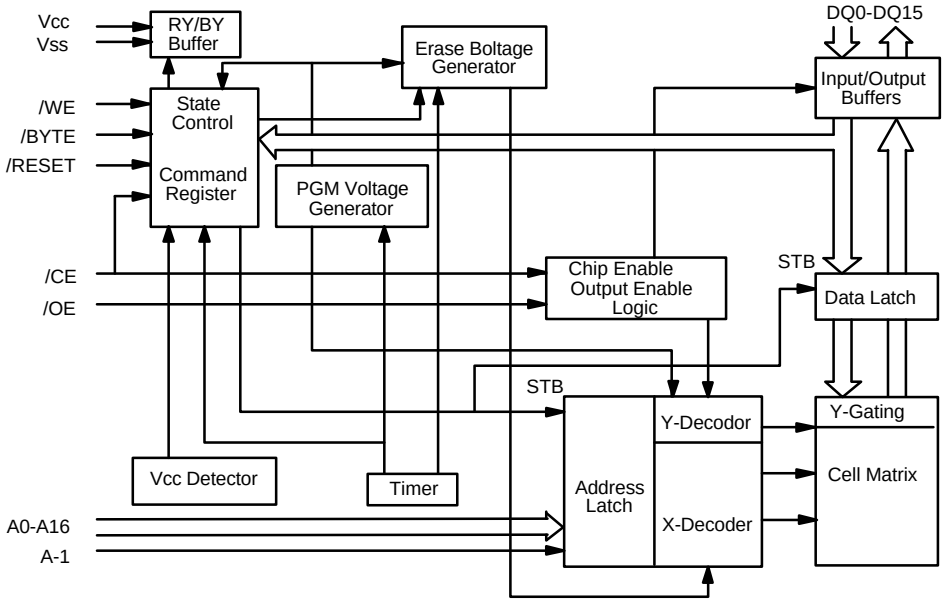


Standard TSOP

PIN DESCRIPTION

A0 - A17	Address Inputs
DQ0 - DQ14	Data Input/Output
DQ15 /A-1	Data Input/Output, Address Mux.
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vss	Device Ground
$\overline{RESET}$	Hardware $\overline{RESET}$ Pin, Active Low
RY/BY	Ready/Busy Status Output
Vcc	Device Power Supply
$\overline{BYTE}$	Selects 8-bit or 16-bit Mode
NC	Not Internally Connected

BLOCK DIAGRAM



BUS OPERATION

Table 1. Bus Operations ($\overline{BYTE}$ = V_{IH})(1)

OPERATION	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	DQ0-DQ15	$\overline{RESET}$
Electronic ID Manufacturer(2)	L	L	H	L	L	L	V_{ID}	Code	H
Electronic ID Device(2)	L	L	H	H	L	L	V_{ID}	Code	H
Read(3)	L	L	H	A0	A1	A6	A9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	High Z	H
Hardware Reset	X	X	X	X	X	X	X	High Z	L
Output Disable	L	H	H	X	X	X	X	High Z	X
Write	L	H	L	A0	A1	A6	A9	D_{IN}(4)	H
Verify Sector Protect(2)	L	L	H	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotect	X	X	X	X	X	X	X	X	V_{ID}

Notes:
1. L = V_{IL}, H = V_{IH}, X = Don't Care. See DC Characteristics for voltage levels.
2. Manufacturer and device codes may also be accessed via a command register sequence. Refer to Table 6.
3. $\overline{WE}$ can be V_{IL} if $\overline{CE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
4. Refer to Table 6 for valid D_{IN} during a write operation.

Table 2. Bus Operations ($\overline{BYTE}$ = V_{IL})(1)

OPERATION	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	DQ0-DQ7	DQ8-DQ15	$\overline{RESET}$
Electronic ID Manufacturer(2)	L	L	H	L	L	L	V_{ID}	Code	High Z	H
Electronic ID Device(2)	L	L	H	H	L	L	V_{ID}	Code	High Z	H
Read(3)	L	L	H	A0	A1	A6	A9	D_{OUT}	High Z	H
Standby	H	X	X	X	X	X	X	High Z	High Z	H
Hardware Reset	X	X	X	X	X	X	X	High Z	High Z	L
Output Disable	L	H	H	X	X	X	X	High Z	High Z	H
Write	L	H	L	A0	A1	A6	A9	D_{IN}(4)	High Z	H
Verify Sector Protect(2)	L	L	H	L	H	L	V_{ID}	Code	High Z	H
Temporary Sector Unprotect	X	X	X	X	X	X	X	X	High Z	V_{ID}

Notes:
1. L = V_{IL}, H = V_{IH}, X = Don't Care. See DC Characteristics for voltage levels.
2. Manufacturer and device codes may also be accessed via a command register sequence. Refer to Table 6.
3. $\overline{WE}$ can be V_{IL} if $\overline{CE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
4. Refer to Table 6 for valid D_{IN} during a write operation.

Table 3. Sector Protection Verify Electronic ID Codes

TYPE			A17-A12	A6	A1	A0	Code (Hex)
Manufacturer Code			X	V_{IL}	V_{IL}	V_{IL}	ADH
29F400	29F400T	Byte	X	V_{IL}	V_{IL}	V_{IH}	23H
		Word					22,23H
	29F400B	Byte	X	V_{IL}	V_{IL}	V_{IH}	ABH
		Word					22 ABH
Sector Protection			Sector Address	V_{IL}	V_{IH}	V_{IL}	01H(1)

Note: Outputs 01H at protected sector addresses, and outputs 00H at unprotected addresses.

Table 4. Sector Address Tables (BM29F400T)

	A17	A16	A15	A14	A13	A12	(x8) Address Range	(x16) Address Range
SA0	0	0	0	X	X	X	00000H-0FFFFH	00000H-07FFFH
SA1	0	0	1	X	X	X	10000H-1FFFFH	08000H-0FFFFH
SA2	0	1	0	X	X	X	20000H-2FFFFH	10000H-17FFFH
SA3	0	1	1	X	X	X	30000H-3FFFFH	18000H-1FFFFH
SA4	1	0	0	X	X	X	40000H-4FFFFH	20000H-27FFFH
SA5	1	0	1	X	X	X	50000H-5FFFFH	28000H-2FFFFH
SA6	1	1	0	X	X	X	60000H-6FFFFH	30000H-37FFFH
SA7	1	1	1	0	X	X	70000H-77FFFH	38000H-3BFFFH
SA8	1	1	1	1	0	0	78000H-79FFFH	3C000H-3CFFFH
SA9	1	1	1	1	0	1	7A000H-7BFFFH	3D000H-3DFFFH
SA10	1	1	1	1	1	X	7C000H-7FFFFH	3E000H-3FFFFH

Notes:

1. The address range is A17:A-1 if in byte mode ($\overline{BYTE}$ = V_{IL}).

2. The address range is A17:A0, if in word mode ($\overline{BYTE}$ = V_{IH}).

Table 5. Sector Address Tables (BM29F400B)

	A17	A16	A15	A14	A13	A12	(x8) Address Range	x16) Address Range
SA0	0	0	0	0	0	X	00000H-03FFFH	00000H-01FFFH
SA1	0	0	0	0	1	0	04000H-05FFFH	02000H-02FFFH
SA2	0	0	0	0	1	1	06000H-07FFFH	03000H-03FFFH
SA3	0	0	0	1	X	X	08000H-0FFFFH	04000H-07FFFH
SA4	0	0	1	X	X	X	10000H-1FFFFH	08000H-0FFFFH
SA5	0	1	0	X	X	X	20000H-2FFFFH	10000H-17FFFH
SA6	0	1	1	X	X	X	30000H-3FFFFH	18000H-1FFFFH
SA7	1	0	0	X	X	X	40000H-4FFFFH	20000H-27FFFH
SA8	1	0	1	X	X	X	50000H-5FFFFH	28000H-2FFFFH
SA9	1	1	0	X	X	X	60000H-6FFFFH	30000H-37FFFH
SA10	1	1	1	X	X	X	70000H-7FFFFH	38000H-3FFFFH

Notes:

1. The address range is A17:A-1 if in byte mode ($\overline{BYTE}$ = V_{IL}).

2. The address range is A17:A0, if in word mode ($\overline{BYTE}$ = V_{IH}).

Electronic ID Mode

The Electronic ID mode allows the reading out of a binary code from the device and will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5V to 12.5V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don't cares except A0, A1, and A6 (see Table 3).

Manufacturer and device codes may also be read via the command register; for instance, when the BM29F400 is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 6 (refer to Electronic ID Command section).

Byte 0 (A0 = V_{IL}) represents the manufacturer's code (Bright Microelectronics = ADH) and byte 1 (A0 = V_{IH}) the device identifier code (BM29F400T = 23H and BM29F400B = ABH for 8-bit mode; BM29F400T = 2223H and BM29F400B = 22ABH for 16-bit mode). These two byte words are given in Table 3. To read the proper device codes when executing the Electronic ID, all identifiers for manufacturer and device will exhibit odd parity with the MSB (DQ7) defined as the parity bit. A1 must be V_{IL} (see Table 3).

Read Mode

The BM29F400 has three control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected. As shown in Table 1, $\overline{WE}$ should be held at V_{IH}, except in Write mode and Enable Sector Protect mode.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. Chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. Output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}-t_{OE} time).

Standby Mode and Hardware $\overline{RESET}$ Standby Mode

The BM29F400 has two methods for implementing standby mode. The first method requires use of both the $\overline{CE}$ pin and the $\overline{RESET}$ pin. The second method only requires use of the $\overline{RESET}$ pin.

When using both pins, a CMOS standby mode is achieved when both $\overline{CE}$ and $\overline{RESET}$ are held at Vcc ±0.5V. In this condition, the current consumed is typically less than 100 uA. A TTL standby mode is achieved with both $\overline{CE}$ and $\overline{RESET}$ held at V_{IH}. In this condition, the typical current required is reduced to 200 uA. The device can be read with standard access time (t_{CE}) from either of these two standby modes.

When using the $\overline{RESET}$ pin only, a CMOS standby mode is achieved with $\overline{RESET}$ held at Vss ±0.5V. In this condition, the current consumed is typically less than 100 uA. A TTL standby mode is achieved with $\overline{RESET}$ held at V_{IL}. In this condition, the typical current required is reduced to 1mA. Once the $\overline{RESET}$ pin is taken high, the device requires 500 nS of wake-up time before outputs are valid for a read access.

If the device is deselected during programming or erase, the device will draw active current until the programming or erase operation is completed. In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable Mode

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state. It is shown in Table 1 that $\overline{CE}$ = V_{IL} and $\overline{WE}$ = V_{IH} for Output Disable. This is to differentiate Output Disable mode from Write mode and to prevent inadvertent writes during Output Disable.

Program and Erase Modes

Device programming and erase are accomplished via the command register. Contents of the register serve as inputs to the internal state machine. Outputs of the state machine dictate the function of the device.

The command register itself does not occupy any addressable memory locations. The register is a latch used to store the commands along with the addresses and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later, while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used. Refer to AC Characteristics for Programming/Erase and their respective Timing Waveforms for specific timing parameters.

Enable Sector Protect and Verify Sector Protect Modes

The BM29F400 has a hardware Sector Protect mode that disables both Programming and Erase operation to the protected sector(s). There are total of 11 sectors in this device. The sector protect feature is enabled using the programming equipment at the user's site. The device is shipped from the BMI factory with all sectors unprotected.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on the address pin A9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. As shown in Table 2, scanning the sector addresses while (A6, A1 and A0) = (0, 1, 0) will produce a 01H code at the device output pins for a protected sector. In the Verify Sector Protect mode, the device will read 00H for an unprotected sector. In this mode, the lower order addresses, except for A0, A1 and A6, are don't care. Address locations with A1 = V_{IL} are reserved for Electronic ID manufacturer and device codes. It is also possible to determine if a sector is protected in-system by writing the Electronic ID command (described in the Electronic ID command section below.)

Temporary Sector Unprotect Mode

The BM29F400 has a Temporary Sector Unprotect feature that allows the protect feature to be temporarily suspended to change data in a protected sector in-system. The Temporary Sector Unprotect mode is activated by setting the $\overline{RESET}$ pin to V_{ID} (11.5V - 12.5V).

In this mode, protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the $\overline{RESET}$ pin, all previously protected sectors will be protected. Refer to the Temporary Sector Unprotect algorithm and timing waveforms.

Read $\overline{\text{RESET}}$ Command

The read or $\overline{\text{RESET}}$ operation is initiated by writing the Read/Reset command sequence in to the command register. Microprocessor read cycles retrieve the data from the memory. The device remains enable for reads until the command register contents are changed.

The device will automatically power-up in the Read/Reset mode. In this case, a command sequence is not needed to read the memory data. This default power-up to Read mode ensures that no spurious changes of the data can take place during the power transitions. Refer to the AC Characteristics for Read-Only Operation and the respective Timing Waveforms for the specific timing parameters.

Electronic ID Command

The BM29F400 contains an Electronic ID command to supplement the traditional PROM programming method described in the Electronic ID Mode section. The operation is initiated by writing the Electronic ID command sequence into the command register. Following command write, a read cycle from address XX00H retrieves manufacturer code of ADH. A read cycle from address XX01H returns the device code (BM29F400T = 23H and BM29F400B = ABH for 8-bit mode; BM29F400T = 2223H and BM29F400B = 22ABH for 16-bit mode) (see Table 3). All manufacturer and device codes exhibit odd parity with the MSB (DQ7) defined as the parity bit.

The Electronic ID command can also be used to identify protected sectors. After writing the Electronic ID command sequence, the CPU can scan the sector addresses (see Table 4 and Table 5) while (A6, A1, A0) = (0, 1, 0). Protected sectors will return 01H on the data outputs and unprotected sectors will return 00H. To terminate the operation, it is necessary to write the Read/Reset command sequence into the command register.

Byte/Word Programming Command

The device is programmed on a byte-by-byte (or word-by-word) basis. Programming is a four bus cycle operation (see Table 6). There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens later, and program data (PD) is latched on the rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first. The rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first, begins programming using the Embedded Program Algorithm.

Upon executing the algorithm, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 (also used as $\overline{\text{Data}}$ Polling) is equivalent to the data written to this bit at which time the device returns to the read mode and addresses are no longer latched (see Table 7, Write Operation Status Flags). Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time for $\overline{\text{Data}}$ Polling operations. $\overline{\text{Data}}$ Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during the Internal Program Algorithm will be ignored. If a hardware $\overline{\text{RESET}}$ occurs during the programming operation, the data at that particular location will be corrupted.

Byte/Word programming is allowed in any sequence, and across sector boundaries. However, remember that a data "0" cannot be programmed to a data "1". Only erase operations can convert a logical "0" to a logical "1". Attempting to program data from "0" to "1" may cause the device to exceed time limits, or even worse, result in an apparent success according to the $\overline{\text{Data}}$ Polling algorithm. In the later case, however, a subsequent read of this bit will show that the data is still a logical "0".

Figure 1 illustrates the Byte/Word Programming Algorithm using typical command strings and bus operations.

The device will ignore any commands written to the chip during execution of the internal Byte/Word Programming Algorithm. If a hardware $\overline{\text{RESET}}$ occurs during the Byte/Word Programming operation, the data at that particular address location will be corrupted.

Chip Erase Command

Chip erase is a six bus cycle operation (see Table 6). The chip erase begins on the rising edge of the last $\overline{\text{WE}}$ pulse in the command sequence.

Upon executing the Chip Erase command sequence, the device's internal state machine executes an internal erase algorithm. The system is not required to provide further controls or timings. The device will automatically provide adequate internally generated erase pulses and verify chip erase within the proper cell margins. During chip erase, all sectors of the device are erased except protected sectors.

During Chip Erase, data bit DQ7 shows a logical "0". This operation is known as $\overline{\text{Data}}$ Polling. The erase operation is completed when the data on DQ7 is a logical "1" (see Write Operation Status section). Upon completion of the Chip Erase operation, the device returns to read mode. At this time, the address pins are no longer latched. Note that $\overline{\text{Data}}$ Polling must be performed at a sector address within any of the sectors being erased and not a protected sector to ensure that DQ7 returns a logical "1" upon completion of the Chip Erase operation.

Figure 2 illustrates the Chip Erase Algorithm using typical command strings and bus operations.

The device will ignore any commands written to the chip during execution of the internal Chip Erase algorithm. If a hardware $\overline{\text{RESET}}$ occurs during the Chip Erase operation, the data in the device will be corrupted.

Sector Erase Command

Sector erase is a six bus cycle operation (see Table 6). The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{\text{WE}}$, while the command data is latched on the rising edge of $\overline{\text{WE}}$. An internal device timer will initiate the Sector Erase operation 100 mS ±20% (80 uS to 120 uS) from the rising edge of the $\overline{\text{WE}}$ pulse for the last Sector Erase command entered on the device.

Upon executing the Sector Erase command sequence, the device's internal state machine executes an internal erase algorithm. The system is not required to provide further controls or timings. The device automatically provides adequate internally generated erase pulses and verify sector erase within the proper cell margins. Protected sectors of the device will not be erased, even if they are selected with the Sector Erase command.

Multiple sectors can be erased simultaneously by writing the sixth bus cycle command of the Sector Erase command for each sector to be erased. The time between initiation of the next Sector Erase

command must be less than 80 mS to guarantee acceptance of the command by the internal state machine. The time-out window can be monitored via the write operation status pin DQ3 (refer to the Write Operation Status section for Sector Erase Timer operation). It is recommended that CPU interrupts be disabled during this time to ensure that the subsequent Sector Erase commands can be initiated within the 100 uS window. The interrupts can be re-enabled after the last Sector Erase command is written. As mentioned above, an internal device timer will initiate the Sector Erase operation 100 uS ±20% (80 uS to 120 uS) from the rising edge of the last $\overline{WE}$ pulse. Sector Erase Timer Write Operation Status pin (DQ3) can be used to monitor time out window. If another falling edge of the $\overline{WE}$ occurs within the 100 mS time-out window, the internal device timer is reset. Loading the sector erase buffer may be done in any sequence and with any number of sectors.

Any command other than Sector Erase or Erase Suspend during this period and afterwards will $\overline{RESET}$ the device to read mode, ignoring the previous command string. Resetting the device with a hardware $\overline{RESET}$ after it has begun execution of a Sector Erase operation will result in the data in the operated sectors being undefined and may be unrecoverable. In this case, restart the Sector Erase operation on those sectors and attempt to allow them to complete the Erase operation.

Command Definitions

Device operations are selected by writing specific address and data sequences in to the Command register. Writing incorrect addresses and data values or writing them in the improper sequence will $\overline{RESET}$ the device to Read mode. Table 5 defines the valid register command sequences. Either of the two Read/Reset commands will $\overline{RESET}$ the device (when applicable).

During Sector Erase operation, data bit DQ7 shows a logical "0". This operation is known as $\overline{Data}$ Polling. Sector Erase operation is complete when data on DQ7 is a logical "1" (see Write Operation Status section) at which time the device returns to read mode. At this time, the address pins are no longer latched. Note that $\overline{Data}$ Polling must be performed at a sector address within any of the sectors being erased and not a protected sector to ensure that DQ7 returns a logical "1" upon completion of the Sector Erase operation.

Figure 2 illustrates the Sector Erase Algorithm using typical command strings and bus operations.

During execution of the Sector Erase command, only the Erase Suspend and Erase Resume commands are allowed. All other commands will $\overline{RESET}$ the device to read mode.

Note: Do not attempt to write an invalid command sequence during the sector erase operation. Doing so will terminate the sector erase operation and the device will /RESET to the read mode.

Table 6. Command Definitions

Command Sequence		Bus Write Cycles	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
Reset/Read		Required	addr	Data	addr	Data	addr	Data	addr	Data	addr	Data	addr	Data
Reset/Read		1	XXXXH	F0H										
Reset	Word	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
/Read	Byte		AAAAH		5555H		AAAAH							
Electronic	Word	4	5555H	AAH	2AAAH	55H	5555H	90H	01H(7)	2223H (T Device ID) 22ABH (B Device ID)				
ID	Byte		AAAAH		5555H		AAAAH			23H (T Device ID) ABH (B Device ID)				
Program	Word	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD				
	Byte		AAAAH		5555H		AAAAH							
Chip	Word	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Erase	Byte		AAAAH		5555H		AAAAH		AAAAH		5555H		AAAAH	
Sector	Word	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Erase	Byte		AAAAH		5555H		AAAAH		AAAAH		5555H			
Erase	Word	1	XXXXH	B0H										
Suspend	Byte													
Erase	Word	1	XXXXH	30H										
Resume	Byte													

Notes:

1. Bus operations are defined in Tables 1 and 2.

2. For a Command Sequence, address bit A15 = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA).

3. RA = Address of the memory location to be read.
   RD = Data read from location RA during read operation.
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$.
   SA = Address of sector to be erased. (See Table 4 for top boot and Table 5 for bottom boot.)

4. The Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress.

5. Reading from, and programming to, non-erasing sectors is allowed in the Erase Suspend mode.

6. The System should generate the following address patterns:
   Word Mode: 5555H or 2AAAH to addresses A0 - A14.
   Byte Mode: AAAAH or 5555H to addresses A-1 - A14.

7. Address 00H returns the manufacturer's ID code (Bright Microelectronics - ADH), address 01H returns the device ID code.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the user to interrupt a Sector Erase operation and read data from or to a sector that is not being erased. The Erase Suspend command is applicable only during Sector Erase operation, including, but not limited to, sector erase time-out period after any Sector Erase commands (30H) have been initiated.

Writing the Erase Suspend command during the time-out will result in immediate termination of the time-out period. Any subsequent writes of the Sector Erase command will be taken as the Erase

Resume command (30H). Note that any other commands during the time-out will $\overline{\text{RESET}}$ the device to the Read mode. The address pins are "don't cares" when writing the Erase Suspend or Erase Resume commands.

When the Erase Suspend command is written during a Sector Erase operation, the chip will take between 1 uS and 230 uS to suspend the erase operation and go into Erase Suspended mode. During this time, the system can monitor the $\overline{\text{Data}}$ Polling or Toggle Bit write operation status flags to determine when the device has entered erase suspend mode (see Write Operation Status section.) The system must use an address of an erasing sector to monitor $\overline{\text{Data}}$ Polling or Toggle Bit to determine if the Sector Erase operation has been suspended.

In Erase Suspend mode, the system can read data from any sector that is not being erased. A read from a sector being erased will result in write operation status data. After the system writes the Erase Suspend command and waits until the Toggle Bit stops toggling, data reads from the device may then be performed (see Write Operation Status section). Any further writes of the Erase Suspend command at this time will be ignored.

To resume operation of Sector Erase, the Erase Resume command (30H) should be written. Any further writes of the Erase Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed Sector Erase operation.

DQ7

$\overline{\text{Data}}$ Polling

The BM29F400 device features $\overline{\text{Data}}$ Polling as a method to indicate to the host the status of the Byte/Word Programming, Chip Erase, and Sector Erase operations. When the Byte/Word Programming operation is in progress, an attempt to read the device will produce the compliment of the data last written to DQ7. Upon completion of the Byte/Word Programming operation, an attempt to read the device will produce the true data last written to DQ7. When the Chip Erase or Sector Erase operation is in progress, an attempt to read the device will produce a logical "0" at the DQ7 output. Upon completion of the Chip Erase or Sector Erase operation, an attempt to read the device will produce a logical "1" at the DQ7 output. The flowchart for Data Polling (DQ7) is shown in Figure 3.

For Chip Erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For Sector Erase, the $\overline{\text{Data}}$ Polling is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. For both Chip Erase and Sector Erase, $\overline{\text{Data}}$ Polling must be performed at sector address within any of the sectors being erased and not a protected sector. Otherwise, the $\overline{\text{Data}}$ Polling status may not be valid. Once the Internal Algorithm operation is close to being completed, the BM29F400 data pins (DQ7) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the device is driving status information on DQ7 at one instant and valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read status or valid data. Even if the device has completed the Internal Algorithm operation and DQ7 has a valid data, data outputs on DQ0-DQ6 may be still invalid. Valid data on DQ0-DQ7 will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is only active during the Byte/Word Programming operation, Chip Erase operation, Sector Erase Operation, or Sector Erase time-out window (see Table 7).

DQ6

Toggle Bit

The BM29F400 also features the "Toggle Bit" as a method to indicate to the host system the status of the Internal Programming and Erase Algorithms (see Figure 4 for Toggle Bit (DQ6) flowchart.

During an Internal Programming or Erase Algorithm cycle, successive attempts to read ($\overline{OE}$ toggling) data from the device will result in DQ6 toggling between one and zero. Once Internal Programming or Erase operation is completed, DQ6 will stop toggling and valid data will be read on the next successive attempts. During $\overline{BYTE}$ Programming, Toggle Bit is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For Chip Erase, Toggle Bit is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For Sector Erase, Toggle Bit is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. Toggle Bit is also active during sector erase time-out window.

In Byte/Word Programming, if the sector being written to is protected, the Toggle Bit will toggle for about 300 nS and then stop toggling without the data having changed. In Chip Erase or Sector Erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the Toggle Bit for about 300ns and then drop back into read mode, having changed none of the data. Either $\overline{CE}$ or $\overline{OE}$ toggling will cause the DQ6 Toggle Bit I to toggle.

DQ5

Exceeded Timing Limits

DQ5 will indicate if the Byte/Word Programming, Chip Erase, or Sector Erase time has exceeded the specified limits (internal pulse count) of the device. Under these conditions DQ5 will produce a logical "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{Data}$ Polling is the only operating function of the device under this condition. The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Table 1.

If this failure condition occurs during Sector Erase operation, it specifies that particular sector is bad and it may not be reused. However, other sectors are still functional and may continue to be used for the program or erase operation. The device must be $\overline{RESET}$ to the Read mode to use other sectors of the device. Write the Read/Reset command sequence to the device, and then execute the Byte/Word Programming or Sector Erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this failure condition occurs during Chip Erase operation, it specifies that the entire chip is bad or combination of sectors are bad. In so, the chip should not be reused.

If this failure condition occurs during Byte/Word Programming operation, it indicates the entire sector containing that $\overline{BYTE}$ is bad and this sector may not be reused (other sectors are still functional and can be reused.)

The DQ5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case, the device may exceed time limits and not complete the Internal Algorithm operation. Hence, the system never reads a valid data on DQ7 bit and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a "1".

DQ3

Sector Erase Timer

After the completion of the initial Sector Erase command sequence, the sector erase time-out window will begin. DQ3 will remain low until the time-out window is closed. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial Sector Erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, DQ3 maybe used to determine if the Sector Erase time-out window is still open. If DQ3 is a logical "1", the internally controlled erase cycle has begun. Attempts to write subsequent command to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit. If DQ3 is a logical "0", the device will accept additional Sector Erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent Sector Erase command. If DQ3 were high on the second status check, the command may not have been accepted. Refer to Table 7: Write Operation Status Flags.

Write Operations Status

Table 7. Write Operation Status Flags(1)

	Status	DQ7	DQ6	DQ5	DQ3
In Progress	Byte/Word Programming Operation	/DQ7	Toggle	0	N/A
	Chip or Sector Erase Operation	0	Toggle	0	1
	Erase Suspend Mode (Non-Erase Suspended Sector)	Data	Data	Data	Data
Exceeded Time Limits	Byte/Word Programming Operation	/DQ7	Toggle	1	0
	Chip or Sector Erase Operation	0	Toggle	1	1

Notes: DQ0, DQ1, DQ4 are reserve pins for future use.

RY/BY

Ready/Busy Status

The BM29F400 provides a RY/BY open-drain output pin as a way to indicate to the host system that an Internal Programming or Erase operation is either in progress or has been completed. If the RY/BY output is low, the device is busy with either a Programming or Erase operation. If the RY/BY output is high, the device is ready to accept a Read, Programming, or Erase command. When the RY/BY pin is low, the device will not accept any additional Programming or Erase commands with the exception of the Erase Suspend command. If the BM29F400 is placed in an Erase Suspend mode, the RY/BY output will be high.

During a programming operation, the RY/BY pin is driven low after the rising edge of the fourth $\overline{\text{WE}}$ pulse. During an erase operation, the RY/BY pin is driven low after the rising edge of the sixth $\overline{\text{WE}}$ pulse. The RY/BY pin will indicate a busy condition during the $\overline{\text{RESET}}$ pulse. Refer to the timing waveforms for the RY/BY status pin for further clarification. The RY/BY pin is high in the Standby mode.

Since this is an open-drain output, several RY/BY pins can be tied together with a pull-up resistor to Vcc.

$\overline{\text{RESET}}$ **Hardware Reset**

The BM29F400 device may be $\overline{\text{RESET}}$ by driving the $\overline{\text{RESET}}$ pin to V_{IL}. The $\overline{\text{RESET}}$ pin must be kept low (V_{IL}) for at least 500 nS. Pulling the $\overline{\text{RESET}}$ pin low will terminate any operation in progress. The internal state machine will be $\overline{\text{RESET}}$ to the read mode 1 mS to 230 mS after the $\overline{\text{RESET}}$ pin is driven low. If a hardware $\overline{\text{RESET}}$ occurs during a Programming or Erase operation, the data at that particular location will be indeterminate.

When the $\overline{\text{RESET}}$ pin is low and the internal $\overline{\text{RESET}}$ is complete, the device goes to Standby mode and cannot be accessed. Also, note that all the data output pins are tri-stated for the duration of the $\overline{\text{RESET}}$ pulse. Once the $\overline{\text{RESET}}$ pin is taken high, the device requires 500 nS of wake up time until outputs are valid for a read access.

The $\overline{\text{RESET}}$ pin may be tied to the system $\overline{\text{RESET}}$ input. Therefore, if a system $\overline{\text{RESET}}$ occurs during an Internal Programming or Erase operation, the device will be automatically $\overline{\text{RESET}}$ to read mode. This will enable the system's microprocessor to read the boot-up firmware from the Flag's memory.

Data Protection

The BM29F400 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power-up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from Vcc power-up and power-down transitions or system noise.

Low Vcc Write Inhibit

To avoid initiation of a write cycle during Vcc power-up and power-down, a write cycle is locked out for Vcc less than 3.2V (typically 3.7V). If Vcc < V_{LKO}, the command register is disabled and all internal programming/erase circuits are disabled. Under this condition the device will $\overline{\text{RESET}}$ to the Read mode. Subsequent writes will be ignored until the Vcc level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when Vcc is above 3.2V.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 nS (typical) on $\overline{\text{OE}}$, $\overline{\text{CE}}$ or $\overline{\text{WE}}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{\text{OE}}$ = V_{IL}, $\overline{\text{CE}}$ = V_{IH}, or $\overline{\text{WE}}$ = V_{IH}. To initiate a write cycle $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be a logical "0" while $\overline{\text{OE}}$ is a logical "1".

Power-Up Write Inhibit

Power-up of the device with $\overline{\text{WE}}$ = $\overline{\text{CE}}$ = V_{IL} and $\overline{\text{OE}}$ = V_{IH} will not accept commands on the rising edge of $\overline{\text{WE}}$. The internal state machine is automatically $\overline{\text{RESET}}$ to the Read mode on power-up.

Sector Unprotect

The BM29F400 also features a sector unprotect mode, so that protected sectors may be unprotected to incorporate any changes in the code. Protecting all sectors is necessary before unprotecting any sector(s). Sector unprotection is accomplished in a PROM programmer.

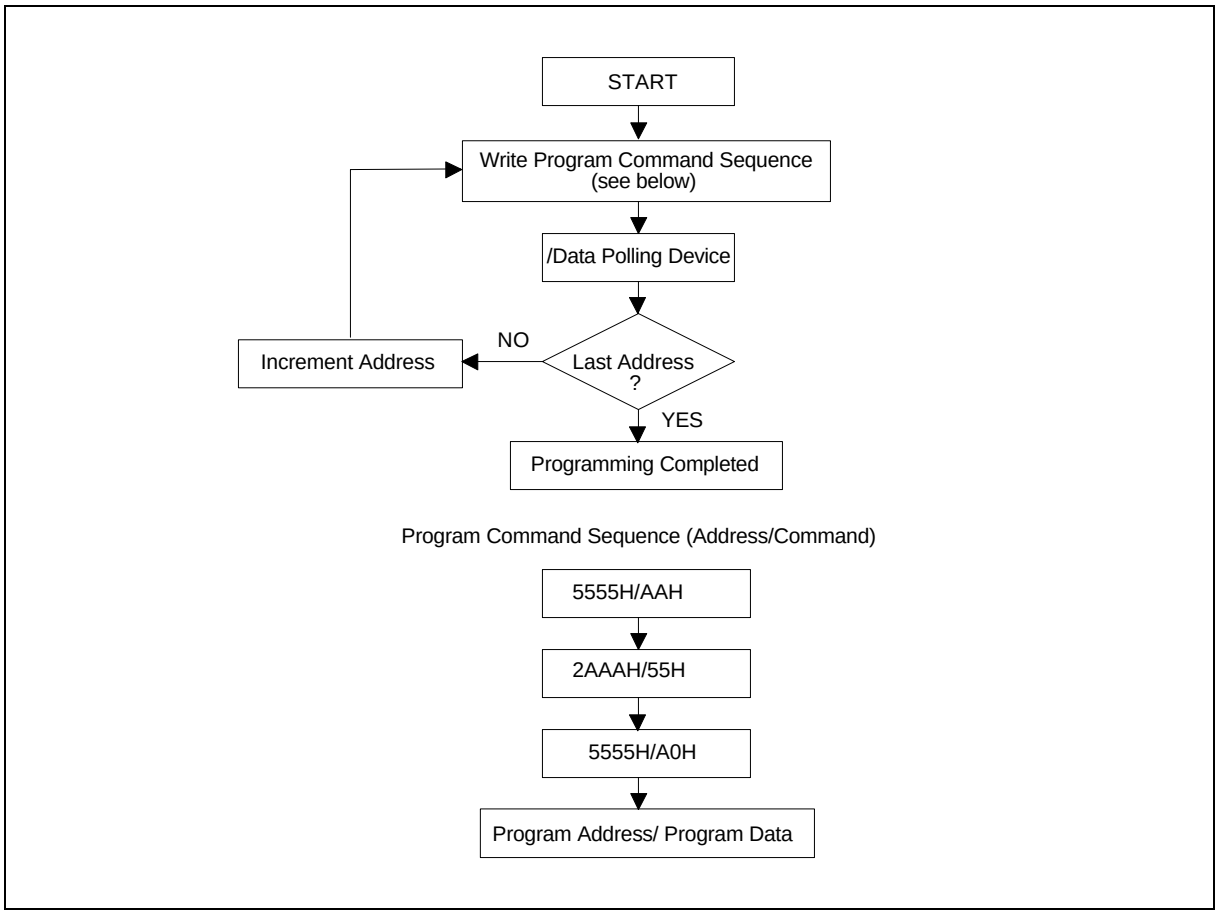


Figure 1. Internal Programming Algorithm

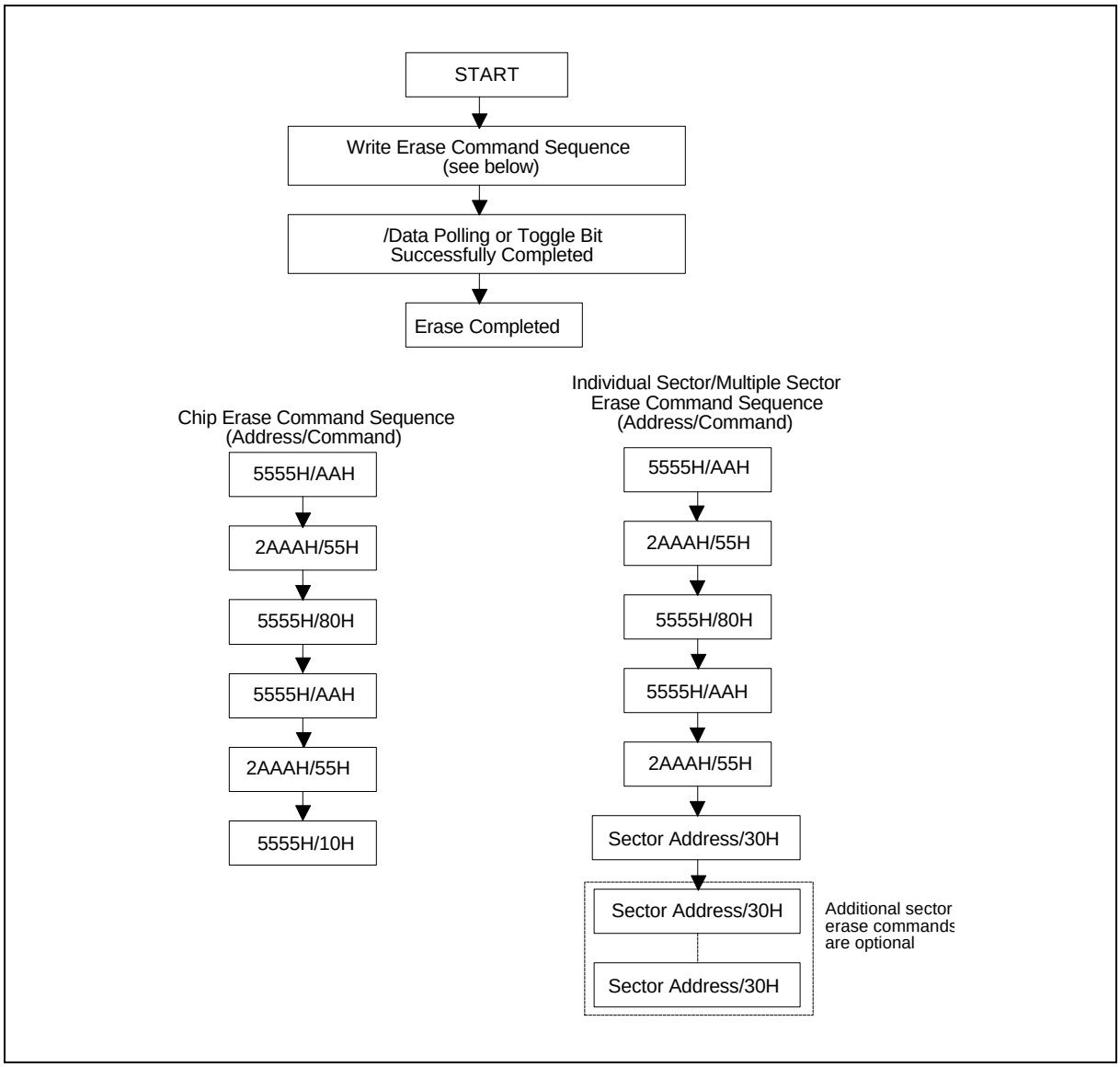


Figure 2. Internal Erase Algorithm

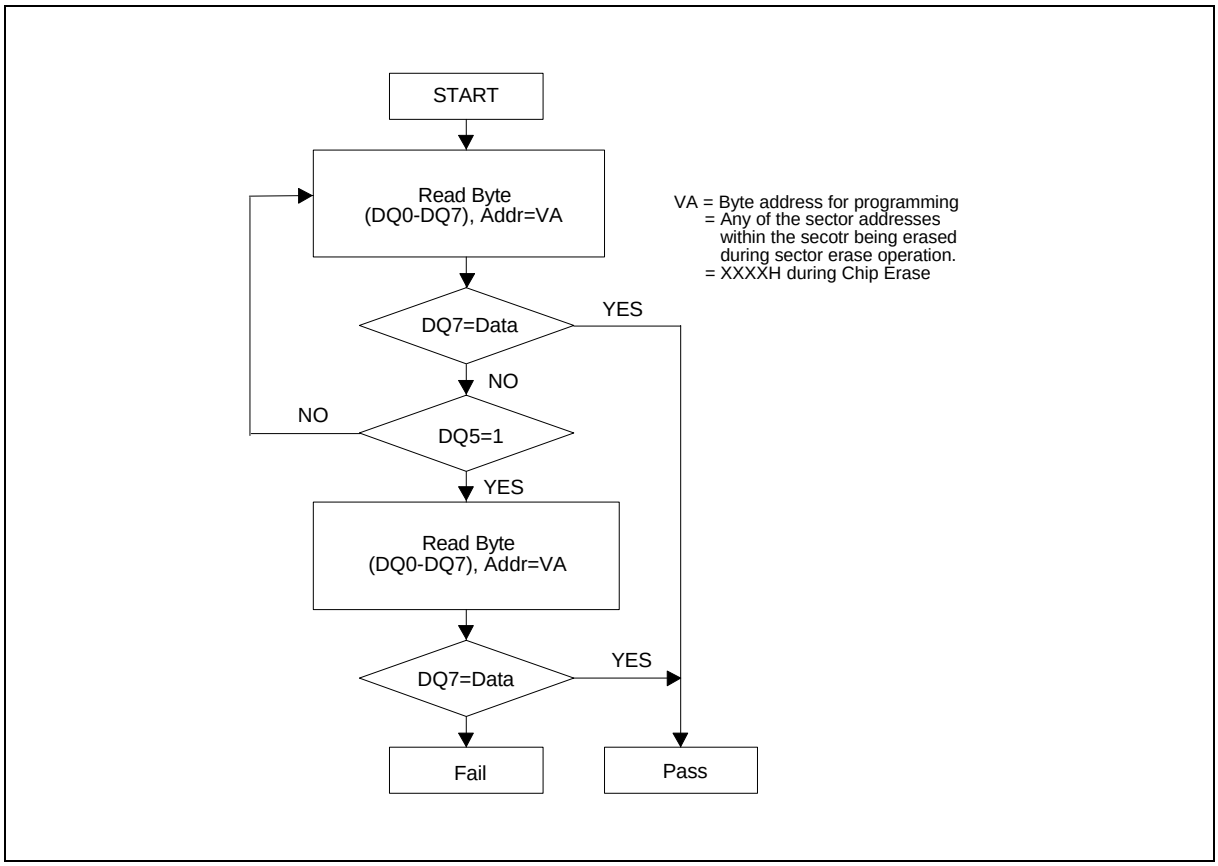


Figure 3. $\overline{\text{Data}}$ Polling Algorithm

Notes: DQ7 is rechecked even if DQ5 = logical "1" because DQ7 may change simultaneously with DQ5.

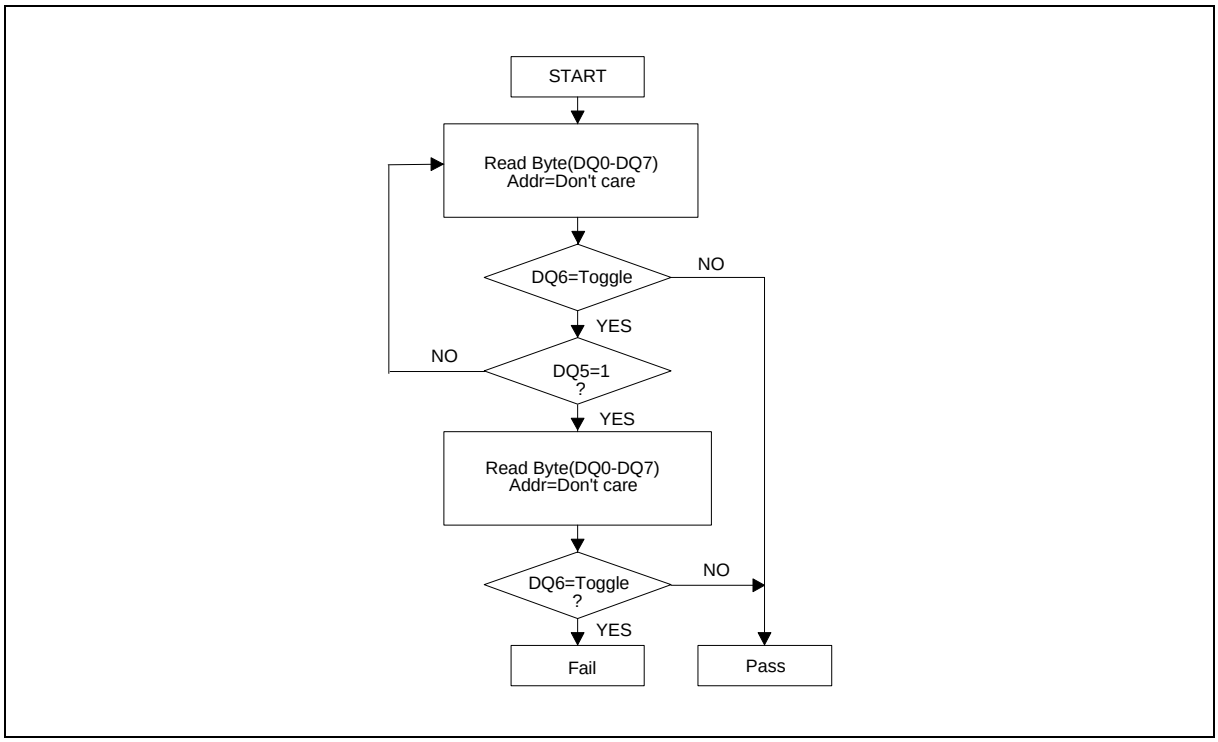


Figure 4. Toggle Bit Algorithm

Note: DQ6 is rechecked even if DQ5 = logical "1" because DQ6 may stop toggling at the same time as DQ5 changing to a logical "1".

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Storage Temperature Plastic Packages	-65 to +125	°C
Ambient Temperature With Power Applied	-55 to +125	°C
Voltages with Respect to Ground All pins except A9 (Note 1) Vcc (Note 1) A9 (Note 2)	 -2 to +7 -2 to +7 -2 to +14	V
Output Short Circuit Current (Note 4)	200	mA

Notes :

1. Minimum DC voltage on input or I/O pins is -0.5V.
   During voltage transitions, inputs may overshoot Vss to -2.0V for periods of up to 20 nS. Maximum DC voltage on output and I/O pins is Vcc +0.5V. During Voltage transitions, outputs may overshoot to Vcc + 2.0V for periods up to 20 nS.
2. Minimum DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 may overshoot Vss to -2.0V for periods of up to 20 nS. Maximum DC input voltage on A9 is + 12.5V which may overshoot to 14.0V for periods of up to 20 nS.
3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.

Operating Ranges

PARAMETER	RATING	UNIT
Commercial (C) Devices	0 to +70	°C
Industrial (I) Devices	-40 to +85	°C
Extended (I) Devices	-55 to +125	°C
Vcc Supply Voltage Vcc for BM29F400-90	+4.5 to 5.5	V

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

***Notice**: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

Maximum Negative Overshoot Waveform

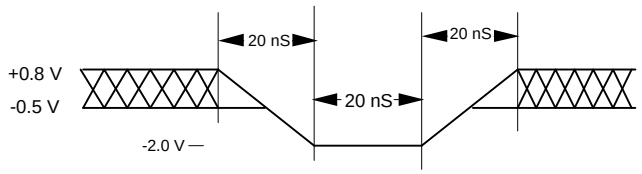


Figure 5.

Maximum positive Overshoot Waveform

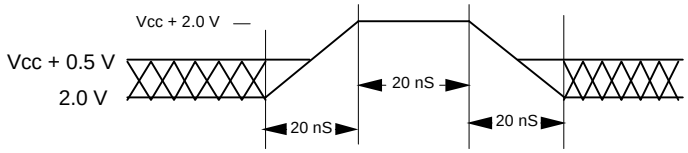


Figure 6.

DC CHARACTERISTICS

TTL/NMOS Compatible

PARAMETER	SYM.	TEST CONDITIONS		MIN.	MAX.	UNIT
Input Load Current	I_{LI}	V_{IN} = Vss to V_{CC}, V_{CC} = V_{CC} Max.			±1.0	uA
A9 Input Load Current	I_{LIT}	V_{CC} = V_{CC} Max., A9 = 12.5 V			±1.0	uA
Output Leakage Current	I_{LO}	V_{OUT} = Vss to V_{CC}, V_{CC} = V_{CC} Max.			±1.0	uA
V_{CC} Active Current(1)	I_{CC1}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	Byte		40	mA
			Word		50	mA
V_{CC} Active Current(2,3)	I_{CC2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			60	mA
V_{CC} Standby Current	I_{CC3}	V_{CC} = V_{CC} Max., $\overline{CE}$ = $\overline{RESET}$ = V_{IH}			1.0	mA
V_{CC} Standby Current ($\overline{RESET}$)	I_{CC4}	V_{CC} = V_{CC} Max., $\overline{RESET}$ = V_{IL}			1.0	mA
Input Low Level	V_{IL}			-0.5	0.8	V
Input High Level	V_{IH}			2.0	V_{CC} +0.5	V
Voltage for Electronic	V_{ID}	V_{CC} = 5.0V		11.5	12.5	V
Output Low Voltage	V_{OL}	I_{OL} = 5.8 mA, V_{CC} = V_{CC} Min.			0.45	V
Output High Voltage	V_{OH}	I_{OH} = -2.5 mA, V_{CC} = V_{CC} Min.		2.4		V

Notes:

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Internal Algorithm (program or erase) is in progress.
3. Not 100% tested.

DC Characteristics, continued

CMOS Compatible

PARAMETER	SYM.	TEST CONDITIONS	MIN.	MAX.	UNIT
Input Load Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.		±1.0	uA
A9 Input Load Current	I_{LIT}	V_{CC} = V_{CC} Max., A9 = 12.5 V		±1.0	uA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.		±1.0	uA
V_{CC} Active Current(1)	I_{CC1}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	Byte	40	mA
			Word	50	mA
V_{CC} Active Current(2,3)	I_{CC2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		60	mA
V_{CC} Standby Current	I_{CC3}	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{CC} ±0.5V, $\overline{RESET}$ = V_{CC} ±0.5V		100	uA
Vcc Standby Current ($\overline{RESET}$)	I_{CC4}	V_{CC} = V_{CC} Max., $\overline{RESET}$ = V_{SS} ±0.5V		100	uA
Input Low Level	V_{IL}		-0.5	0.8	V
Input High Level	V_{IH}		0.7 x V_{CC}	V_{CC} + 0.3	V
Voltage for Electronic ID and Sector Protect	V_{ID}	V_{CC} = 5.0 V	11.5	12.5	V
Output Low Voltage	V_{OL}	I_{OL} = 5.8 mA, V_{CC} = V_{CC} Min.		0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.5 mA, V_{CC} = V_{CC} Min.	0.85 x V_{IH}		V
	V_{OH2}	I_{OH} = -100 mA, V_{CC} = V_{CC} Min.	V_{CC} -0.4	V	
Low V_{CC} Lock-out Voltage	V_{LKO}		3.2	4.2	V

Notes:

1.The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 Mhz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.

2. I_{CC} active while Internal Algorithm (program or erase) is in progress.

3. Not 100% tested.

AC CHARACTERISTICS

Read-Only Operations

PARAMETER SYM.		DESCRIPTION	TEST SETUP		-90	-120	-150	UNIT
JEDEC	Standard							
t_{AVAV}	t_{RC}	Read Cycle Time(2)		Min.	90	120	150	nS
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = V_{IL} $\overline{OE}$ = V_{IL}	Max.	90	120	150	nS
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Max.	90	120	150	nS
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max.	35	50	55	nS
t_{EHQZ}	t_{HZ}	Chip Enable to Output High Z(3,4)		Max.	20	30	35	nS
t_{GHQZ}	t_{DF}	Output Enable to Output High Z(2,3)			20	30	35	nS
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		Min.	0	0	0	nS
	t_{READY}	$\overline{RESET}$ Pin Low to Read Mode(4)		Max.	20	20	20	mS
	t_{ELFL} t_{ELFH}	$\overline{CE}$ to $\overline{BYTE}$ Switching Low or High		Max.	5	5	5	nS

Notes:

1. Test Conditions: Output Load: 1 TTL gate and 100 pF
   Input rise and fall times: 20 nS; Input pulse levels: 0.45 V to 2.4 V
2. Timing measurement reference level
   Input: 0.8 and 2.0 V; Output: 0.8 and 2.0 V
3. Output driver disable time.
4. Not 100% tested.

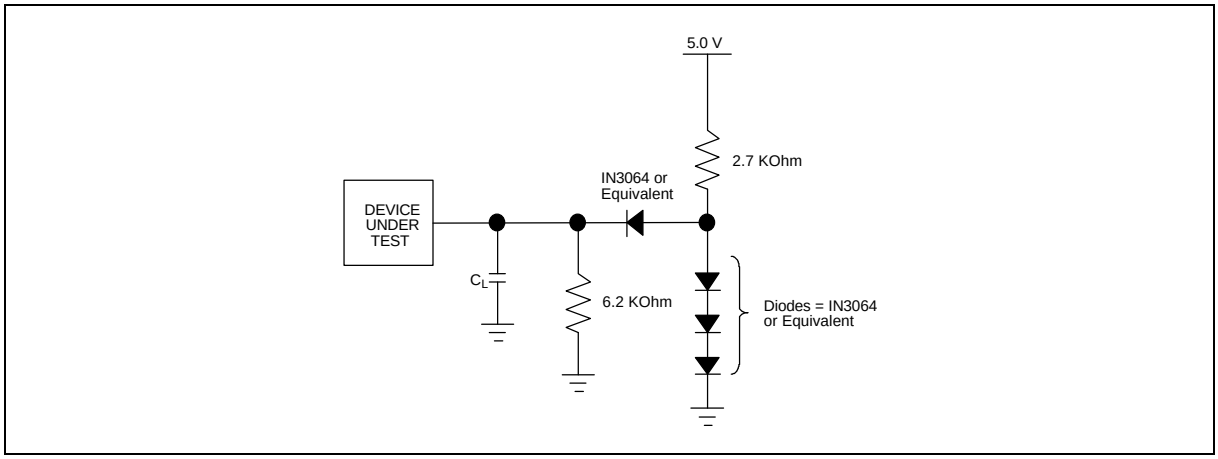


Figure 7. Test Condition

Note: CL = 100 pF including jig capacitance.

AC CHARACTERISTICS

Programming/Erase Operations

PARAMETER SYM. JEDEC	PARAMETER SYM. Standard	DESCRIPTION			-90	-120	-150	UNIT
t_{AVAV}	t_{WC}	Write Cycle Time(1)		Min.	90	120	150	nS
t_{AVWL}	t_{AS}	Address Setup Time		Min.	0	0	0	nS
t_{WLAX}	t_{AH}	Address Hold Time		Min.	45	50	50	nS
t_{DVWH}	t_{DS}	Data Setup Time		Min.	45	50	50	nS
t_{WHDX}	t_{DH}	Data Hold Time		Min.	0	0	0	nS
	t_{OES}	Output Enable Setup Time		Min.	0	0	0	nS
	t_{OEH}	Output Enable Hold Time	Read(1)	Min.	0	0	0	nS
			Toggle & $\overline{\text{Data}}$ Polling(1)	Min.	10	10	10	nS
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write		Min.	0	0	0	nS
t_{ELWL}	t_{CS}	$\overline{\text{CE}}$ Setup Time		Min.	0	0	0	nS
t_{WHEH}	t_{CH}	$\overline{\text{CE}}$ Hold Time		Min.	0	0	0	nS
t_{WLWH}	t_{WP}	Write Pulse Width		Min.	45	50	50	nS
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min.	20	20	20	nS
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ. Max.	16 400	16 400	16 400	uS uS
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation(2)		Typ. Max.	0.26 12	0.26 12	0.26 12	sec
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation(2)		Typ. Max.	2.0 90	2.0 90	2.0 90	sec
	t_{VCS}	Vcc Setup Time(1)		Min.	50	50	50	mS
	t_{VIDR}	Rise Time to VID(1,3)		Min.	500	500	500	nS
	t_{OESP}	$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active(1, 3, 4)		Min.	4	4	4	mS
	t_{RP}	$\overline{\text{RESET}}$ Pulse Width		Min.	500	500	500	nS
	t_{RSP}	$\overline{\text{RESET}}$ Setup Time(3)		Min.	4	4	4	uS
	t_{BUSY}	Programming/Erase Valid to RY/BY Delay(1)		Min.	40	50	60	nS
	t_{VLHT}	Voltage Transition Time(1, 4)		Min.	4	4	4	mS
	t_{WPP1}	Sector Protect Write Pulse Width(4)		Min.	100	100	100	mS
	t_{WPP2}	Sector Unprotect Write Pulse Width(4)		Min.	350	350	350	mS
	t_{CSP}	$\overline{\text{CE}}$ Setup Time to $\overline{\text{WE}}$ Active(1, 4)		Min.	4	4	4	nS

Notes:
1. Not 100% tested.
2. Does not include pre-programming time.
3. This timing is for Temporary Sector Unprotect operation.
These timings are for Sector Protect and/or Sector Unprotect operations.

SWITCHING WAVEFORMS

WAVEFORM	INPUT	OUTPUT
———	Must Be Steady	Will Be Steady
⟋⟋⟋	May Change from H to L	Will Be Change from H to L
⟍⟍⟍	May Change from L to H	Will Be Change from L to H
⟋⟍⟋⟍	Don't Care, Any Change Permitted	Change, State Unknown
⟋⟍ ⟍⟋	Does Not Apply	Center Line is High impedance Off State

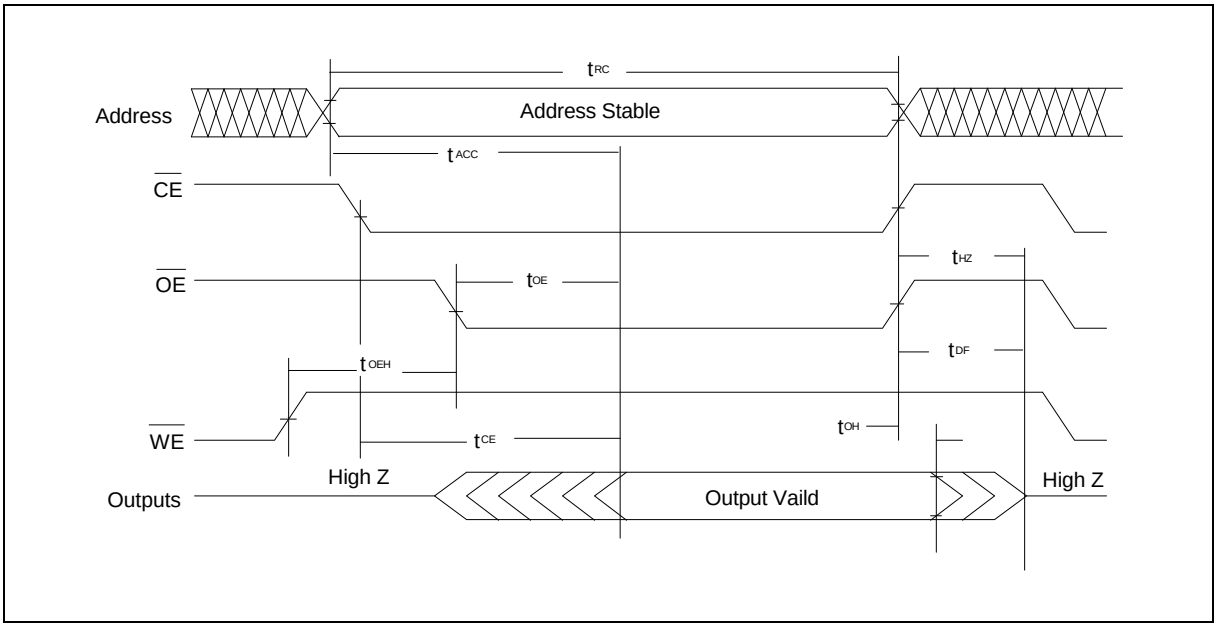


Figure 8. AC Waveforms for Read Operations

Switching Waveforms, continued

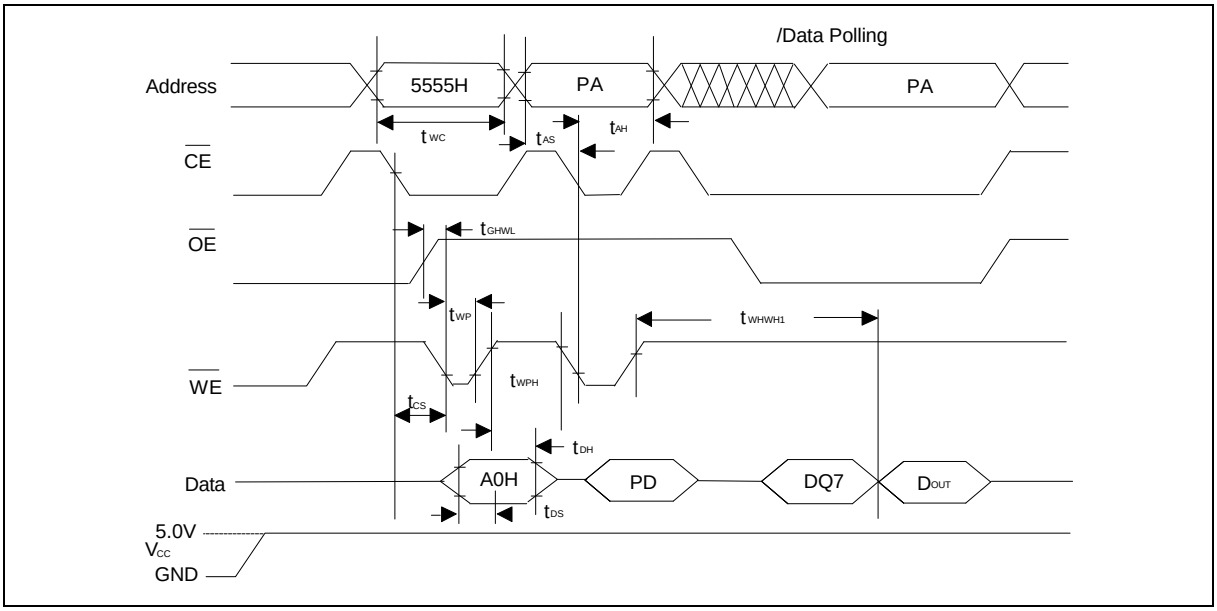


Figure 9. AC Waveforms Program Operations

Notes:
1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at $\overline{\text{BYTE}}$ address.
3. /DQ7 is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.
6. These waveforms are for 16-bit mode.

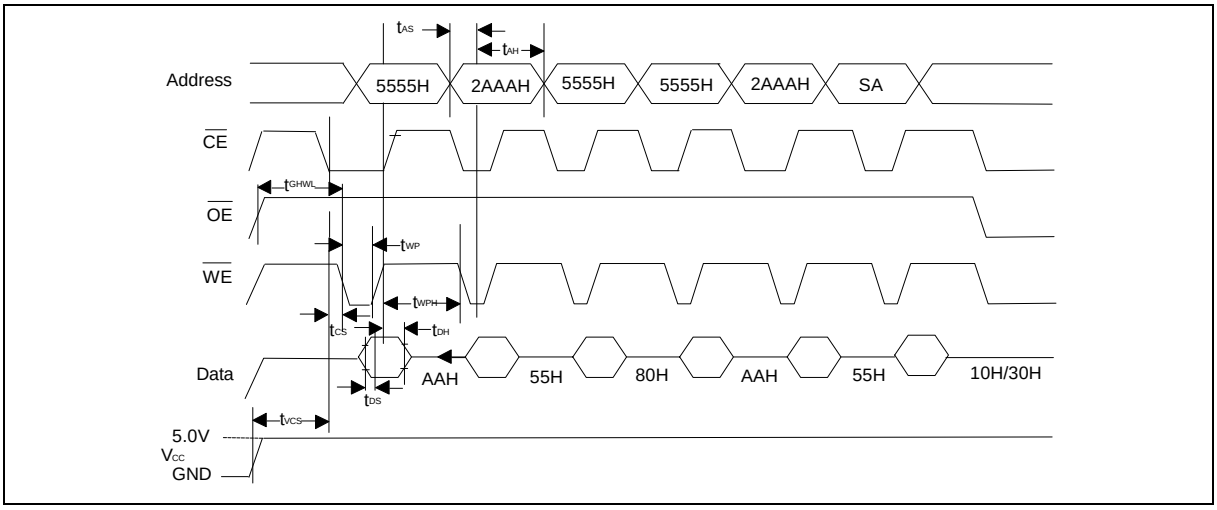


Figure 10. AC Waveforms Chip/Sector Erase Operations

Notes:
1. SA is the sector address for Sector Erase. Address = X = Don't Care for Chip Erase.
2. These waveforms are for 16-bit mode.

Switching Waveforms, continued

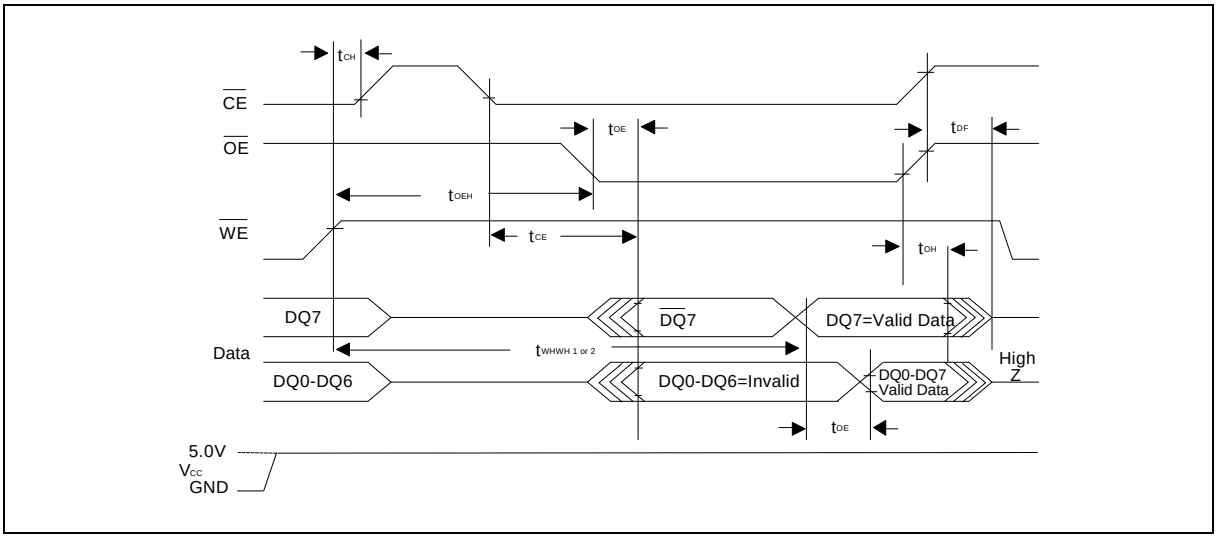


Figure 11. AC Waveforms for $\overline{\text{Data}}$ Polling during Internal Algorithm Operations

Note: DQ7 = Valid Data (The device has completed the internal program or erase operation.)

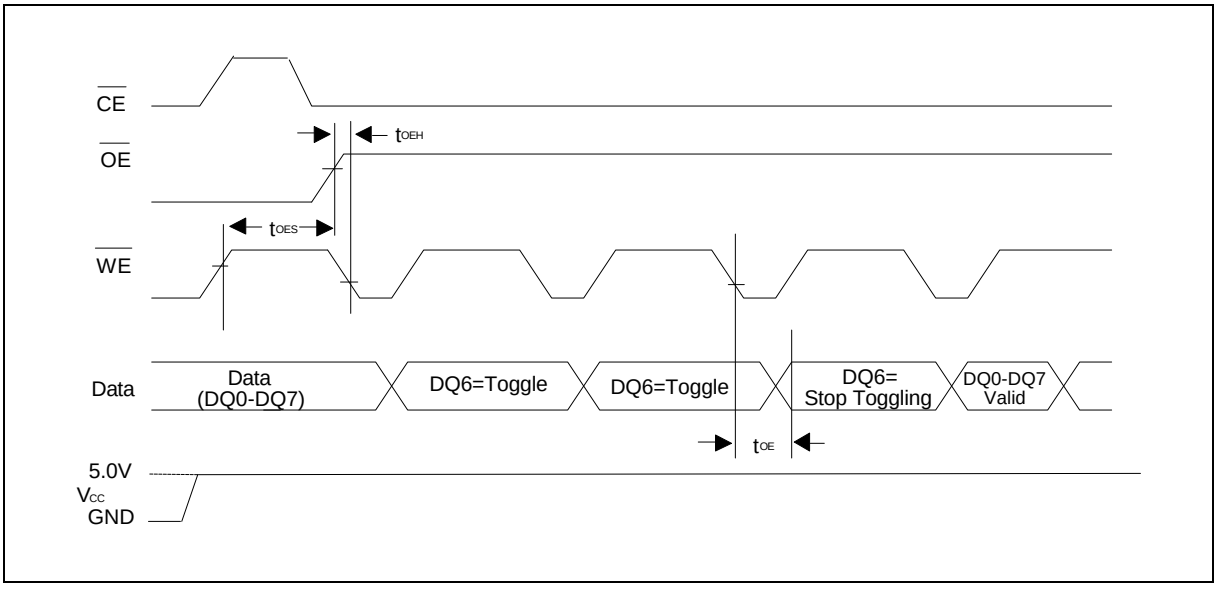


Figure 12 AC Waveforms for Toggle Bit during Internal Algorithm Operation

Note: DQ6 stops toggling (The device has completed the internal program or erase operation.)

Switching Waveforms, continued

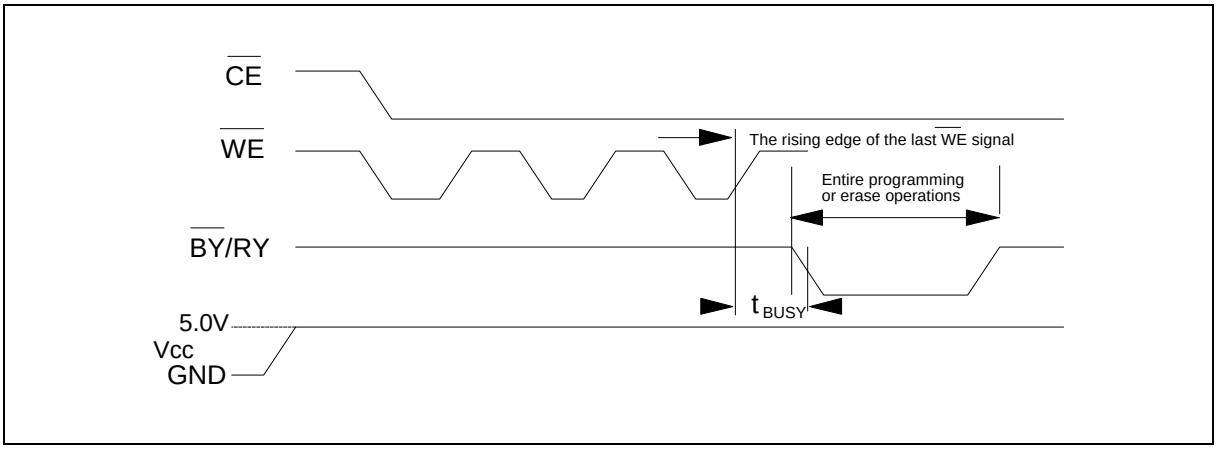


Figure 13. RY/BY Timing Diagram During Program/Erase Operation

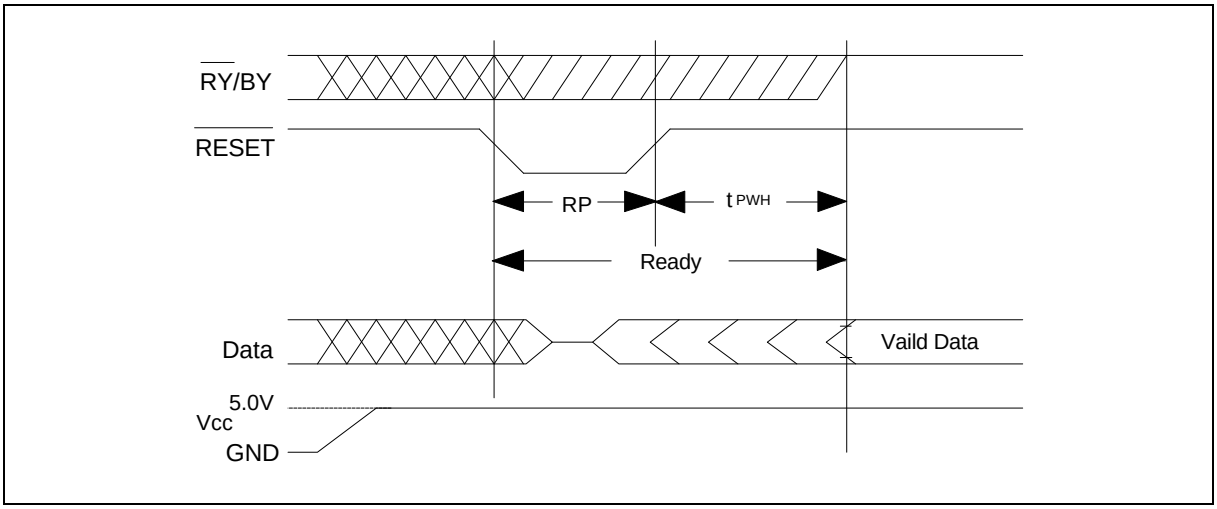


Figure 14. /RESET Timing Diagram

Switching Waveforms, continued

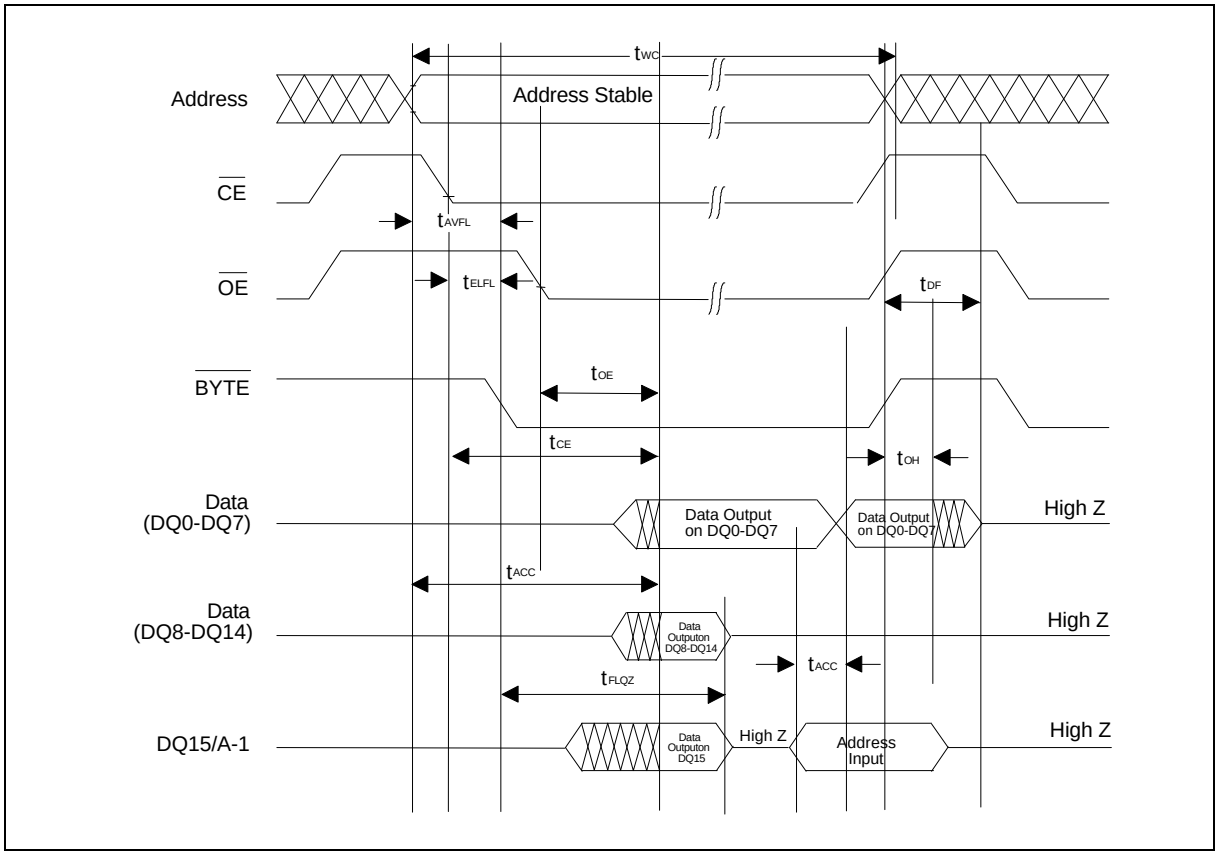


Figure 15. $\overline{\text{BYTE}}$ Timing Diagram for Read Operation

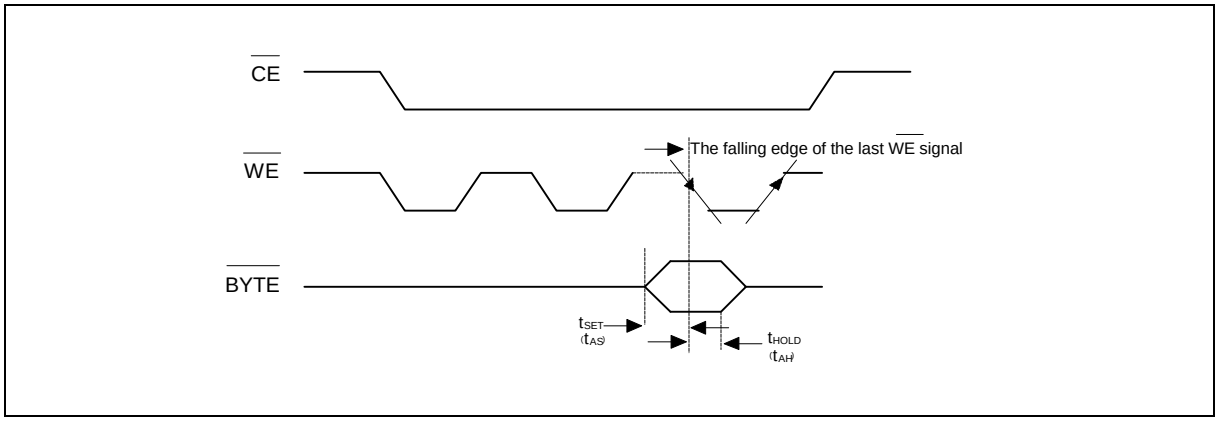


Figure 16. $\overline{\text{BYTE}}$ Timing Diagram for Write Operation

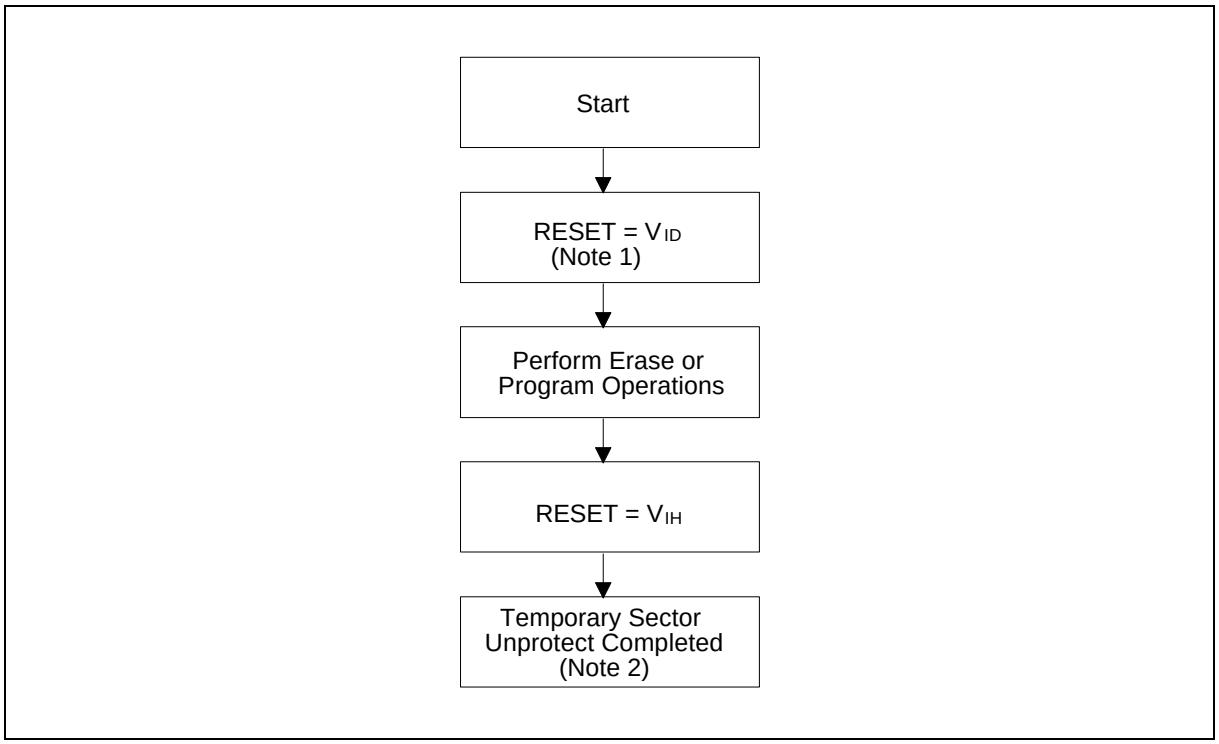


Figure 17. Temporary Sector Unprotect Algorithm

Notes:

1. All protected sector groups unprotected.
2. All previously protected sector groups are protected again.

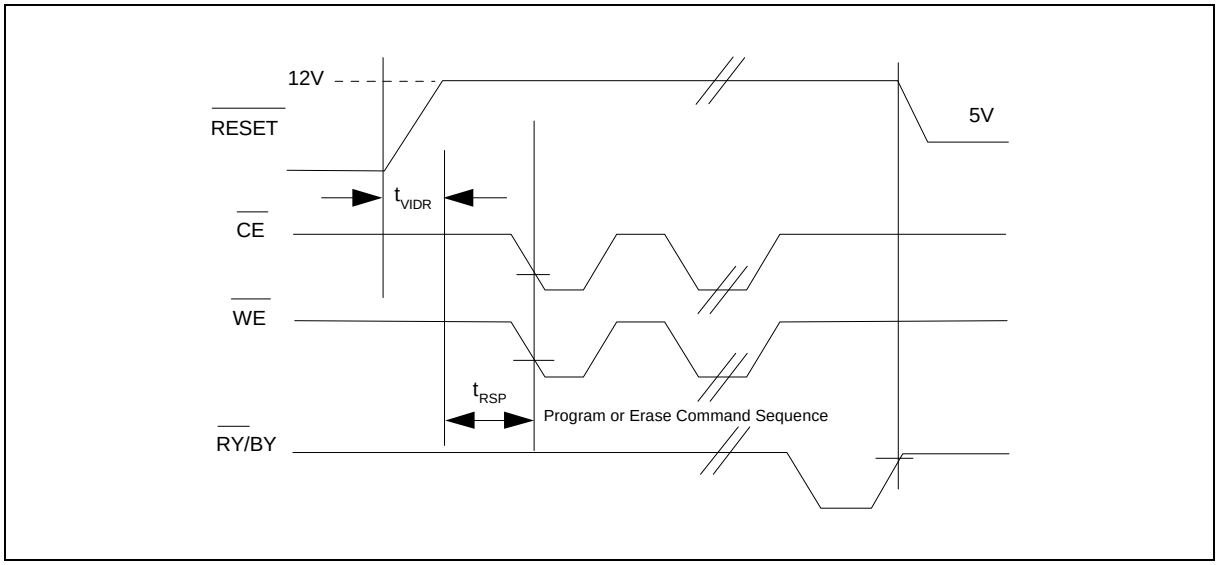


Figure 18. Temporary Unprotect Timing Diagram

AC CHARACTERISTICS

Programming/Erase Operations

PARAMETER	SYM.	DESCRIPTION			-90	-120	-150	Unit
JEDEC	Standard							
t_{AVAV}	t_{WC}	Write Cycle Time(1)		Min.	90	120	150	nS
t_{AVEL}	t_{AS}	Address Setup Time		Min.	0	0	0	nS
t_{ELAX}	t_{AH}	Address Hold Time		Min.	45	50	50	nS
t_{DVEH}	t_{DS}	Data Setup Time		Min.	45	50	50	nS
t_{EHDX}	t_{DH}	Data Hold Time		Min.	0	0	0	nS
	t_{OES}	Output Enable Setup Time(1)		Min.	0	0	0	nS
	t_{OEH}	Output Enable Hold Time	Read(1)	Min.	0	0	0	nS
			Toggle and $\overline{Data}$ Polling(1)	Min.	10	10	10	nS
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write		Min.	0	0	0	nS
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		Min.	0	0	0	nS
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min.	0	0	0	nS
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		Min.	45	50	50	nS
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High		Min.	20	20	20	nS
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ.	16	16	16	mS
				Max.	400	400	400	mS
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation(2)		Typ.	0.26	0.26	0.26	sec
				Max.	12	12	12	sec
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation(2)		Typ.	2.0	2.0	2.0	sec
				Max.	90	90	90	sec
	t_{VCS}	Vcc Setup Time(1,3)		Min.	50	50	50	mS
	t_{VIDR}	Rise Time to V_{ID}(1,3)		Min.	500	500	500	nS
	t_{VLHT}	Voltage Transition Time(1,3)		Min.	4	4	4	mS
	t_{WPP1}	Sector Protect Write Pulse Width(4)		Min.	100	100	100	mS
	t_{WPP2}	Sector Unprotect Write Pulse Width(4)		Min.	10	10	10	mS
	t_{OESP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active(1, 3)		Min.	4	4	4	mS
	t_{CSP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active(1, 4)		Min.	4	4	4	nS

Notes:
1. Not 100% tested.
2. Does not include pre-programming time.
3. This timing is for Sector Unprotect operation.
4. Output Driver Disable Time.

Switching Waveforms, continued

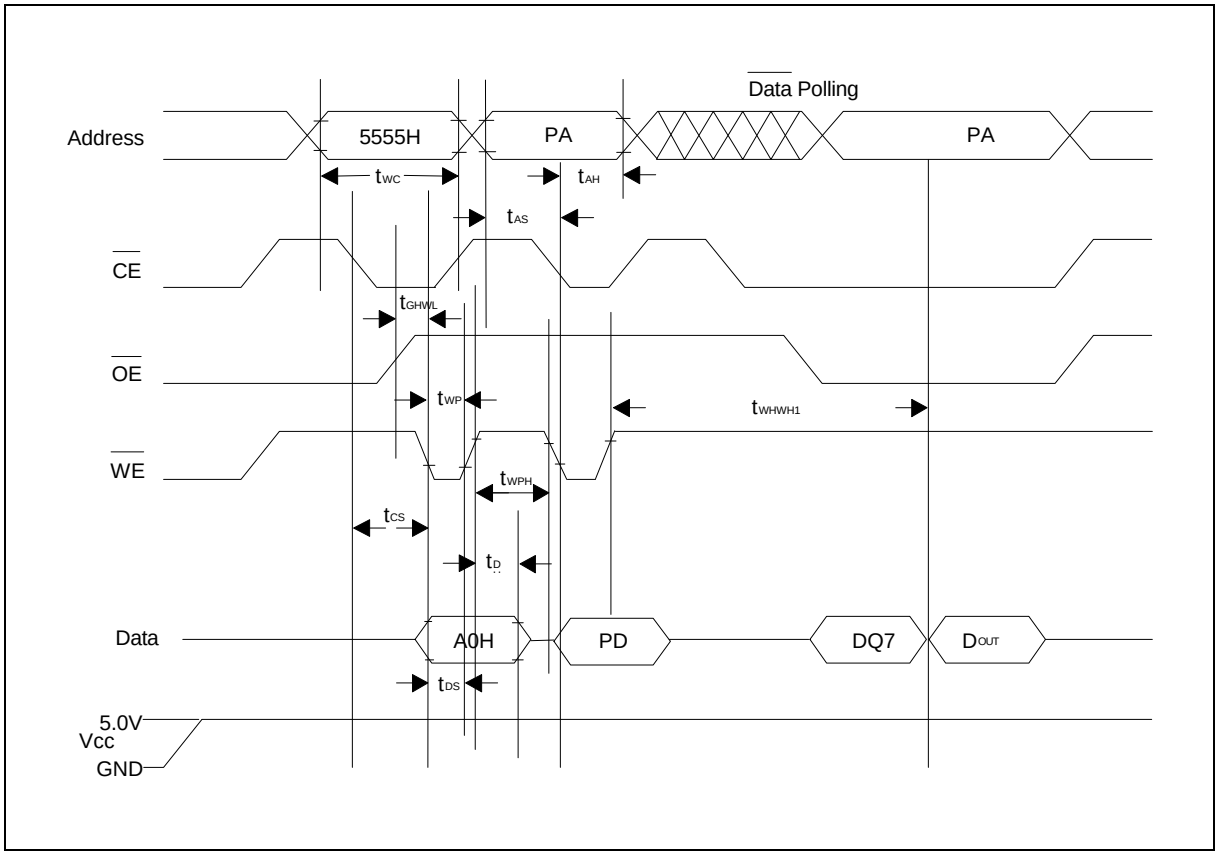


Figure 19. Alternate $\overline{CE}$ Controlled Program Operation Timings

Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at $\overline{BYTE}$ address.
3. /DQ7 is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.
6. These waveforms are for the x16 mode.

Erase and Programming Performance

PARAMETER	LIMITS			UNIT
	MIN.	TYP.	MAX.	
Sector Erase Time		0.33	15	sec
Chip Erase Time		2.4	120	sec
Byte Programming Time		16	400	us
Chip Programming Time		8	200	sec
Erase/Program Cycles	10,000	100,000		cycles

Latch Up Characteristics

PARAMETER	MIN.	MAX.
Input Voltage with respect to Vss on all I/O pins	-1.0V	Vcc + 1.0V
Vcc Current	-100 mA	+ 100 mA

Note: Includes all pins except Vcc. Test conditions: Vcc = 5.0V, one pin at a time.

CAPACITANCE

TSOP Pin

PARAMETER	SYMBOL	TEST SETUP	TYP.	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0	6	7.5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	8.5	12	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	8	10	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°, f = 1.0 MHz.

SOP Pin

PARAMETER	SYMBOL	TEST SETUP	TYP.	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0	6	7.5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	8.5	12	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	8	10	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions TA = 25°, f = 1.0 MHz.

Data Retention

PARAMETER	TEST CONDITIONS	MIN.	UNIT
Minimum Pattern Data Retention Time	150°	10	Years
Minimum Pattern Data Retention Time	125°	20	Years

ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	BOOT BLOCK	PACKAGE	CYCLING (MIN.)	TEMPERATURE RANGE
29F400T-90PC	90	60	Top	44SOP	10,000	0°C - 70°C
29F400T-12PC	120	60	Top	44SOP	10,000	0°C - 70°C
29F400T-90TC	90	60	Top	48TSOP	10,000	0°C - 70°C
29F400T-12TC	120	60	Top	48TSOP	10,000	0°C - 70°C
29F400B-90PC	90	60	Bottom	44SOP	10,000	0°C - 70°C
29F400B-12PC	120	60	Bottom	44SOP	10,000	0°C - 70°C
29F400B-90TC	90	60	Bottom	48TSOP	10,000	0°C - 70°C
29F400B-12TC	120	60	Bottom	48TSOP	10,000	0°C - 70°C
29F400T-90PI	90	60	Top	44SOP	10,000	-40°C - 85°C
29F400T-12PI	120	60	Top	44SOP	10,000	-40°C - 85°C
29F400T-90TI	90	60	Top	48TSOP	10,000	-40°C - 85°C
29F400T-12TI	120	60	Top	48TSOP	10,000	-40°C - 85°C
29F400B-90PI	90	60	Bottom	44SOP	10,000	-40°C - 85°C
29F400B-12PI	120	60	Bottom	44SOP	10,000	-40°C - 85°C
29F400B-90TI	90	60	Bottom	48TSOP	10,000	-40°C - 85°C
29F400B-12TI	120	60	Bottom	48TSOP	10,000	-40°C - 85°C

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.
3. Typical Program/Erase Cycle is 100,000.

APPENDIX A:

Compatibility to AMD's AMD29F400B:

The device is essentially fully functional compatible to the AMD29F400B except for three issues:

1. During Erase Suspend
2. DQ2 Status Flag
3. Command Address Subset

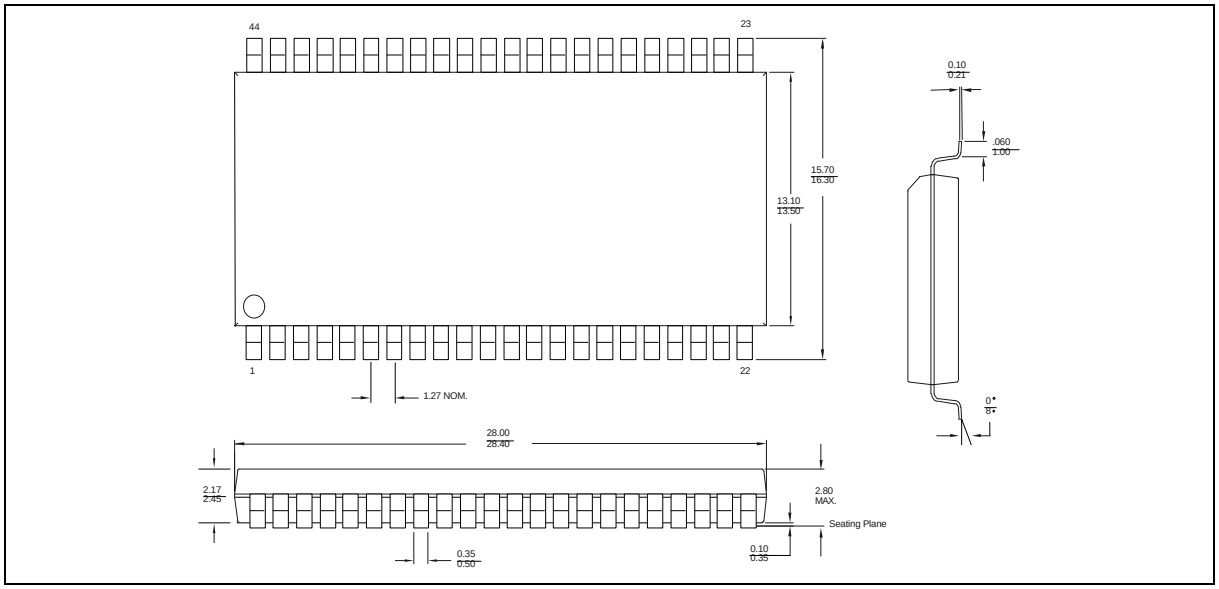
During Erase Suspend, the device can only read data in the memory-- not Program or execute an Auto Command like the AMD29400B. Also, the DQ2 Flag is not available. This flag is used to determine during multiple or single sector erase whether a sector has been selected for erase. DQ2 can only be used during and embedded sector erase operation or during erase suspend.

In the AMD device, commands do not require address pin A15, A14, A13, A12, A11 to be forced during the command sequence. This makes their device slighly easier to inadvertently create a command and cause a program, erase or malfunction. The advantage of reducing the address to a subset is to simplify the hardware interface in systems where control signals are limited in number. The 29F400B reduces the interface requirement by 4 signals. However if the full address is supplied (i.e.2AAAH and 5555H) by the host system, there will be no incompatibility using either device.

PACKAGE DIMENSIONS

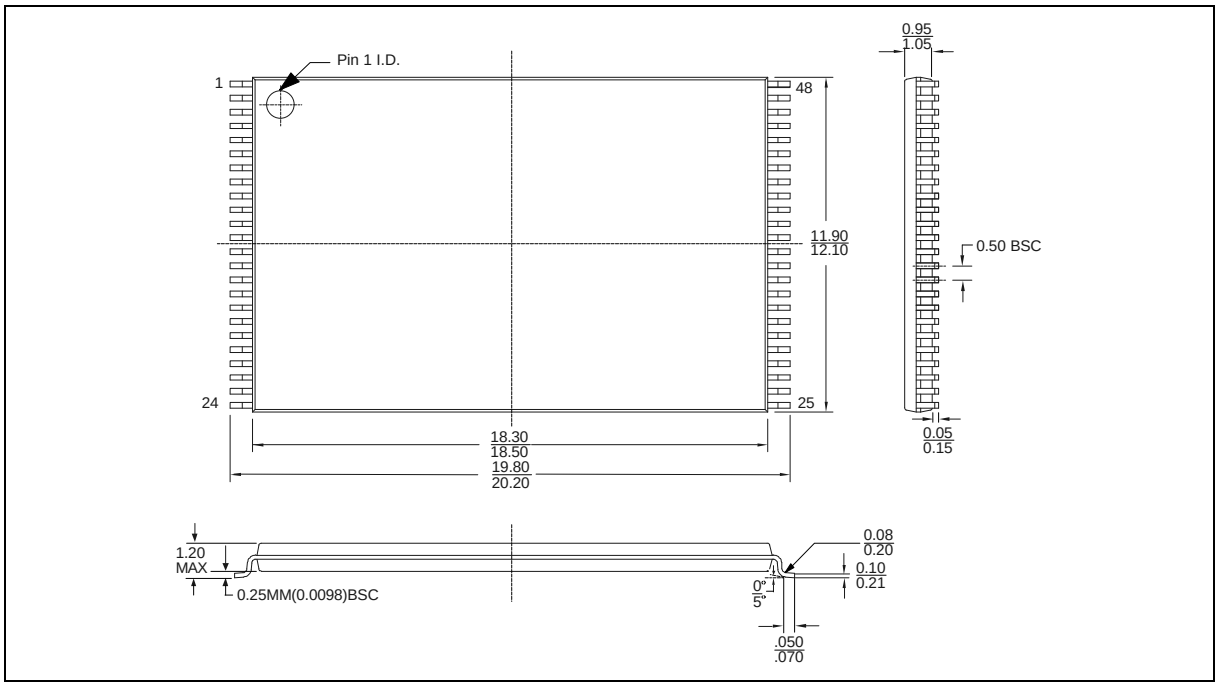
PSOP44

44-pin Small Outline Package (measured in millimeters)



TSOP48

48-Pin Standard Thin Small Outline Package (measured in millimeters)



VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	May. 1999	-	Initial Issued

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