

Synchronization signal processor for high definition displays

BA7078S

The BA7078S is a synchronization signal processing LSI chip designed for multiscan high-definition displays. It generates a synchronization signal and clamp pulse for three types of input signals: separate synchronization, composite synchronization, and synchronization on video.

●Applications

CRT displays

●Features

- 1) Operates on a single 5V power supply, with low power consumption.
- 2) Synchronization signal existence and polarity detection output.
- 3) Adjustable clamp pulse width, allowing for the selection of front or back editing.
- 4) Vertical synchronization separation is based on horizontal frequency tracking, for separation starting at 1H.
- 5) Minimal attached components.

●Absolute maximum ratings (Ta = 25°C)

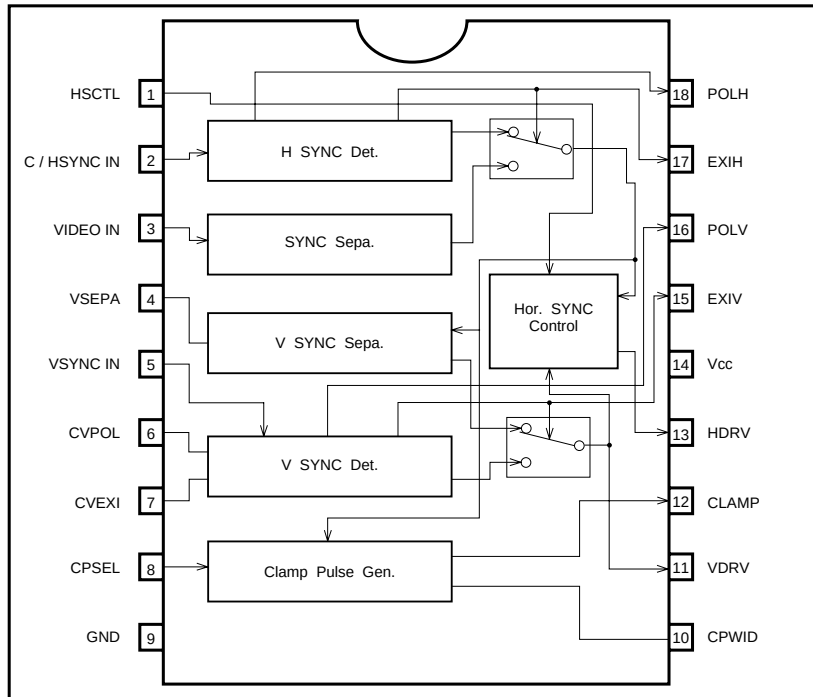
Parameter	Symbol	Limits	Unit
Power supply voltage	V _{CC}	7.0	V
Power dissipation	P _d	600	mW
Operating temperature	T _{opr}	– 25 ~ + 75	°C
Storage temperature	T _{stg}	– 55 ~ + 125	°C

* Reduced by 6mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V _{CC}	4.5	5.0	5.5	V

●Block diagram



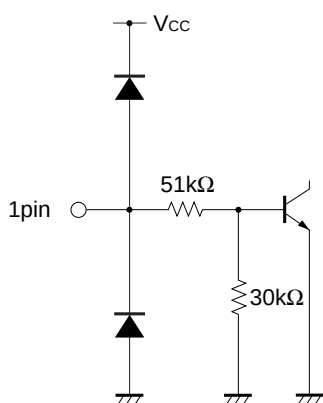
● Pin descriptions

Pin No.	Pin name	Function	
1	HSCTL	HDRV output	Used to select whether to output the VDRV section of the HDRV output signal. High: VDRV section of HDRV is output Low: VDRV section of HDRV is not output
2	CHSYNC IN	Composite sync / H SYNC input	Inputs either the composite synchronization signal or the horizontal synchronization signal. Input is clamped, and is initiated by capacitor coupling.
3	VIDEO IN	SYNC ON VIDEO input	Inputs the SYNC ON VIDEO signal (green). Input is sink chip clamped. Input is initiated by capacitor coupling.
4	VSEPA	f-V conversion	Converts the horizontal synchronization signal frequency into a voltage. The voltage generated is proportional to the frequency of the horizontal synchronization signal. Attach a 0.56μF capacitor between the ground pins.
5	VSIN	V SYNC input	Inputs the vertical synchronization signal.
6	CVPOL	Vertical polarity integration	Integrates the vertical synchronization signal polarity detection circuit. Attach a 1.5μF capacitor between this pin and the ground.
7	CVEXI	Vertical existence integration	Integrates the vertical synchronization signal existence detection circuit. Attach a 1μF capacitor between this pin and the ground.
8	CPSEL	Setting the clamp position	Used to set the clamp pulse generation position to either the front or back edge of HSYNC High: The front edge is the generation position Open: Composite / H SYNC IN: The front edge is the generation position VIDEO IN: The back edge is the generation position Low: The back edge is the generation position
9	GND	Ground	—
10	CPWID	Setting the clamp pulse width	Sets the clamp pulse width according to the attached time constant. Attach a resistor between this pin and Vcc, and a capacitor between this pin and GND. When R = 3.9kΩ and C = 100pF, pulse width is approximately 400 ns. Set the resistor to register an abnormality at 1kΩ.
11	VDRV	VDRV output	Outputs the vertical synchronization signal. The output signal has positive polarity.
12	CLAMP	Clamp output	Outputs the clamp pulse generated from the vertical synchronization signal. The output signal has a positive polarity.
13	HDRV	HDRV output	Outputs the clamp pulse generated from the horizontal synchronization signal. The output signal has positive polarity.
14	Vcc	Power supply	—

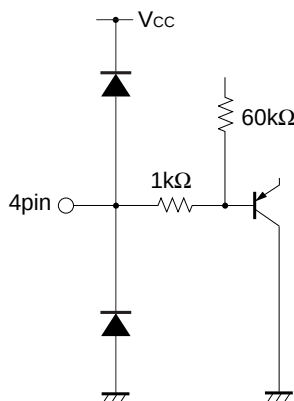
Pin No.	Pin name	Function	
15	EXIV	Vertical existence output	Indicates whether the vertical synchronization signal exists. For the output logic, refer to the separate table.
16	POLV	Vertical polarity output	Indicates the polarity of the vertical synchronization signal. For the output logic, refer to the separate table.
17	EXIH	Horizontal existence output	Indicates whether the horizontal synchronization signal exists. For the output logic, refer to the separate table.
18	POLH	Horizontal polarity output	Indicates the polarity of the horizontal synchronization signal. For the output logic, refer to the separate table.

● Input / output circuits

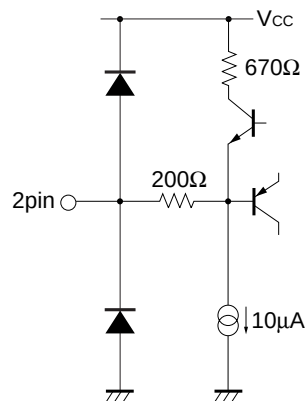
HSCTL



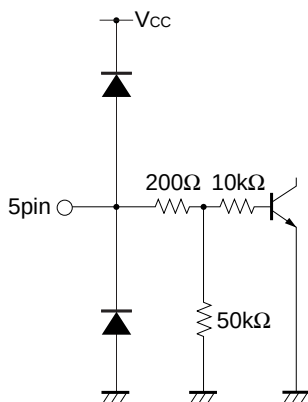
VSEPA



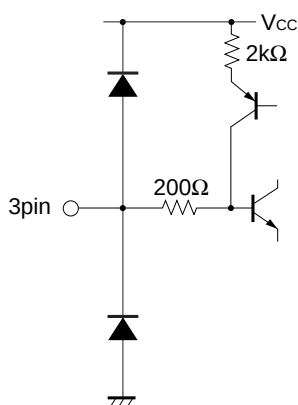
CHSYNC IN



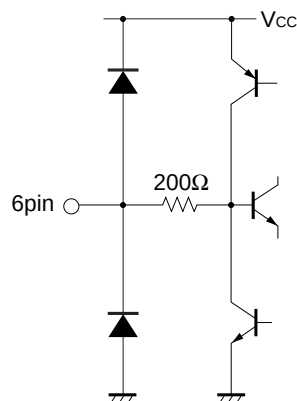
VSYNC IN



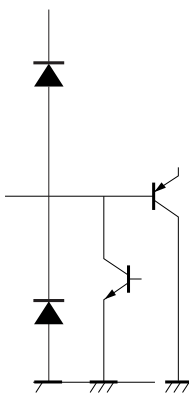
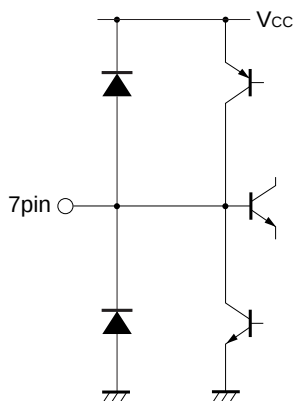
VIDEO IN



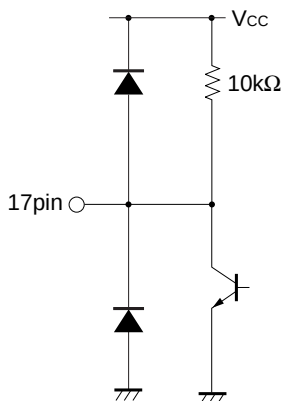
CVPOL



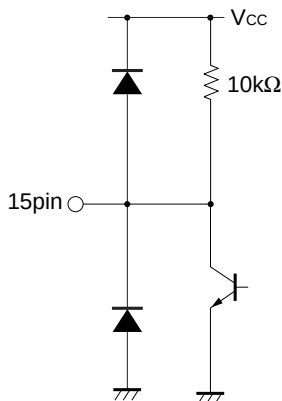
CVEXI



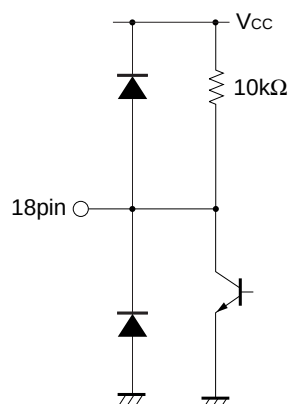
EXIH



EXIV



POLH



●Electrical characteristics (unless otherwise noted, $V_{CC} = 5V$, $T_a = 25^\circ C$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply voltage	V_{CC}	4.5	5.0	5.5	V	
Quiescent current	I_{CC}	21	30	39	mA	
VDRV output voltage (high)	V_{VDH}	4.5	5.0	—	V	
VDRV output voltage (low)	V_{VDL}	—	0.2	0.5	V	
VDRV output current (low)	I_{VDL}	8	—	—	mA	
VDRV rising delay time	t_{rdVD}	—	280	450	ns	VSYNC IN
HDRV output voltage (high)	V_{HDH}	4.5	5.0	—	V	
HDRV output voltage (low)	V_{HDL}	—	0.2	0.5	V	
HDRV output current (low)	I_{HDL}	8	—	—	mA	
HDRV rising delay time (1)	$trdHD1$	—	65	115	ns	CHSYNC IN
HDRV rising delay time (2)	$trdHD2$	—	95	145	ns	VIDEO IN
CLAMP output voltage (high)	V_{CPH}	4.5	5.0	—	V	
CLAMP output voltage (low)	V_{CPL}	—	0.2	0.5	V	
CLAMP output current (low)	I_{CPL}	8	—	—	mA	
CLAMP rising delay time (1)	$trdCP1$	—	75	125	ns	front edge
CLAMP rising delay time (2)	$trdCP2$	—	95	145	ns	back edge
Synchronization detection output voltage (high)	V_{DH}	4.5	5.0	—	V	
Synchronization detection output voltage (low)	V_{DL}	—	0.2	0.5	V	
Synchronization detection output current (low)	I_{DL}	3	—	—	mA	
Synchronization detection output impedance	Z_{oD}	7	10	13	kΩ	
Minimum synchronization separation level	$V_{SMin.}$	—	—	0.2	V_{P-P}	
HSCTL high level threshold voltage	V_{tHSH}	2.5	—	—	V	
HSCTL low level threshold voltage	V_{tHSL}	—	—	1.5	V	
CPSEL high level threshold voltage	V_{tCPH}	3.8	—	—	V	
CPSEL low level threshold voltage	V_{tCPL}	—	—	1.2	V	

● Measurement circuit

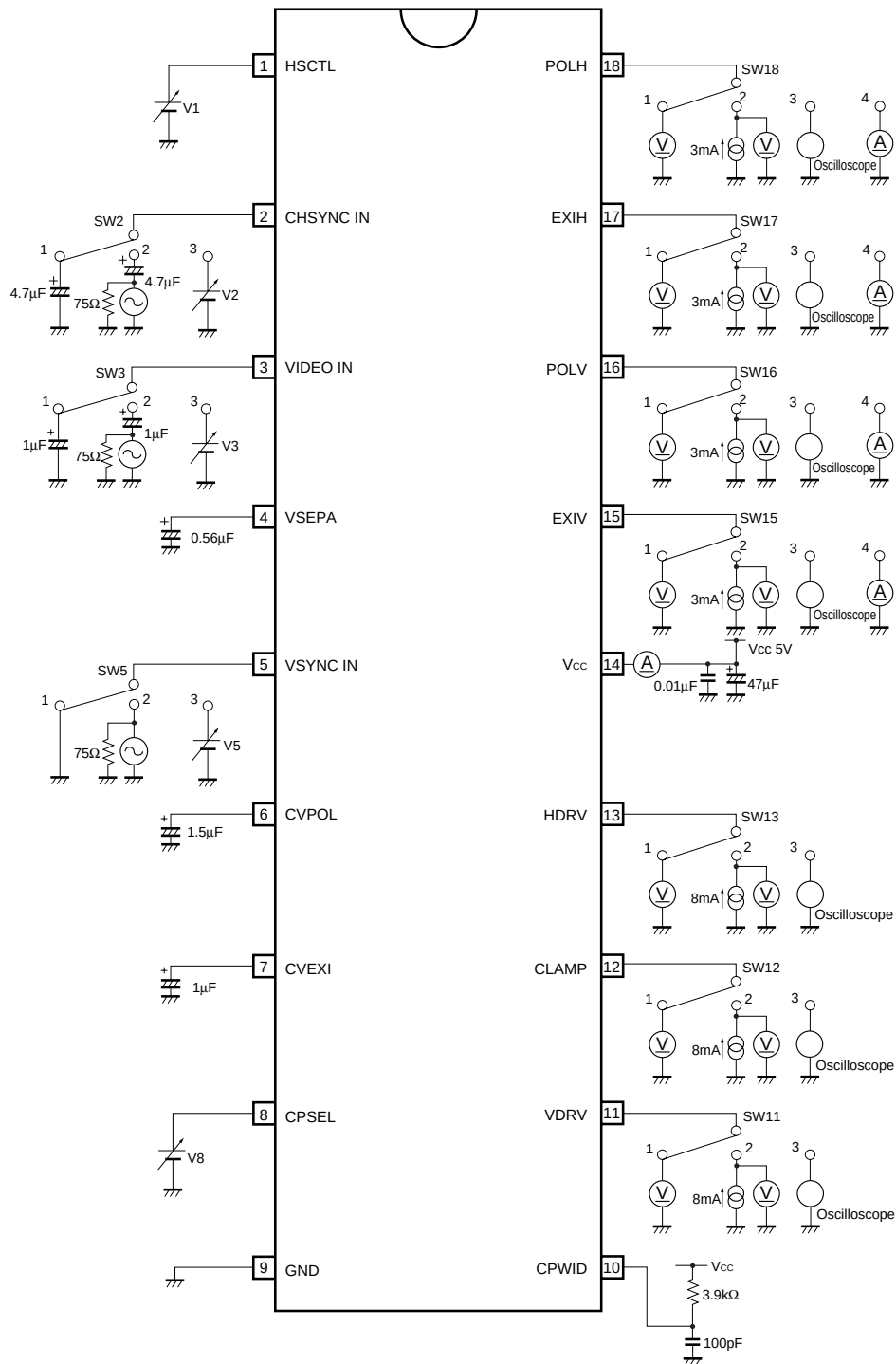


Fig. 1

● Conditions for measurement of electrical characteristics

Parameter	Switch condition										
	2	3	5	11	12	13	15	16	17	18	
Quiescent current	1	1	1	1	1	1	1	1	1	1	
VDRV output voltage (high)	1	1	3	1	1	1	1	1	1	1	
VDRV output voltage (low)	1	1	3	1	1	1	1	1	1	1	
VDRV output current (low)	1	1	3	2	1	1	1	1	1	1	
VDRV rising delay time	1	1	2	3	1	1	1	1	1	1	
HDRV output voltage (high)	3	1	1	1	1	1	1	1	1	1	
HDRV output voltage (low)	3	1	1	1	1	1	1	1	1	1	
HDRV output current (low)	3	1	1	1	1	2	1	1	1	1	
HDRV rising delay time (1)	2	1	1	1	1	3	1	1	1	1	
HDRV rising delay time (2)	1	2	1	1	1	3	1	1	1	1	
CLAMP output voltage (high)	2	1	1	1	3	1	1	1	1	1	
CLAMP output voltage (low)	2	1	1	1	3	1	1	1	1	1	
CLAMP output current (low)	3	1	1	1	2	1	1	1	1	1	
CLAMP rising delay time (1)	2	1	1	1	3	1	1	1	1	1	
CLAMP rising delay time (2)	1	2	1	1	3	1	1	1	1	1	
POLH output voltage (high)	2	1	1	1	1	1	1	1	1	1	
POLH output voltage (low)	2	1	1	1	1	1	1	1	1	1	
POLH output current (low)	3	1	1	1	1	1	1	1	1	2	
POLH output impedance	3	1	1	1	1	1	1	1	1	4	
EXIH output voltage (high)	2	1	1	1	1	1	1	1	1	1	
EXIH output voltage (low)	1	1	1	1	1	1	1	1	1	1	
EXIH output current (low)	3	1	1	1	1	1	1	1	2	1	
EXIH output impedance	3	1	1	1	1	1	1	1	4	1	
POLV output voltage (high)	1	1	2	1	1	1	1	1	1	1	
POLV output voltage (low)	1	1	2	1	1	1	1	1	1	1	
POLV output current (low)	1	1	3	1	1	1	1	2	1	1	
POLV output impedance	1	1	3	1	1	1	1	4	1	1	
EXIV output voltage (high)	1	1	2	1	1	1	1	1	1	1	
EXIV output voltage (low)	1	1	1	1	1	1	1	1	1	1	
EXIV output current (low)	1	1	3	1	1	1	2	1	1	1	
EXIV output impedance	1	1	3	1	1	1	4	1	1	1	
Minimum synchronization separation level	1	2	1	1	1	3	1	1	1	1	
HSCTL high level threshold voltage	2	1	2	1	1	3	1	1	1	1	
HSCTL low level threshold voltage	2	1	2	1	1	3	1	1	1	1	
CPSEL high level threshold voltage	1	2	1	1	3	3	1	1	1	1	
CPSEL low level threshold voltage	2	1	1	1	3	3	1	1	1	1	

● Application example

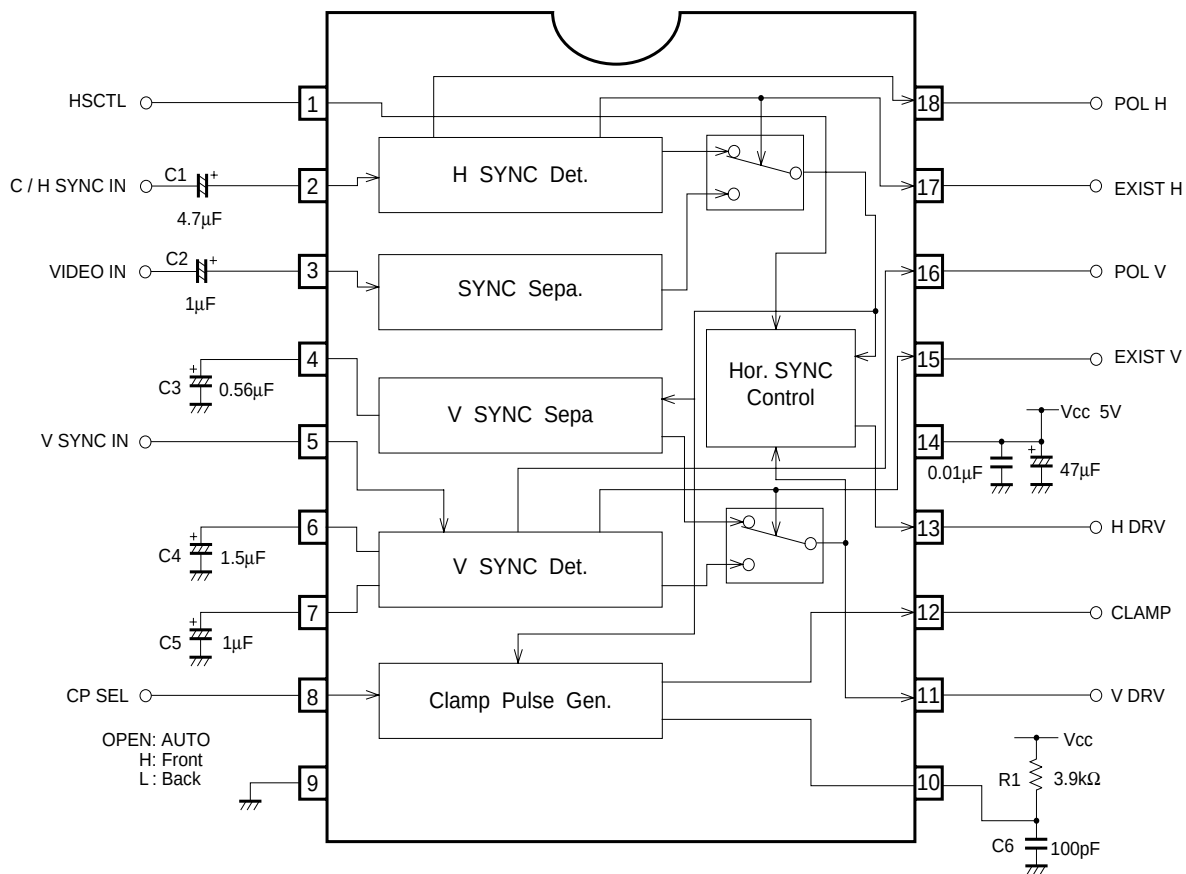


Fig. 2

● Attached components

- C1: 47 μ F Coupling capacitor for C / H SYNC IN
A low capacitance increases the size of the input pin waveform's sag.
- C2: 1 μ F Coupling capacitor for VIDEO IN
A low capacitance increases the size of the input pin waveform's sag.
- C3: 0.56 μ F Conversion capacitor for f-V
A low capacitance increases the size of the ripple of the f-V conversion voltage. A large capacitance is not a problem, but will delay the reaction speed.
- C4: 1.5 μ F Capacitor for POLH (detection of the vertical synchronization signal's polarity)
The minimum capacitance is determined as follows:
The internal hysteresis comparator does not react when the duty of minimum frequency synchronization (fV = 40Hz, T = 25ms) is 50%.
 $C_{Min.} = 30\mu * T[F]$
A large capacitance is not a problem, but will delay the reaction speed.
- C5: 1 μ F Capacitor for EXIH (detection of the vertical synchronization signal's existence)
The minimum capacitance is determined as follows:
The internal hysteresis comparator does not react at the minimum frequency synchronization (fV = 40Hz, T = 25ms)
 $C_{Min.} = 16\mu * T[F]$
A large capacitance is not a problem, but will delay the reaction speed.
- C6: 100pF Constant for setting the clamp pulse width
- R1: 3.9k Ω A low resistance results in a narrow clamp pulse width. Set no lower than 1k Ω .

●Electrical characteristic curves

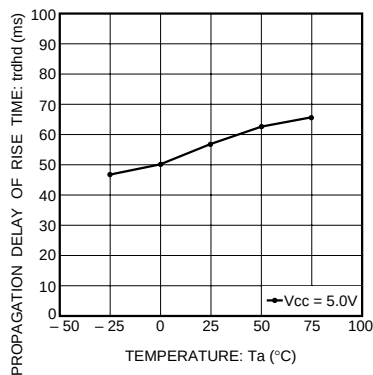


Fig. 3 C / HSYNC IN-HDRV
Rising delay time vs.
temperature

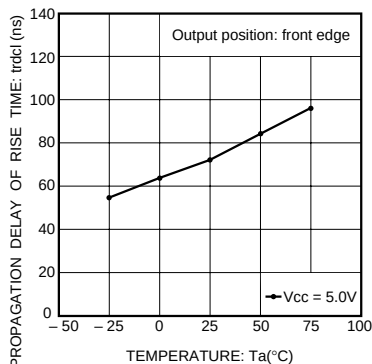


Fig. 4 C / HSYNC IN-CLAMP
Rising delay time vs.
temperature

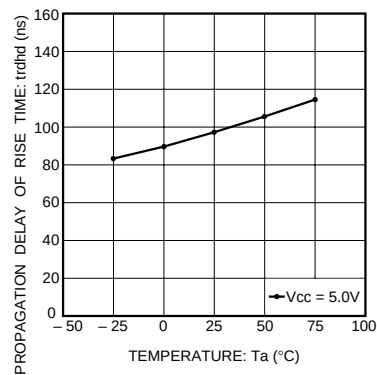


Fig. 5 VIDEO IN-HDRV
Rising delay time vs.
temperature

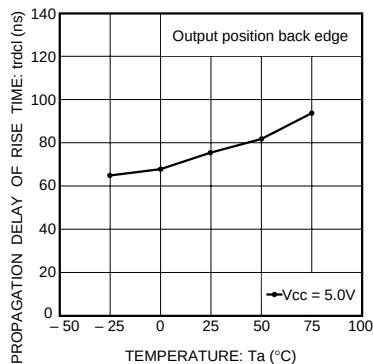


Fig. 6 VIDEO IN-CLAMP
Rising delay time vs.
temperature

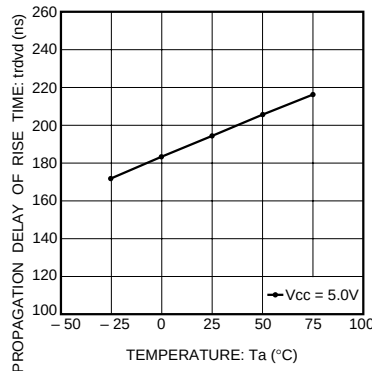


Fig. 7 VSYNC IN-HDRV
Rising delay time vs.
temperature

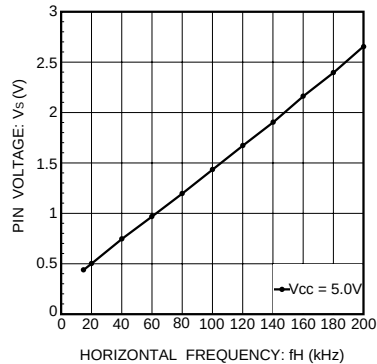


Fig. 8 VSEPA horizontal
frequency vs.
pin voltage

●External dimensions (Units: mm)

