# LAMBDA ADVANCED ANALOG INC.

# ATR2800S Series
## Hybrid - High Reliability DC/DC Converters

### DESCRIPTION

The ATR2800S Series of DC/DC converters feature high power density and an extended temperature range for use in military and industrial applications. Designed to MIL-STD-704 input requirements, these devices have nominal 28$V_{DC}$ inputs with +5v, +12v and +15v single outputs to satisfy a wide range of requirements. The circuit design incorporates a pulse width modulated single forward topology operating in the feed-forward mode at a nominal switching frequency of 550 KHz. Input to output isolation is achieved through the use of transformers in the forward and feedback circuits.

The advanced feedback design provides fast loop response for superior line and load transient characteristics and offers greater reliability and radiation tolerance than devices incorporating optical feedback circuits.

Three standard temperature grades are offered with screening options. Refer to Part Number section. They can be provided in a standard plug-in package for PC mounting or in a flanged package for more severe environments.

These converters are manufactured in a facility certified to MIL-PRF-38534. All processes used to manufacture these converters have been qualified to enable Lambda Advanced Analog to deliver compliant devices. Four screening grades are available to satisfy a wide range of requirements. The CH grade converters are fully compliant to MIL-PRF-38534 class H. The HB grade converters are processed to full class H screening but do not have class H element evaluation as required by MIL-PRF-38534. Both grades are fully tested and operate over the full military temperature range without derating of output power. The ES version is a full temperature device without the full class H screening or element evaluation. The non-suffix device is a low cost limited temperature range option. Variations in electrical, mechanical and screening can be accommodated. Extensive computer simulation using complex modeling enables rapid design modification to be provided. Contact Lambda Advanced Analog with specific requirements.

### FEATURES

- 16-40$V_{DC}$ input range (28$V_{DC}$ nominal)
- 5V, 12V and 15V outputs available
- Indefinite short circuit and overload protection
- Up to 35W/$in^3$ power density
- 30 watt output power models
- Fast loop response for superior transient characteristics
- Operating temperature range from -55°C to + 125°C
- Popular industry standard pin-out
- Resistance seam welded case for superior long term hermeticity
- Ceramic feed-thru pins
- External Synchronization
- Efficiencies up to 84%
- Shutdown from external signal
- Military screening

ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Input Voltage | -0.5V to 50V |
| Soldering Temperature | 300°C for 10 seconds |
| Case Temperature | Operating-55°C to +125°C<br>Storage -65°C to +135°C |

**TABLE I. Electrical Performance Characteristics**

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{IN}$ = 28 V dc ±5%, $C_L$ = 0 unless otherwise specified | Group A subgroups | Device types | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Output voltage | $V_{OUT}$ | $I_{OUT}$ = 0 | 1 | 01 | 4.95 | 5.05 | V |
| | | | 2,3 | | 4.90 | 5.10 | |
| Output current 1/ | $I_{OUT}$ | $V_{IN}$ = 16, 28, and 40 V dc | 1,2,3 | 01 | | 6000 | mA |
| Output ripple voltage 2/ | $V_{RIP}$ | $V_{IN}$ = 16, 28, and 40 V dc<br>B.W. = 20 Hz to 2 MHz | 1,2,3 | 01 | | 60 | mV p-p |
| Line regulation 3/ | $VR_{LINE}$ | $V_{IN}$ = 16, 28, and 40 V dc<br>$I_{OUT}$ = 0, 3000, and 6000 mA | 1 | 01 | | ±20 | mV |
| | | | 2,3 | | | ±30 | |
| Load regulation 3/ | $VR_{LOAD}$ | $V_{IN}$ = 16, 28, and 40 V dc<br>$I_{OUT}$ = 0, 3000, and 6000 mA | 1,2,3 | 01 | | ±50 | mV |
| Input current | $I_{IN}$ | $I_{OUT}$ = 0, inhibit (pin 2) tied to input return (pin 10) | 1,2,3 | 01 | | 18 | mA |
| | | $I_{OUT}$ = 0, inhibit (pin 2) = open | | | | 50 | |
| Input ripple current 2/ | $I_{RIP}$ | $I_{OUT}$ = 6000 mA<br>B.W. = 20 Hz to 2 MHz | 1,2,3 | 01 | | 50 | mA p-p |
| Efficiency | $E_{FF}$ | $I_{OUT}$ = 6000 mA | 1 | 01 | 76 | | % |
| | | | 2,3 | | 72 | | |
| Isolation | ISO | Input to output or any pin to case (except pin 8) at500 V dc, $T_C$ = +25°C | 1 | 01 | 100 | | MΩ |
| Capacitive load 4/ 5/ | $C_L$ | No effect on dc performance<br>$T_C$ = +25°C | 4 | 01 | | 500 | µf |
| Power dissipation load fault | $P_D$ | Overload, $T_C$ = +25°C 6/ | 1 | 01 | | 12 | W |
| | | Short circuit | 1,2,3 | | | 9 | |

See footnotes at end of table.

**TABLE I. Electrical Performance Characteristics - Continued**

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{IN}$ = 28 V dc ±5%, $C_L$ = 0 unless otherwise specified | Group A Subgroups | Device types | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Switching frequency | $F_S$ | $I_{OUT}$ = 6000 mA | 4,5,6 | 01 | 500 | 600 | KHz |
| Sync frequency range | $F_{sync}$ | $I_{OUT}$ = 6000 mA | 4,5,6 | 01 | 500 | 700 | KHz |
| Output response to step transient load changes 7/ | $VO_{TLOAD}$ | 3000 mA to/from 6000 mA | 4,5,6 | 01 | -500 | +500 | mV pk |
| | | 500 mA to/from 3000 mA | 4,5,6 | | -500 | +500 | |
| Recovery time step transient load changes 7/ 8/ | $TT_{LOAD}$ | 3000 mA to/from 6000 mA | 4 | 01 | | 100 | µs |
| | | | 5,6 | | | 200 | |
| | | 500 mA to/from 3000 mA | 4 | | | 100 | |
| | | | 5,6 | | | 200 | |
| Output response to transient step line changes 5/ 9/ | $VO_{TLINE}$ | Input step 16 V to/from 40 V dc, $I_{OUT}$ = 6000 mA | 4,5,6 | 01 | | ±500 | mV pk |
| Recovery time transient step line changes 5/ 8/ 9/ | $TT_{LINE}$ | Input step 16 V to/from 40 V dc, $I_{OUT}$ = 6000 mA | 4,5,6 | 01 | | 10 | ms |
| Turn on overshoot | $VTon_{os}$ | $I_{OUT}$ = 0 and 6000 mA | 4,5,6 | 01 | | 500 | mV pk |
| Turn on delay 10/ | $Ton_D$ | $I_{OUT}$ = 0 and 6000 mA | 4,5,6 | 01 | | 25 | ms |
| Load fault recovery 5/10/ | $Tr_{LF}$ | | 4,5,6 | 01 | | 25 | ms |

**Notes:**

1/ Parameter guaranteed by line and load regulation tests.
2/ Bandwidth guaranteed by design. Tested for 20 KHz to 2 MHz.
3/ Output voltage measured at load with remote sense leads connected across load.
4/ Capacitive load may be any value from 0 to the maximum limit without compromising dc performance. A capacitive load in excess of the maximum limit will not disturb loop stability but may interfere with the operation of the load fault detection circuitry, appearing as a short circuit during turn on.
5/ Parameter shall be tested as part of design characterization and after design or process changes. Thereafter parameters shall be guaranteed to the limits specified in Table II.
6/ An overload is that condition with a load in excess of the rated load but less than that necessary to trigger the short circuit protection and is the condition of maximum power dissipation.
7/ Load step transition time between 2 and 10 microseconds.
8/ Recovery time is measured from the initiation of the transient to where $V_{OUT}$ has returned to within ±1 percent of $V_{OUT}$ at 50 percent load.
9/ Input step transition time between 2 and 10 microseconds.
10/ Turn on delay time measurement is for either a step application of power at the input or the removal of a ground signal from the inhibit pin (pin 2) while power is applied to the input.

ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Input Voltage | -0.5V to 180V |
| Soldering Temperature | 300°C for 10 seconds |
| Case Temperature | Operating-55°C to +125°C<br>Storage -65°C to +135°C |

**TABLE II. Electrical Performance Characteristics**

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{IN}$ = 28 V dc ±5%, $C_L$ = 0 unless otherwise specified | Group A subgroups | Device types | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Output voltage | $V_{OUT}$ | $I_{OUT}$ = 0 | 1 | 01 | 11.88 | 12.12 | V |
| | | | 2,3 | | 11.70 | 12.30 | |
| Output current 1/ | $I_{OUT}$ | $V_{IN}$ = 16, 28, and 40 V dc | 1,2,3 | 01 | | 2500 | mA |
| Output ripple voltage 2/ | $V_{RIP}$ | $V_{IN}$ = 16, 28, and 40 V dc<br>B.W. = 20 Hz to 2 MHz | 1,2,3 | 01 | | 60 | mV p-p |
| Line regulation 3/ | $VR_{LINE}$ | $V_{IN}$ = 16, 28, and 40 V dc<br>$I_{OUT}$ = 0, 1250, and 2500 mA | 1 | 01 | | ±30 | mV |
| | | | 2,3 | | | ±60 | |
| Load regulation 3/ | $VR_{LOAD}$ | $V_{IN}$ = 16, 28, and 40 V dc<br>$I_{OUT}$ = 0, 1250, and 2500 mA | 1 | 01 | | ±60 | mV |
| | | | 2,3 | | | ±120 | |
| Input current | $I_{IN}$ | $I_{OUT}$ = 0, inhibit (pin 2) tied to input return (pin 10) | 1,2,3 | 01 | | 18 | mA |
| | | $I_{OUT}$ = 0, inhibit (pin 2) = open | 1 | | | 50 | |
| | | | 2,3 | | | 75 | |
| Input ripple current 2/ | $I_{RIP}$ | $I_{OUT}$ = 2500 mA<br>B.W. = 20 Hz to 2 MHz | 1,2,3 | 01 | | 50 | mA p-p |
| Efficiency | $E_{FF}$ | $I_{OUT}$ = 2500 mA | 1 | 01 | 80 | | % |
| | | | 2,3 | | 75 | | |
| Isolation | ISO | Input to output or any pin to case (except pin 8) at 500 V dc, $T_{C = +25°C}$ | 1 | 01 | 100 | | MΩ |
| Capacitive load 4/ 5/ | $C_L$ | No effect on dc performance<br>$T_{C = +25°C}$ | 4 | 01 | | 500 | µf |
| Power dissipation load fault | $P_D$ | Overload, $T_C$ = +25°C 6/ | 1 | 01 | | 12 | W |
| | | Short circuit | 1,2,3 | | | 9 | |

See footnotes at end of table.

**TABLE II. Electrical Performance Characteristics - Continued.**

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{IN}$ = 28 V dc ±5%, $C_L$ = 0 unless otherwise specified | Group A Subgroups | Device types | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Switching frequency | $F_S$ | $I_{OUT}$ = 2500 mA | 4,5,6 | 01 | 500 | 600 | KHz |
| Sync frequency range | $F_{sync}$ | $I_{OUT}$ = 2500 mA | 4,5,6 | 01 | 500 | 700 | KHz |
| Output response to step transient load changes 7/ | $VO_{TLOAD}$ | 1250 mA to/from 2500 mA | 4,5,6 | 01 | -800 | +800 | mV pk |
| | | 200 mA to/from 1250 mA | 4,5,6 | | -1000 | +1000 | |
| Recovery time step transient load changes 7/ 8/ | $TT_{LOAD}$ | 1250 mA to/from 2500 mA | 4 | 01 | | 100 | µs |
| | | | 5,6 | | | 200 | |
| | | 200 mA to/from 1250 mA | 4 | | | 100 | |
| | | | 5,6 | | | 200 | |
| Output response to transient step line changes 5/ 9/ | $VO_{TLINE}$ | Input step 16 V to/from 40 V dc, $I_{OUT}$ = 2500 mA | 4,5,6 | 01 | | ±1200 | mV pk |
| Recovery time transient step line changes 5/ 8/ 9/ | $TT_{LINE}$ | Input step 16 V to/from 40 V dc, $I_{OUT}$ = 2500 mA | 4,5,6 | 01 | | 10 | ms |
| Turn on overshoot | $VTon_{os}$ | $I_{OUT}$ = 0 and 2500 mA | 4,5,6 | 01 | | 800 | mV pk |
| Turn on delay 10/ | $Ton_D$ | $I_{OUT}$ = 0 and 2500 mA | 4,5,6 | 01 | | 25 | ms |
| Load fault recovery 5/ 10/ | $Tr_{LF}$ | | 4,5,6 | 01 | | 25 | ms |

**Notes:**

1/ Parameter guaranteed by line and load regulation tests.
2/ Bandwidth guaranteed by design. Tested for 20 KHz to 2 MHz.
3/ Output voltage measured at load with remote sense leads connected across load.
4/ Capacitive load may be any value from 0 to the maximum limit without compromising dc performance. A capacitive load in excess of the maximum limit will not disturb loop stability but may interfere with the operation of the load fault detection circuitry, appearing as a short circuit during turn on.
5/ Parameter shall be tested as part of design characterization and after design or process changes. Thereafter parameters shall be guaranteed to the limits specified in Table II.
6/ An overload is that condition with a load in excess of the rated load but less than that necessary to trigger the short circuit protection and is the condition of maximum power dissipation.
7/ Load step transition time between 2 and 10 microseconds.
8/ Recovery time is measured from the initiation of the transient to where $V_{OUT}$ has returned to within ±1 percent of $V_{OUT}$ at 50 percent load.
9/ Input step transition time between 2 and 10 microseconds.
10/ Turn on delay time measurement is for either a step application of power at the input or the removal of a ground signal from the inhibit pin (pin 2) while power is applied to the input.

ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Input Voltage | -0.5V to 50V |
| Soldering Temperature | 300°C for 10 seconds |
| Case Temperature | Operating-55°C to +125°C<br>Storage -65°C to +135°C |

**TABLE III. Electrical Performance Characteristics**

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{IN}$ = 28 V dc ±5%, $C_L$ = 0 unless otherwise specified | Group A subgroups | Device types | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Output voltage | $V_{OUT}$ | $I_{OUT}$ = 0 | 1 | 01 | ±14.85 | ±15.15 | V |
| | | | 2,3 | | ±14.60 | ±15.40 | |
| Output current 1/ | $I_{OUT}$ | $V_{IN}$ = 16, 28, and 40 V dc each output. | 1,2,3 | 01 | | 2000 | mA |
| Output ripple voltage 3/ | $V_{RIP}$ | $V_{IN}$ = 16, 28, and 40 V dc<br>B.W. = 20 Hz to 2 MHz | 1,2,3 | 01 | | ±75 | mV p-p |
| Line regulation 3/ | $VR_{LINE}$ | $V_{IN}$ = 16, 28, and 40 V dc<br>$I_{OUT}$ = 0, 1250, and 2500 mA | 1 | 01 | | ±35 | mV |
| | | | 2,3 | | | ±75 | |
| Load 3/ regulation | $VR_{LOAD}$ | $V_{IN}$ = 16, 28, and 40 V dc<br>$I_{OUT}$ = 0, 1250, and 2500 mA | 1 | 01 | | ±75 | mV |
| | | | 2,3 | | | ±150 | |
| Input current | $I_{IN}$ | $I_{OUT}$ = 0, inhibit (pin 2) tied to input return (pin 10) | 1,2,3 | 01 | | 18 | mA |
| | | $I_{OUT}$ = 0,<br>inhibit (pin 2) = open | 1 | | | 75 | |
| | | | 2,3 | | | 100 | |
| Input ripple current 2/ | $I_{RIP}$ | $I_{OUT}$ = 2500 mA<br>B.W. = 20 Hz to 2 MHz | 1,2,3 | 01 | | 50 | mA p-p |
| Efficiency 4/ | $E_{FF}$ | $I_{OUT}$ = 2500 mA | 1 | 01 | 79 | | % |
| | | | 2,3 | | 75 | | |
| Isolation | ISO | Input to output or any pin to case (except pin 7) at 500 V dc, $T_C$ = +25°C | 1 | 01 | 100 | | MΩ |
| Capacitive 4/ 5/ load | $C_L$ | No effect on dc performance, $T_{C = +25°C}$. Total for both outputs | 4 | 01 | | 500 | µf |
| Power dissipation load fault | $P_D$ | Overload, $T_C$ = +25°C 6/ | 1 | 01 | | 12 | W |
| | | Short circuit | 1,2,3 | | | 9 | |

See footnotes at end of table.

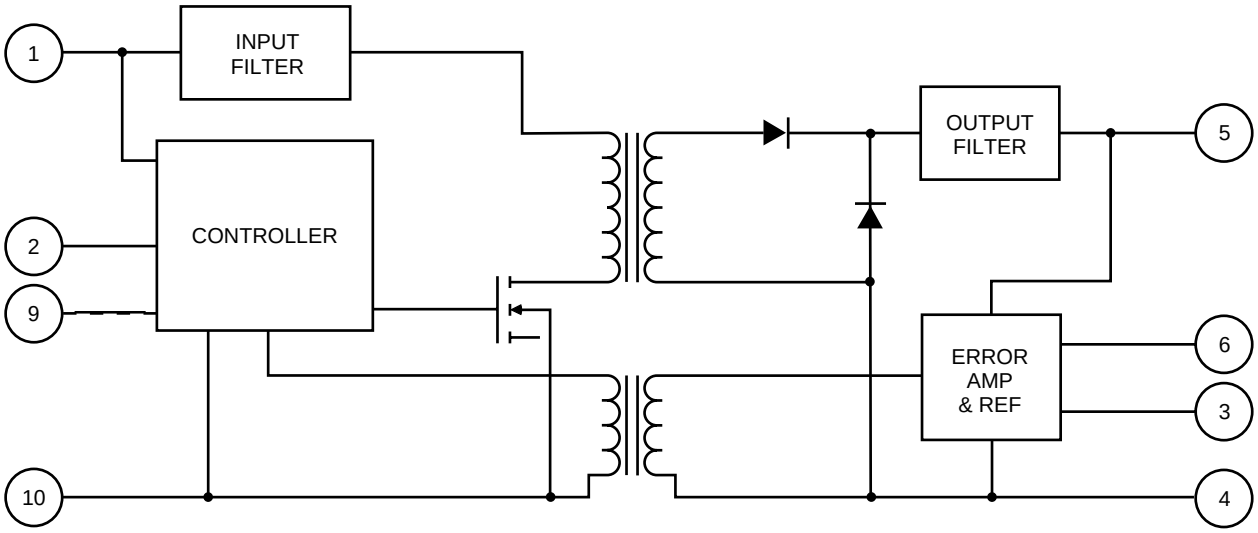
**TABLE III. Electrical Performance Characteristics - Continued.**

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{IN}$ = 28 V dc ±5%, $C_L$ = 0 unless otherwise specified | Group A Subgroups | Device types | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Switching frequency 4/ | $F_S$ | $I_{OUT}$ = 2500 mA | 4,5,6 | 01 | 500 | 600 | KHz |
| Sync frequency range | $F_{sync}$ | $I_{OUT}$ = 2500 mA | 4,5,6 | 01 | 500 | 700 | KHz |
| Output response to step transient load changes 7/ | $VO_{TLOAD}$ | 1000 mA to/from 2000 mA | 4,5,6 | 01 | -1000 | +1000 | mV pk |
| | | 167 mA to/from 1000 mA | 4,5,6 | | -1000 | +1000 | |
| Recovery time step transient load changes 7/ 8/ | $TT_{LOAD}$ | 1000 mA to/from 2000 mA | 4 | 01 | | 100 | µs |
| | | | 5,6 | | | 200 | |
| | | 167 mA to 1000 mA | 4 | | | 100 | |
| | | | 5,6 | | | 200 | |
| Output response to transient step line changes 5/ 9/ | $VO_{TLINE}$ | Input step 16 V to/from 40 V dc, $I_{OUT}$ = 2000 mA | 4,5,6 | 01 | | ±1500 | mV pk |
| Recovery time transient step line changes 5/ 8/ 9/ | $TT_{LINE}$ | Input step 16 V to/from 40 V dc, $I_{OUT}$ = 2500 mA | 4,5,6 | 01 | | 10 | ms |
| Turn on overshoot | $VTon_{os}$ | $I_{OUT}$ = 0 and 2000 mA | 4,5,6 | 01 | | 1000 | mV pk |
| Turn on delay 10/ | $Ton_D$ | $I_{OUT}$ = 0 and 2000 mA | 4,5,6 | 01 | | 25 | ms |
| Load fault recovery 5/ 10/ | $Tr_{LF}$ | | 4,5,6 | 01 | | 25 | ms |

**Notes:**

1/ Parameter guaranteed by line and load regulation tests.
2/ Up to 90 percent of full power is available from either output provided the total output does not exceed 30 watts.
3/ Bandwidth guaranteed by design. Tested for 20 KHz to 2 MHz.
4/ Load current split equally between $+V_{OUT}$ and $-V_{OUT}$.
5/ 3 watt load on output under test. 3 watt to 27 watt load change on other output.
6/ Capacitive load may be any value from 0 to the maximum limit without compromising dc performance. A capacitive load in excess of the maximum limit will not disturb loop stability but may interfere with the operation of the load fault detection circuitry, appearing as a short circuit during turn on.
7/ Parameter shall be tested as part of design characterization and after design or process changes. Thereafter parameters shall be guaranteed to the limits specified in Table III.
8/ An overload is that condition with a load in excess of the rated load but less than that necessary to trigger the short circuit protection and is the condition of maximum power dissipation.
9/ Load step transition time between 2 and 10 microseconds.
10/ Recovery time is measured from the initiation of the transient to where $V_{OUT}$ has returned to within ±1 percent of $V_{OUT}$ at 50 percent load.
11/ Input step transition time between 2 and 10 microseconds.
12/ Turn on delay time measurement is for either a step application of power at the input or the removal of a ground signal from the inhibit pin (pin 2) while power is applied to the input.

## BLOCK DIAGRAM




## APPLICATION INFORMATION

### Inhibit Function

Connecting the inhibit input (Pin 2) to input common (Pin 10) will cause the converter to shut down. It is recommended that the inhibit pin be driven by an open collector device capable of sinking at least 400µA of current. The open circuit voltage of the inhibit input is 11.5 ±1VDC.

**EMI Filter**

An optional EMI filter (AFC461) will reduce the input ripple current to levels below the limits imposed by MIL-STD-461 CEO3.

### Output Adjust

The output voltage of the ATR2800S can be adjusted upward by connecting Positive Output (Pin 5) and Positive Sense (Pin 6) as shown in Table 1.

| Resistance Pin 5 to 6 (Ω) | Output Voltage Increase (V) |
|---|---|
| 109 | 0.1 |
| 240 | 0.2 |
| 400 | 0.3 |
| 600 | 0.4 |
| 857 | 0.5 |
| 1200 | 0.6 |

*Table 1 Output adjustment resistor values for ATR2805S*

### Device Synchronization

Whenever multiple DC/DC converters are utilized in a single system, significant low frequency noise may be generated due to slight difference in the switching frequencies of the converters (beat frequency noise). Because of the low frequency nature of this noise (typically less than 10KHz), it is difficult to filter out and may interfere with proper operation of sensitive systems (communications, radar or telemetry). Lambda Advanced Analog provides synchronization of multiple ATR type converters to match switching frequency of the converter to the frequency of the system clock, thus eliminating this type of noise.

PIN DESIGNATION

| | |
|---|---|
| Pin 1 Positive Input | Pin 10 Input common |
| Pin 2 Inhibit Input | Pin 9 Sync |
| Pin 3 Sense return* | Pin 8 Case gnd |
| Pin 4 Output common | Pin 7 N/C |
| Pin 5 Positive output | Pin 6 Positive sense* |

*If neither remote sense nor voltage trim are used, tie pin 3 to 4, 5 to 6 or output voltage will increase by 1.2V.

## PART NUMBER

**ATR 28 xx S x / x**

Model

Input Voltage

Output Voltage
05 – 5VDC
12 – 12VDC
15 – 15VDC

Single Output

Temperature Range
Omit for -55°C to +85°C
ES – -55°C to +125°C
HB – -55°C to +125°C
CH – -55°C to +125°C

Package option
F – Flange
Omit Standard

STANDARD MICROCIRCUIT DRAWING CROSS REFERENCE

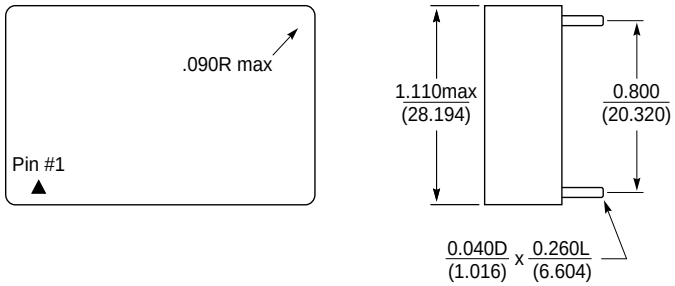
| Standard microcircuit drawing number | Vendor CAGE PIN | Vendor similar |
|---|---|---|
| 5962-94624 | 52467 | ATR2805S/CH |
| 5962-94625 | 52467 | ATR2812S/CH |
| 5962-94626 | 52467 | ATR2815S/CH |

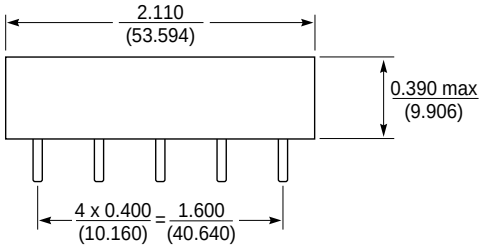
## Available Screening Levels and Process Variations for ATR Series

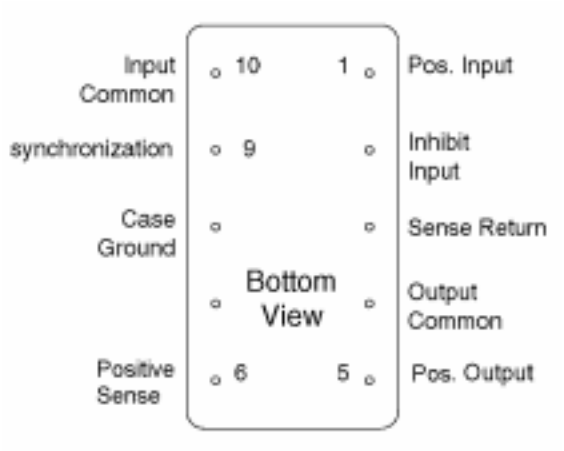
| Requirement | MIL-STD-883 Method | No Suffix | ES Suffix | HB Suffix | CH Suffix |
|---|---|---|---|---|---|
| Temperature Range | | -20 to +85°C | -55°C to +125°C | -55°C to +125°C | -55°C to +125°C |
| Element Evaluation | | | | | MIL-PRF-38534 |
| Internal Visual | 2017 | * | Yes | Yes | Yes |
| Temperature Cycle | 1010 | | Cond B | Cond C | Cond C |
| Constant Acceleration | 2001 | | 500g | Cond A | Cond A |
| Burn-in | 1015 | 96hrs @ 125°C | 96hrs @ 125°C | 160hrs @ 125°C | 160hrs @ 125°C |
| Final Electrical (Group A) | MIL-PRF-38534 | 25°C | 25°C | -55, +25, +125°C | -55, +25, +125°C |
| Seal, Fine & Gross | 1014 | * | Cond A, C | Cond A, C | Cond A, C |
| External Visual | 2009 | * | Yes | Yes | Yes |

* Per Commercial Standards

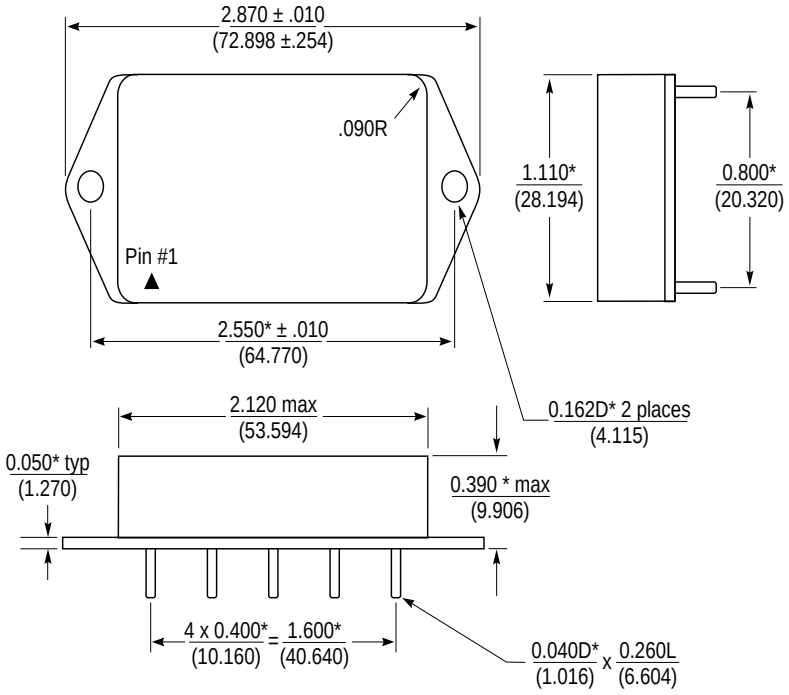
MECHANICAL OUTLINE




ATR2800S



**Thermal Management**

Assuming that there is no forced air flow, the package termperature rise above ambient ($\Delta T$) may be calculated using the following expression:

$$\Delta T \spadesuit 80\ A^{-0.7}\ p^{0.85}\ (^{\circ}C)$$

where A = the effective surface area in square inches (including heat sink if used;) P = power dissipation in watts.

The total surface area of the ATR standard package is 7.34 square inches. If a worse case full load efficiency of 76% is assumed, then the case temperature rise of an ATR 2805S can be calculated as follows:

$$P = P_{OUT}\left[\frac{1}{Eff} - 1\right] = 30\left[\frac{1}{76} - 1\right] = 9.5\ W$$

$$\Delta T = 80\ (7.34)^{-0.7}\ (9.5)^{0.85} = 134^{\circ}C$$

Hence, if $T_{AMBIENT}$ = +25°C, the DC/DC converter case temperature will be approximately 159°C if no heat sink or air flow is provided.

To calculate the heat sink area required to maintain a specific case temperature rise, the above equation may be manipulated as follows:

$$A_{HEAT\ SINK} = \left[\frac{\Delta T}{80P^{0.85}}\right]^{-1.43} - A_{PKG}$$

As an example, if a maximum case temperature rise of 50°C above ambient is desired, then the required effective heat sink area is:

$$A_{HEAT\ SINK} = \left[\frac{50}{80\ (9.5)^{0.85}}\right]^{-1.43} - 7.34 = 22.9\ in.^2$$

*LAMBDA ADVANCED ANALOG INC.*

**MIL-PRF-38534 Certified**
**ISO9001 Registered**

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