Features

- **AVR® 8-bit RISC Microcontroller with 83 ns Instruction Cycle Time**
- **USB Hub with One Attached and Two External Ports**
- **USB Keyboard Function with Three Endpoints**
- **16K Bytes of Program Memory, 512 Bytes SRAM**
- **32 x 8 General-purpose Working Registers**
- **34 Programmable I/O Port Pins**
- **Support for 18 x 8 Keyboard Matrix**
- **Keyboard Scan Inputs with Pull-up Resistors**
- **4 LED Driver Outputs**
- **One 8-bit Timer/Counter with Separate Prescaler**
- **External and Internal Interrupt Sources**
- **Programmable Watchdog Timer**
- **6 MHz Oscillator with On-chip PLL**
- **5V Operation with On-chip 3.3V Power Supply**
- **48-lead SSOP and 48-lead LQFP**

USB Multimedia Keyboard Controller

AT43USB324

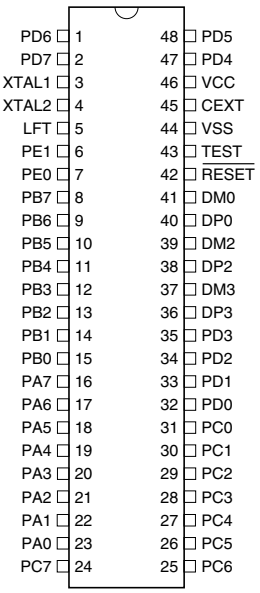
Overview

The Atmel AT43USB324 is a compound USB device designed for use in multimedia USB keyboards with an embedded hub. Internally, the AT43USB324 consists of a USB hub and function interface, a hub repeater, and an AVR microcontroller. To the USB host, the embedded function appears as an attached port of the hub with its own device address and three endpoints. The third function endpoint makes the AT43USB324 extremely suitable for keyboards supporting the Consumer Page as described in the USB HID Usage tables. A typical application of the AT43USB324 is shown in Figure 1 and block diagrams are shown in Figures 2 and 3.

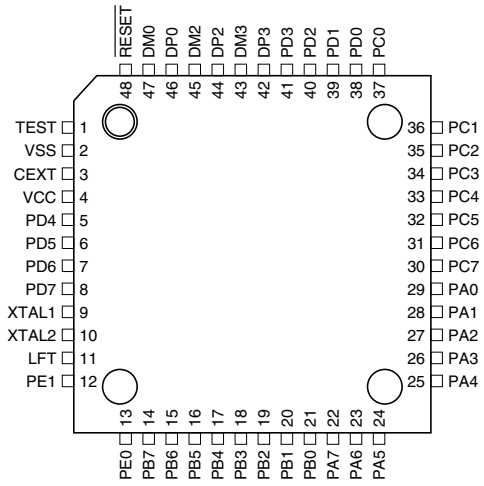
The AT43USB324 interfaces to the USB host at the transaction layer while the microcontroller firmware handles the USB protocol layers in addition to performing the keyboard control functions. Except for LEDs, no other external components are required for the keyboard function.

Pin Configurations

48-lead SSOP



48-lead LQFP



Rev. 1941A–02/01

Figure 1. A Typical USB Hub/Keyboard Application

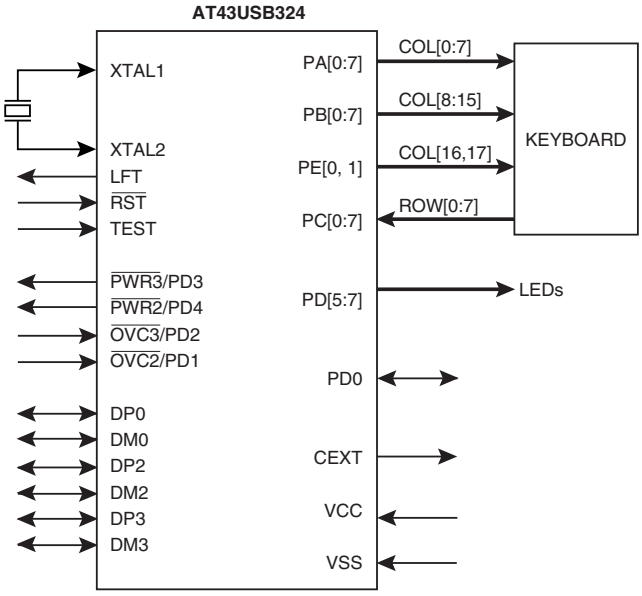


Figure 2. USB Block Diagram (1)

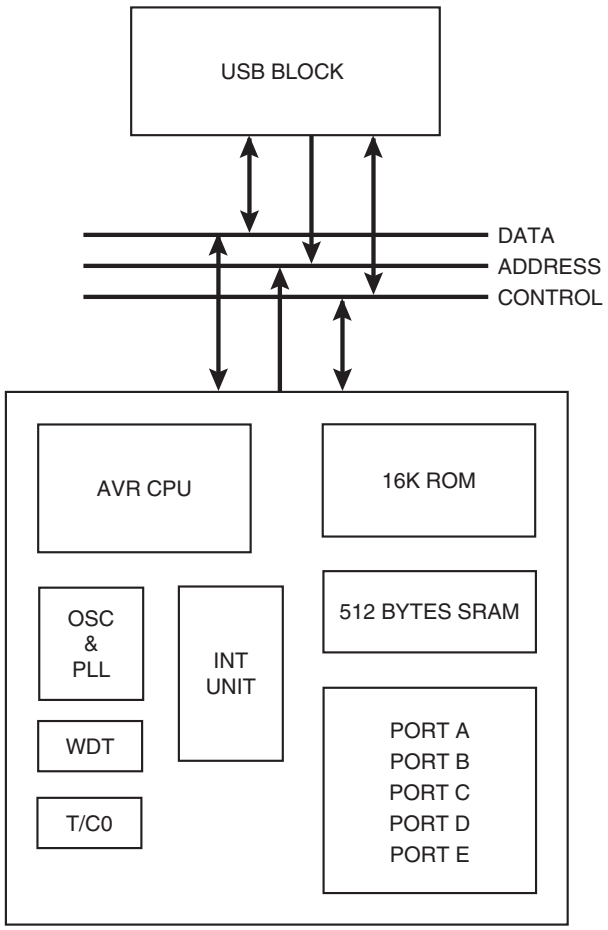
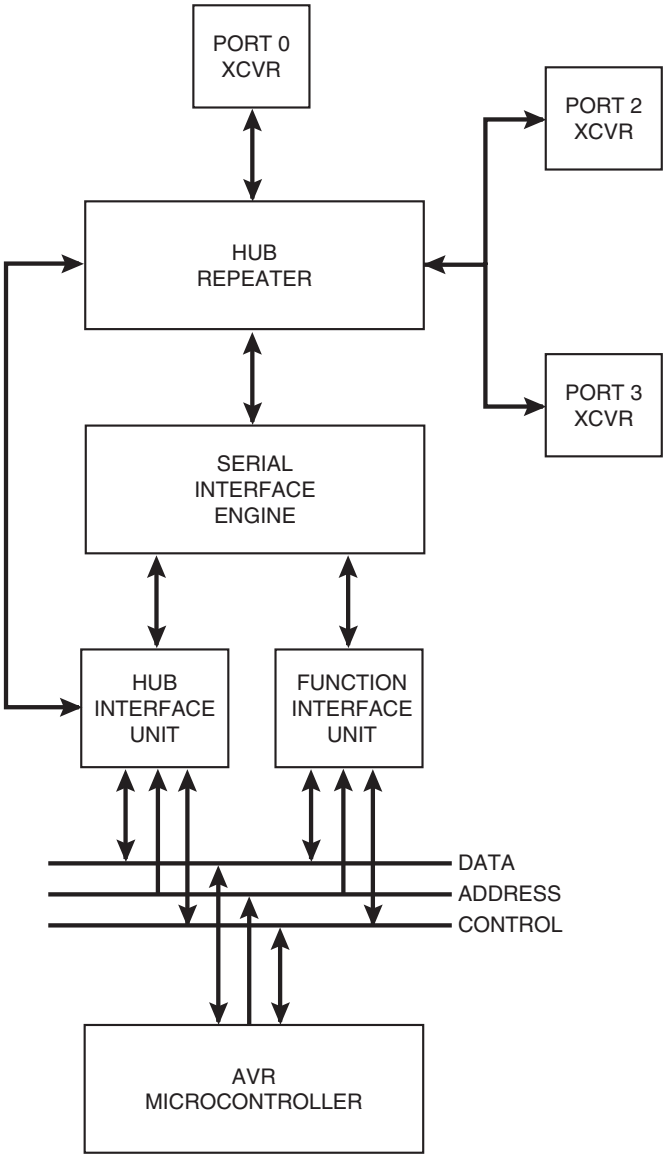


Figure 3. USB Block Diagram (2)



Pin Assignment

Type:
- I = Input
- O = Output
- B = Bi-directional
- U = USB IO
- V = Power Supply, Ground

48-lead LQFP Pin Assignment

Pin #	Signal	Type
1	TEST	I
2	VSS	V
3	CEXT	V
4	VCC	V
5	PD4	B
6	PD5	B
7	PD6	B
8	PD7	B
9	XTAL1	I
10	XTAL2	O
11	LFT	O
12	PE1/CL17	B
13	PE0/CL16	B
14	PB7/CL15	B
15	PB6/CL14	B
16	PB5/CL13	B
17	PB4/CL12	B
18	PB3/CL11	B
19	PB2/CL10	B
20	PB1/CL9	B
21	PB0/CL8	B
22	PA7/CL7	B
23	PA6/CL6	B
24	PA5/CL5	B

Pin #	Signal	Type
25	PA4/CL4	B
26	PA3/CL3	B
27	PA2/CL2	B
28	PA1/CL1	B
29	PA0/CL0	B
30	PC7/RW7	B
31	PC6/RW6	B
32	PC5/RW5	B
33	PC4/RW4	B
34	PC3/RW3	B
35	PC2/RW2	B
36	PC1/RW1	B
37	PC0/RW0	B
38	PD0	B
39	PD1	B
40	PD2	B
41	PD3	B
42	DP3	U
43	DM3	U
44	DP2	U
45	DM2	U
46	DP0	U
47	DM0	U
48	$\overline{\text{RESET}}$	I

48-lead SSOP Pin Assignment

Pin #	Signal	Type
1	PD6	B
2	PD7	B
3	XTAL1	I
4	XTAL2	O
5	LFT	O
6	PE1/COL17	B
7	PE0/CL16	B
8	PB7/CL15	B
9	PB6/CL14	B
10	PB5/CL13	B
11	PB4/CL12	B
12	PB3/CL11	B
13	PB2/CL10	B
14	PB1/CL9	B
15	PB0/CL8	B
16	PA7/CL7	B
17	PA6/CL6	B
18	PA5/CL5	B
19	PA4/CL4	B
20	PA3/CL3	B
21	PA2/CL2	B
22	PA1/CL1	B
23	PA0/CL0	B
24	PC7/RW7	B

Pin #	Signal	Type
25	PC6/RW6	B
26	PC5/RW5	B
27	PC4/RW4	B
28	PC3/RW3	B
29	PC2/RW2	B
30	PC1/RW1	B
31	PC0/RW0	B
32	PD0	B
33	PD1	B
34	PD2	B
35	PD3	B
36	DP3	U
37	DM3	U
38	DP2	U
39	DM2	U
40	DP0	U
41	DM0	U
42	$\overline{\text{RESET}}$	I
43	TEST	I
44	VSS	V
45	CEXT	V
46	VCC	V
47	PD4	B
48	PD5	B

Signal Description

Signal	Type	Name and Functions
VCC	V	**Power Supply** – 5V supply input
CEXT	O	**External Capacitor** – A high quality 0.47 µF must be connected to CEXT for proper operation of the chip.
VSS	V	**Ground**
XTAL1	I	**Oscillator Input** – Input to the inverting oscillator amplifier
XTAL2	O	**Oscillator Output** – Output of the inverting oscillator amplifier
LFT	I	**PLL Filter** – For proper operation of the PLL, this pin should be connected through a 0.01 µF capacitor in parallel with a 100Ω resistor in series with a 0.22 µF capacitor to ground (VSS). Both capacitors must be high quality ceramic
DP0	U	**Upstream Plus USB I/O** – This pin should be connected to CEXT1 through an external 1.5 kΩ pull-up resistor. DP0 and DM0 form the differential signal pin pairs connected to the host controller or an upstream hub
DM0	U	**Upstream Minus USB I/O**
DP[2,3]	U	**Port Plus USB I/O** – Each of these pins should be connected to VSS through an external 15 kΩ resistor. The DP[2,3] and DM[2,3] are the differential signal-pin pairs to connect downstream USB devices
DM[2,3]	U	**Port Minus USB I/O** – Each of these pins should be connected to VSS through an external 15 kΩ resistor
PA[0:7]	B	**Port A[0:7]** – Bi-directional 8-bit I/O port with controlled slew rate. These pins are used as eight of the keyboard matrix column output strobes: PA[0:7] = COL[0:7]
PB[0:7]	B	**Port B[0:7]** – Bi-directional 8-bit I/O port with controlled slew rate. These pins are used as the eight of the keyboard matrix column output strobes: PB[0:7] = COL[8:15]
PC[0:7]	B	**Port C[0:7]** – Bi-directional 8-bit I/O port with internal pull-ups. These pins are used as keyboard matrix row input signals: PC[0:7] = ROW[0:7]
PD[0:7]	B	**Port D[0:7]** – Bi-directional I/O ports. PD[4:7] have built-in series limiting resistors and can be used to drive LEDs directly. An alternate function of PD2 is as INT0 and PD3 is as INT1, the external interrupt pins
PE[0:1]	B	**Port E[0:1]** – Bi-directional I/O port with controlled slew rate which can be used as two additional keyboard column output strobes: COL 16, 17
$\overline{\text{RESET}}$	I	**Reset** – A low on this pin for two machine cycles while the oscillator is running resets the device
TEST	I	**Test Pin** – This pin should be tied to ground

Multimedia Keyboards

The hardware of the AT43USB324 supports a wide variety of USB keyboards with an embedded hub. The exact configuration and function of the keyboard/hub is defined by the firmware programmed into its masked ROM.

Oscillator and PLL

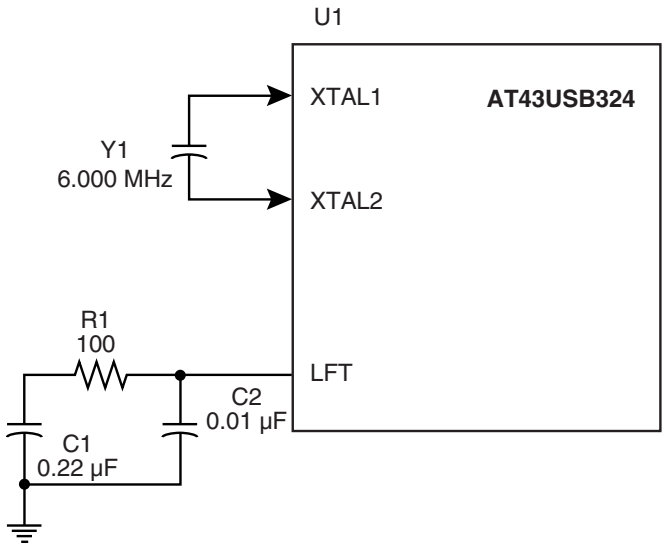
All the clock signals required to run the AT43USB324 are derived from on-chip oscillator. To reduce EMI and power dissipation, the oscillator is designed to operate with a 6 MHz crystal. An on-chip PLL generates the high frequency for the clock/data separator of the serial interface engine. In the suspended state, the oscillator circuitry is turned off.

The oscillator of the AT43USB324 is of a special low drive type, designed to work with most crystals without any external components. The crystal must be of the parallel resonance type requiring a load capacitance of about 10 pF. If the crystal requires a higher value capacitance, external capacitors can be added to the two terminals of the crystal and ground to meet the required value. To assure quick startup, a crystal with a high Q, or low ESR, should be used. To meet the USB hub frequency accuracy and stability requirements for hubs, the crystal should have an accuracy and stability of better than 100 ppm. The use of a ceramic resonator in place of the crystal is not recommended because a resonator would not have the necessary frequency accuracy and stability.

The clock can also be externally sourced. In this case, connect the clock source to the XTAL1 pin, while leaving XTAL2 pin floating. The switching level at the XTAL1 pin can be as low as 0.47V (see Electrical Specifications section on page 10) and a CMOS device is required to drive this pin to maintain good noise margins at the low switching level.

For proper operation of the PLL, an external RC filter consisting of a series RC network of 100Ω and 0.22 µF in parallel with a 0.01 µF capacitor must be connected from the LFT pin to VSS (see Figure 4). Use only high quality ceramic capacitors.

Figure 4. External RC Filter



I/O Pins

The keyboard matrix strobe output pins, PA[0:7], PB[0:7] and PE[0,1] have controlled slope drives. With a load of 100 pF, the output fall time ranges between 75 ns and 300 ns. The keyboard matrix strobe input pins, PC[0:7] have built-in pull-up resistors, 20 kΩ nominal value, to the internal 3.3V power supply.

The PD[4:7] have 5V tolerant open-drain outputs and each has a built-in series resistor of 330Ω nominal value. These output pins are designed for driving a LED connected to the 5V supply.

The remaining GP I/O pins of the AT43USB324 are bi-directional with CMOS inputs and push-pull outputs.

Hub and Port Power Management

The embedded hub in a keyboard will most likely be a bus-powered hub even though the hardware of the AT43USB324 is designed to accommodate both types of hubs. Management of the downstream port power is also defined by the firmware – per port or global overcurrent sensing, individual or gang power switching. While the interface to the external power supply monitoring and switching is achieved through the microcontroller's I/O ports, the USB hardware of the AT43USB324 contains the circuitry to handle all the possible combinations port power management tasks.

Overcurrent Sensing

The AT43USB324 is capable of detecting an overcurrent in its downstream ports even while it is in the suspend state. Overcurrent input flag for Port 2 is routed to PD1 and for Port 3 to PD2.

1. **Global Overcurrent Protection**. In this mode, the Port Overcurrent Indicator and Port Overcurrent Indicator Change should be set to 0's. For the AT43USB324, an external solid state switch, such as the Micrel MIC2025, is required to switch power to both external USB ports. The FLG output of the switch should be connected to either PD0 or PD1 of the microcontroller. When an overcurrent occurs, FLG is asserted and the firmware should set the Hub Overcurrent Indicator and Hub Overcurrent Indicator Change and switch off power to the hub.
2. **Individual Port Overcurrent Protection**. The Hub Overcurrent Indicator and Hub Overcurrent Indicator Change bits should be set to 0's. One MIC2536 is required for the two USB ports. One $\overline{\text{FLG}}$ output of the MIC2536 should be connected to PD0 and the other to PD1 of the microcontroller. An overcurrent is indicated by $\overline{\text{FLG}}$ being asserted. The firmware sets the corresponding port's Overcurrent Indicator and the Overcurrent Indicator Change bits and switches off power to the port. At the next IN token from the host, the AT43USB324 reports the status change.

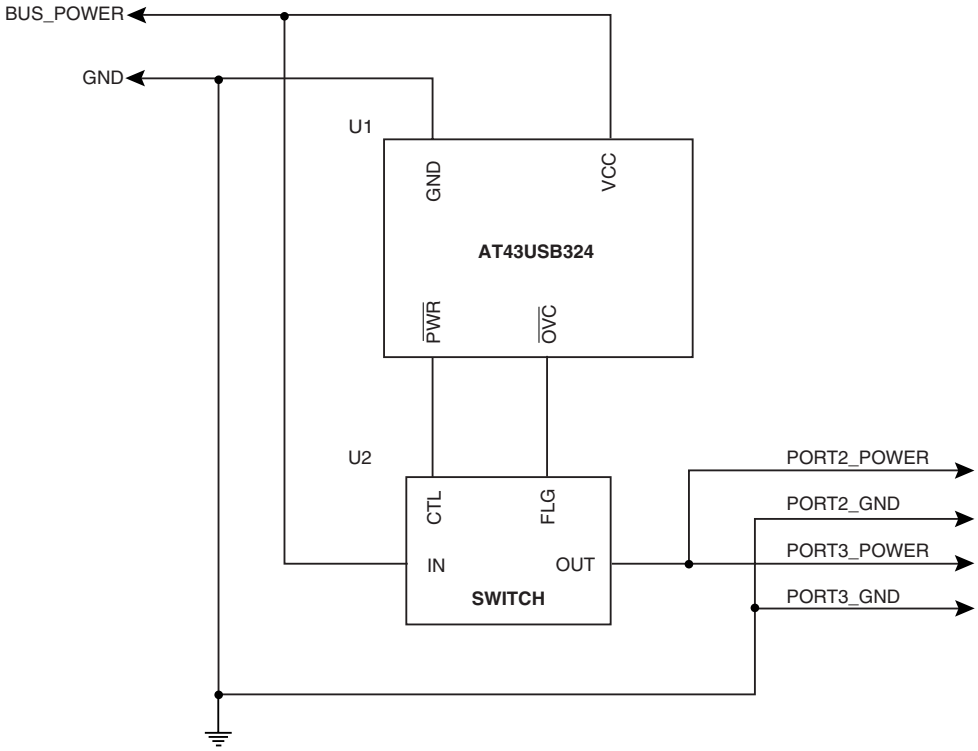
Port Power Switching

1. **Gang Power Switching**. One of the microcontroller I/O port pins must be programmed as an output to control the external switch, $\overline{\text{PWR}}$. Switch ON is requested by the USB host through the SetPortFeature (PORT_POWER) request. Switch OFF is executed upon receipt of a ClearPortFeature (PORT_POWER) or upon detecting an overcurrent condition. The firmware clears the Power Control Bit. Only if all BOTH of the Power Control Bits of Ports 2 AND 3 are cleared should the firmware de-assert the $\overline{\text{PWR}}$ pin.
2. **Individual Power Switching**. One microcontroller I/O port pin must be assigned for each USB port to control the external switch, $\overline{\text{PWR}}$x, where x = 2, 3. Each of the Power Control Bits controls one $\overline{\text{PWR}}$x.

Power Management Circuit

Figure 5 shows a simplified diagram of a power management circuit of an AT43USB324-based hub design with global overcurrent protection and ganged power switching.

Figure 5. Power Management Circuit Diagram



Electrical Specification

Absolute Maximum Ratings*

Operating Temperature	-40°C to +125°C
Storage Temperature	-65°C to +150°C
All Input/Output Voltage	-0.3V to V_{CEXT} + 0.3V, 4.6V max
Supply Voltage (V_{CC})	4.4V to +5.5V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = 0°C to 85°C, V_{CC} = 4.4V to 5.25V, unless otherwise noted.

Power Supply

Symbol	Parameter	Min	Max	Unit
V_{CC}	5V Power Supply	4.4	5.25	V
I_{CC}	5V Supply Current		30	mA
I_{CCS}	Suspended Device Current		150	µA

USB Signals: DPx, DMx

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	Input Level High (Driven)		2.0		V
V_{IHZ}	Input Level High (Floating)		2.7		V
V_{IL}	Input Level Low			0.8	V
V_{DI}	Differential Input Sensitivity	DPx and DMx	0.2		V
V_{CM}	Differential Common Mode Range		0.8	2.5	V
V_{OL1}	Static Output Low	RL of 1.5 kΩ to 3.6V		0.3	V
V_{OH1}	Static Output High	RL of 15 kΩ to GND	2.8	3.6	V
V_{CRS}	Output Signal Crossover		1.3	2.0	V
V_{IN}	Input Capacitance			20	pF

PA, PB, PC, PD, PE

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL2}	Output Low Level, PA, PB, PE0,1	I_{OL} = 4 mA		0.5	V
R_{PU}	PC Pull-up Resistor Current	V = 0	90	280	µA
V_{IL3}	Input Low Level, PC			0.3 V_{CEXT}	V
V_{IH3}	Input High Level, PC		0.7 V_{CEXT}		V
V_{IL4}	Input Low Level, PD[0:3]			0.3 V_{CEXT}	V
V_{IH4}	Input High Level, PD[0:3]		0.7 V_{CEXT}		V
V_{OL4}	Output Low Level, PD[0:3]	I_{OL} = 4 mA		0.3 V_{CEXT}	V
V_{OH4}	Output High Level, PD[0:3]	I_{OH} = 4 mA	0.7 V_{CEXT}		V
C	Input/Output Capacitance	1 MHz		10	pF

Oscillator Signals: XTAL1, XTAL2

Symbol	Parameter	Condition	Min	Max	Unit
V_{LH}	XTAL1 Switching Level		0.47	1.20	V
V_{HL}	XTAL2 Switching Level		0.67	1.44	V
C_{X1}	Input Capacitance, XTAL1			10	pF
C_{X2}	Output Capacitance, XTAL2			10	pF
C_{12}	XTAL1/2 Capacitance			5	pF
t_{SU}	Start-up Time	6 MHz, Fundamental		2	ms
DL	Drive Level			50	µW

Note: XTAL2 must not be used to drive other circuitry.

AC Characteristics

DPx, DMx Driver Characteristics, Full Speed Operation

Symbol	Parameter	Condition	Min	Max	Unit
t_R	Rise Time	CL = 50 pF	4	20	ns
t_F	Fall Time	CL = 50 pF	4	20	ns
t_{RFM}	t_R/t_F Matching		90	110	%
Z_{DRV}	Driver Output Resistance[1]	Steady State Drive	28	44	Ω

Note: 1. With external 27Ω series resistor.

DPx, DMx Source Timings, Full Speed Operation

Symbol	Parameter	Condition	Min	Max	Unit
t_{DRATE}	Full Speed Data Rate[1]	Average Bit Rate	11.97	12.03	Mb/s
t_{FRAME}	Frame Interval[1]		0.9995	1.0005	ms
t_{RFI}	Consecutive Frame Interval Jitter[1]	No Clock Adjustment		42	ns
t_{RFIADJ}	Consecutive Frame Interval Jitter[1]	With Clock Adjustment		126	ns
t_{DJ1} t_{DJ2}	Source Differential Driver Jitter To Next Transition For Paired Transitions		-2 -1	2 1	ns
t_{FDEOP}	Source Jitter for Differential Transition to SEO Transitions		-2	5	ns
t_{DEOP}	Differential to EOP Transition Skew		-2	5	ns
t_{JR1} t_{JR2}	Receiver Data Jitter Tolerance To Next Transition For Paired Transitions		-18.5 -9	18.5 9	ns
t_{FEOPT}	Source SEO Interval of EOP		160	175	ns
t_{FEOPR}	Receiver SEO Interval of EOP		82		ns
t_{FST}	Width of SEO Interval during Differential Transition			14	ns

Note: 1. With 6.000 MHz, 100 ppm crystal.

DPx, DMx Driver Characteristics, Low Speed Operation

Symbol	Parameter	Condition	Min	Max	Unit
t_R	Rise Time	CL = 200 - 600 pF	75	300	ns
t_F	Fall Time	CL = 200 - 600 pF	75	300	ns
t_{RFM}	t_R/t_F Matching		80	125	%

DPx, DMx Hub Timings, Full Speed Operation

Symbol	Parameter	Min	Max	Unit
t_{HDD2}	Hub Differential Data Delay without Cable		44	ns
t_{HDJ1} t_{HDJ2}	Hub Differential Driver Jitter To Next Transition For Paired Transitions	-3 -1	3 1	ns
t_{FSOP}	Data Bit Width Distortion after SOP	-5	5	ns
t_{FEOPD}	Hub EOP Delay Relative to t_{HDD}	0	15	ns
t_{FHESK}	Hub EOP Output Width Skew	-15	15	ns

DPx, DMx Hub Timings, Low Speed Operation

Symbol	Parameter	Min	Max	Unit
t_{LHDD}	Hub Differential Data Delay		300	ns
t_{LHDJ1} t_{LHDJ2} t_{LUHJ1} t_{LUHJ2}	Downstream Hub Differential Driver Jitter To Next Transition, Downstream For Paired Transitions, Downstream To Next Transition, Upstream for Paired Transitions, Upstream	-45 -15 -45 -45	45 15 45 45	ns
t_{SOP}	Data Bit Width Distortion after SOP	-60	60	ns
t_{LEOPD}	Hub EOP Delay Relative to t_{HDD}	0	200	ns
t_{LHESK}	Hub EOP Output Width Skew	-300	300	ns

Hub Event Timings

Symbol	Parameter	Condition	Min	Max	Unit
t_{DCNN}	Time to Detect a Downstream Port Connect Event		2.5	2000	µs
t_{DDIS}	Time to Detect a Disconnect Event on Downstream Port Awake Hub Suspended Hub		2.5 2.5	2000 12000	µs
t_{URSM}	Time from Detecting Downstream Resume to Rebroadcast			100	µs
t_{DRST}	Duration of Driving Reset to a Downstream Device	Only for a SetPortFeature (PORT_RESET) Request	10	20	ms
t_{DSPDEV}	Time to Evaluate Device Speed after Reset		2.5	1000	µs
t_{URLK}	Time to Detect a Long K from Upstream		2.5	5.5	µs
t_{URLSEO}	Time to Detect a Long SEO from Upstream		2.5	5.5	µs
t_{URPSEO}	Duration of Repeating SEO Upstream			23	FS Bits
t_{UDEOP}	Duration of Sending SEO Upstream after EOF1			2	FS Bits

Typical Application

The Atmel sample version of the AT43USB324 contains firmware that supports customization of the Vendor ID, Product ID, String Descriptor and the Keyboard Matrix. This information is stored in an external AT24C02A Serial EEPROM. Data in the EEPROM is stored in the following format.

Address range	Content
0x00 - 0x01	EEPROM's Signature
0x02 - 0x03	Mask Bits
0x04 Onwards	VID, PID and Strings
	Initial Check Byte
0x70 - 0xFF	Keyboard Matrix

Detailed Description

EEPROM's Signature

Address Location	Value/Content
0x00	0x17
0x01	0x5A

Mask Bits

The mask bits identify what features are stored in the EEPROM. A "1" in the mask bit location means that the feature is stored and should be read. A "0", not stored and should not be read.

Address Location	Remark							
0x02	Mask 2 - Reserved for Future Use							
0x03	Mask 1							
	Bit 0: VID, PID, Version	Bit 1: Language String	Bit 2: Manufacturer String	Bit 3: Product String	Bit 4: Serial Number String	Bit 5: Extra Hot Key Codes	Bit 6: Reserved	Bit 7: Keyboard Matrix

Address locations 0x04 through 0x6E store the VID, PID and String Descriptors if they are enabled by the mask bits in location 0x03. The data are stored sequentially as described below.

VID and PID

VID Byte 1	VID Byte 2	PID Byte 1	PID Byte 2	Release # Byte 1	Release # Byte 2	Check Byte

Language ID and Strings

Length (N)	Byte 1	Byte 2

Byte N - 1	Check Byte

Initial Check Byte

This check byte is located immediately after the last VID, PID or strings. It is computed as the truncated sum of Mask 1 and all the string length specified.

Keyboard Matrix

144 bytes. If specified, its check byte is located in address 0x6F while the matrix itself is located from address 0x70 - 0xFF.

0x70 = Col 1, Row 1

0x71 = Col 1, Row 2

.....

0x78 = Col 2, Row 1

0x79 = Col 2, Row 2

.....

0xF8 = Col 18, Row 1

0xF9 = Col 18, Row 2

.....

0xFF = Col 18, Row 8

Example of EEPROM Data

Address	Data	Description
00	17	Fixed ID
01	5A	Fixed ID
02	00	Reserved
03	BF	Mask Bits

The mask bits in location 03 are used to indicate whether a particular function is supported or not.

0 = Function not Supported

1 = Function Supported

Bit7 = Keyboard Matrix

Bit6 = Reserved. Must be Set to 0

Bit5 = Extra Hot Key USB Codes

Bit4 = Serial Number String

Bit3 = Product String

Bit2 = Manufacturer String

Bit1 = Language ID String

Bit0 = VendorID, ProductID, Version.

Vendor ID, Product ID, Version Number

Address	Data	Description
04	5E	Vendor ID
05	04	Vendor ID
06	1D	Product ID
07	00	Product ID
08	11	Version Number
09	01	Version Number
0A	91	Checksum

Language ID

Address	Data	Description
0B	04	Number of Bytes
0C	03	The Next 3 Bytes Specifies the Language ID
0D	09	
0E	10	
0F	20	Checksum

Manufacturer String

Address	Data	Description
10	0C	Number of Bytes, 2 Bytes per Character
11	03	
12	41	A
13	00	
14	74	T
15	00	
16	6D	M
17	00	
18	65	E
19	00	
1A	6C	L
1B	00	
1C	02	Checksum

Product String

Address	Data	Description
1D	12	Number of Bytes
1E	03	
1F	4D	M
20	00	
21	4D	M
22	00	
23	4B	K
24	00	
25	42	B
26	00	
27	44	D
28	00	
29	48	H
2A	00	
2B	55	U
2C	00	
2D	42	B
2E	00	
2F	5F	Checksum

Serial Number String

Address	Data	Description
30	08	Number of Bytes
31	03	
32	31	1
33	00	
34	32	2
35	00	
36	33	3
37	00	
38	A1	Checksum

Extra Hot Keys

Address	Data	Description
39	07	Number of Bytes
3A	D0	KB Matrix Code
3B	23	First Byte Sent to Host
3C	02	Second Byte Sent to Host
3D	D1	KB Matrix Code
3E	8A	First Byte Sent to Host
3F	01	Second Byte Sent to Host
40	58	Checksum

Miscellaneous Data

Address	Data	Description
41	F0	Checksum of Mask Byte + Bytes in Language ID + Bytes in Manuf String + Bytes in Product String + Bytes in Serial Number + Bytes in Extra Hot Keys (BF + 04 + 0C + 12 + 08 + 07 = F0)
42 through 6E		Don't Cares. May be Written with 0's
6F	2D	Checksum of Keyboard Matrix Codes

Keyboard Matrix

Address	Data	KB Row	KB Col	Description
70	28	0	0	KB Enter
71	31	1	0	KB \
72	50	2	0	Left Arrow
73	3F	3	0	F6
74	30	4	0	]
75	3E	5	0	F5
76	2A	6	0	Backspace
77	2E	7	0	=
78	36	0	1	Comma
79	07	1	1	D
7A	06	2	1	C
7B	25	3	1	KB 8

Keyboard Matrix (Continued)

Address	Data	KB Row	KB Col	Description
7C	0E	4	1	K
7D	20	5	1	KB 3
7E	08	6	1	E
7F	0C	7	1	I
80	63	0	2	KP Period
81	5E	1	2	KP 6
82	5B	2	2	KP 3
83	3D	3	2	F4
84	61	4	2	KP 9
85	3C	5	2	F3
86	4C	6	2	Delete
87	49	7	2	Insert
88	37	0	3	Period
89	2F	1	3	[
8A	0F	2	3	L
8B	41	3	3	F8
8C	12	4	3	O
8D	40	5	3	F7
8E	2D	6	3	-
8F	26	7	3	9
90	05	0	4	B
91	0A	1	4	G
92	19	2	4	V
93	22	3	4	5
94	09	4	4	F
95	21	5	4	4
96	17	6	4	T
97	15	7	4	R
98	13	0	5	P
99	34	1	5	Quote
9A	38	2	5	/
9B	43	3	5	F10
9C	33	4	5	;
9D	42	5	5	F9
9E	41	6	5	Down Arrow
9F	27	7	5	0

Keyboard Matrix (Continued)

Address	Data	KB Row	KB Col	Description
A0	10	0	6	M
A1	0D	1	6	J
A2	11	2	6	N
A3	24	3	6	7
A4	0B	4	6	H
A5	23	5	6	6
A6	18	6	6	U
A7	1C	7	6	Y
A8	68	0	7	
A9	69	1	7	
AA	6A	2	7	
AB	2C	3	7	Space
AC	78	4	7	
AD	4F	5	7	Right Arrow
AE	E7	6	7	Right GUI
AF	52	7	7	Up Arrow
B0	62	0	8	KP 0
B1	5D	1	8	KP 5
B2	5A	2	8	KP 2
B3	45	3	8	F12
B4	60	4	8	KP 8
B5	44	5	8	F11
B6	4D	6	8	End
B7	4A	7	8	Home
B8	59	0	9	KP 1
B9	5C	1	9	KP 4
BA	57	2	9	KP +
BB	65	3	9	Application
BC	5F	4	9	KP 7
BD	46	5	9	Print Screen
BE	55	6	9	KP *
BF	54	7	9	KP /
C0	1B	0	10	X
C1	1A	1	10	W
C2	16	2	10	S
C3	3B	3	10	F2

Keyboard Matrix (Continued)

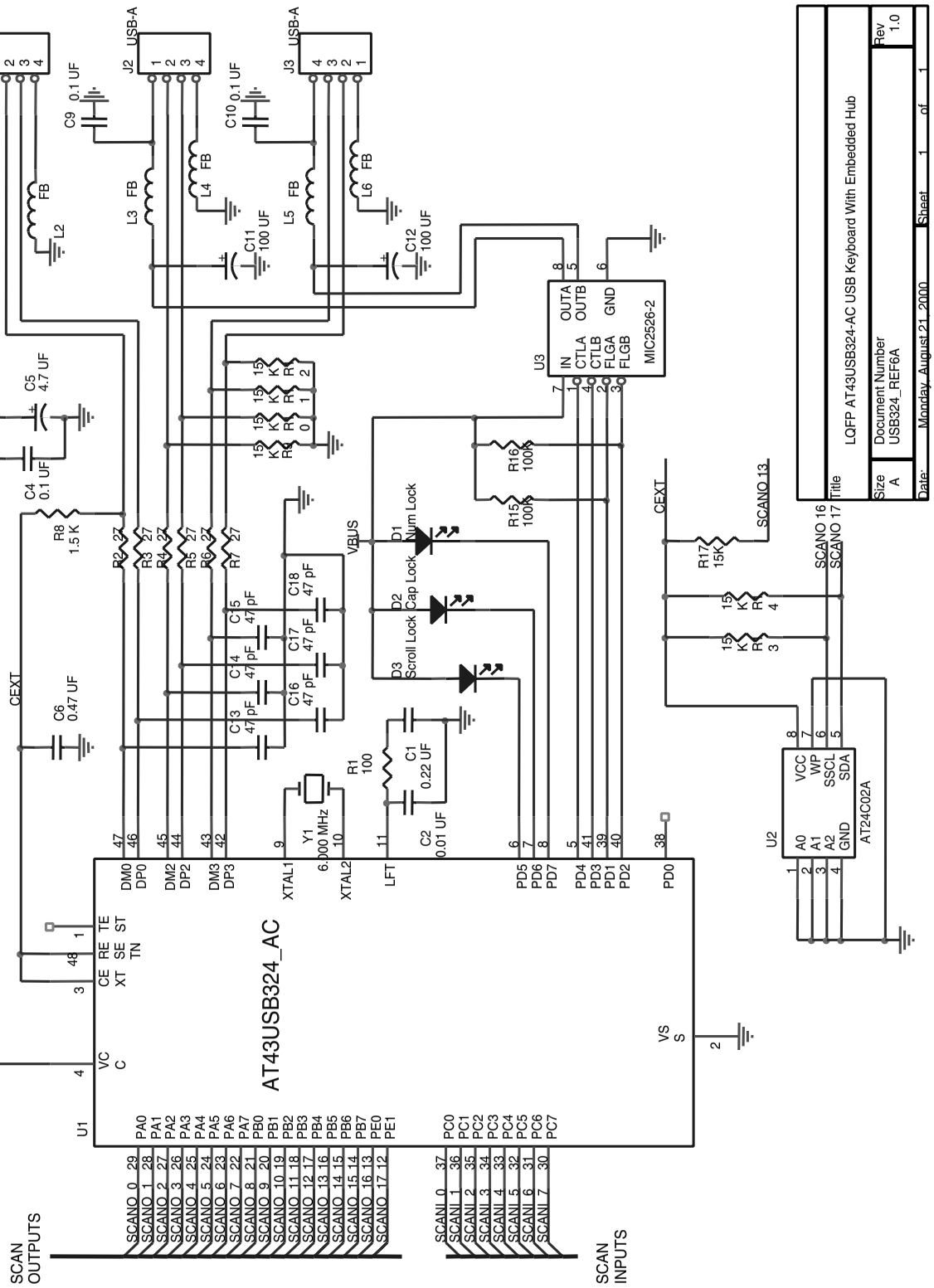
Address	Data	KB Row	KB Col	Description
C4	1F	4	10	2
C5	3A	5	10	F1
C6	4E	6	10	Page Down
C7	4B	7	10	Page Up
C8	E4	0	11	Right Ctrl
C9	6B	1	11	
CA	D5	2	11	HK Calculator
CB	D4	3	11	HK Media
CC	E0	4	11	L
CD	C0	5	11	HK Suspend
CE	39	6	11	Caps Lock
CF	D6	7	11	HK My Comp
D0	1D	0	12	Z
D1	04	1	12	A
D2	6D	2	12	
D3	35	3	12	~
D4	14	4	12	Q
D5	29	5	12	Escape
D6	2B	6	12	Tab
D7	1E	7	12	1
D8	6E	0	13	
D9	C9	1	13	HK Vol Decrement
DA	70	2	13	
DB	71	3	13	
DC	B0	4	13	HK Mute
DD	72	5	13	
DE	73	6	13	
DF	74	7	13	
E0	E5	0	14	Right Shift
E1	C8	1	14	HK Vol Increment
E2	C1	2	14	HK Play/Pause
E3	C2	3	14	HK Scan Next
E4	E1	4	14	Left Shift
E5	48	5	14	Pause
E6	C4	6	14	HK Stop
E7	C3	7	14	HK Scan Previous

Keyboard Matrix (Continued)

Address	Data	KB Row	KB Col	Description
E8	D1	0	15	HK WWW
E9	E2	1	15	Left Alt
EA	E6	2	15	Right Alt
EB	53	3	15	KP Num Lock
EC	DF	4	15	HK Bookmark
ED	56	5	15	KP -
EE	D9	6	15	HK Search
EF	D0	7	15	HK e-mail
F0	DD	0	16	HK AC Stop
F1	74	1	16	
F2	DE	2	16	HK Refresh
F3	58	3	16	KP Enter
F4	DC	4	16	HK Forward
F5	47	5	16	Scroll Lock
F6	DB	6	16	HK Back
F7	E3	7	16	Left GUI
F8	00	0	17	
F9	00	1	17	
FA	00	2	17	
FB	00	3	17	
FC	00	4	17	
FD	00	5	17	
FE	00	6	17	
FF	00	7	17	

The following two pages show a schematic diagram of an AT43USB324 keyboard with an embedded hub and its Bill of Materials information.

AT43USB324 Keyboard Schematic Diagram

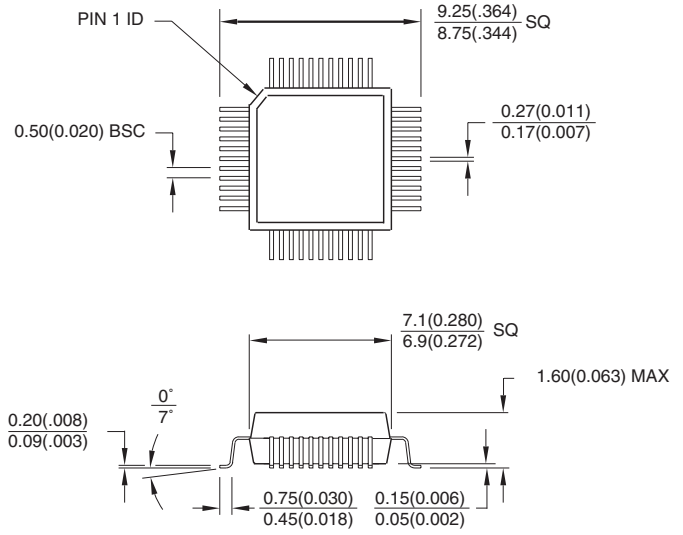


Bill of Materials

Item	Quantity	Reference	Part	Supplier
1	1	C1	0.22 µF, Ceramic, Kemet C1812C224K5RAC	Newark 99F6389
2	1	C2	0.01 µF, Ceramic, Kemet C0805C103K5RAC	Newark 93F2330
3	3	C4,C9,C10	0.1 µF, Ceramic, Kemet C1206C104M5UAC	Newark 89F5966
4	1	C5	4.7 µF, Electrolytic, Panasonic ECE-V1ES4R7SR	Digikey PCE3065CT-ND
5	1	C6	0.27 µF, Ceramic, Kemet C1210C274M5UAC	Newark 93F241
6	2	C12,C11	100 µFD, Electrolytic, Panasonic ECE-V1AA101SP	Digikey PCE3176CT-ND
7	6	C13,C14,C15,C16,C17,C18	47 pF, Ceramic, Kemet C1206C470J5GACTR	Newark 93F2371
8	1	J1	USB-B, Series B Connector	AMP 787780-1
9	2	J2,J3	USB-A, Series A Connector	AMP 787616-1
10	3	D1,D2,D3	LED, Green	Jameco 34606, XC2
11	6	L1,L2,L3,L4,L5,L6	Ferrite Bead, Stewart HI 1806 N 750 R	Digikey 240-1-11-1-ND
12	1	R1	100, Panasonic ERJ-GEYJ100	Digikey P-100-ACT-ND
13	6	R2,R3,R4,R5,R6,R7	27, Panasonic ERJ-GEYJ27	Digikey P-27-ACT-N
14	1	R8	1.5K, Panasonic ERJ-GEYJ1.5K	Digikey P-1.5K-ACT-ND
15	7	R9,R10,R11,R12,R13,R14,R17	15K, Panasonic ERJ-GEYJ15K	Digikey P-15K-ACT-ND
16	2	R15,R16	100K, Panasonic ERJ-GEYJ100K	Digikey P-100K-ACT-ND
17	1	U1	AT43USB324-AC	Atmel
18	1	U2	AT24C02A	Atmel
19	1	U3	MIC2526-2BM	Micrel
20	1	Y1	6.000 MHz Crystal, CTS ATS060SM-T	Digikey CTX505CT-ND

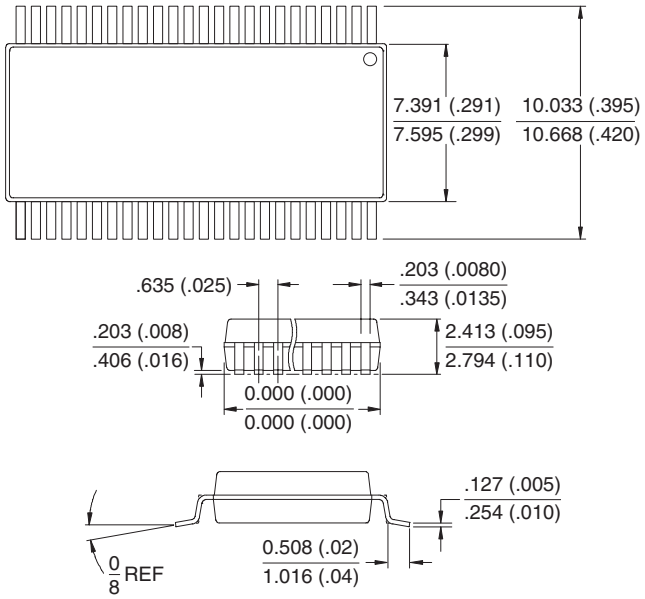
Packaging Information

48A, 48-lead, Low-profile (1.4 mm) Plastic Quad Flat Package (LQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-026 ACB



*Controlling dimension: millimeters

48Y, 48-lead, 7.62 mm Wide, Plastic Shrink Small Outline (SSOP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel SarL
Route des Arsenaux 41
Casa Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Atmel Smart Card ICs
Scottish Enterprise Technology Park
East Kilbride, Scotland G75 0QR
TEL (44) 1355-357-000
FAX (44) 1355-242-743

Atmel Grenoble
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex
France
TEL (33) 4-7658-3000
FAX (33) 4-7658-3480

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

1941A–02/01/xM