AN8104FBP

High speed Low Power Consumption 8-Bit A/D Converter

■ Overview

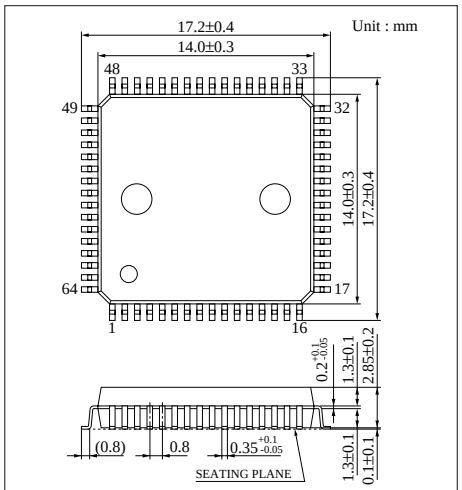
The AN8104FBP is a 8-bit A/D convertor for measurement which uses the high frequency bipolar process to suppress the power consumption. It can operate with single power supply of –5.2V and maximum conversion rate of 125 MSPS, realizing the wide input band and the low error rate.

■ Features

- 8-bit resolution
- High speed : maximum conversion rate of 125MSPS (min.)
- Wide input band : 250MHz, typ.(–3dB)
- Low error rate : 10^{-12} tps or lower
- Low input capacitance : 15pF
- Input/Output form : ECL level

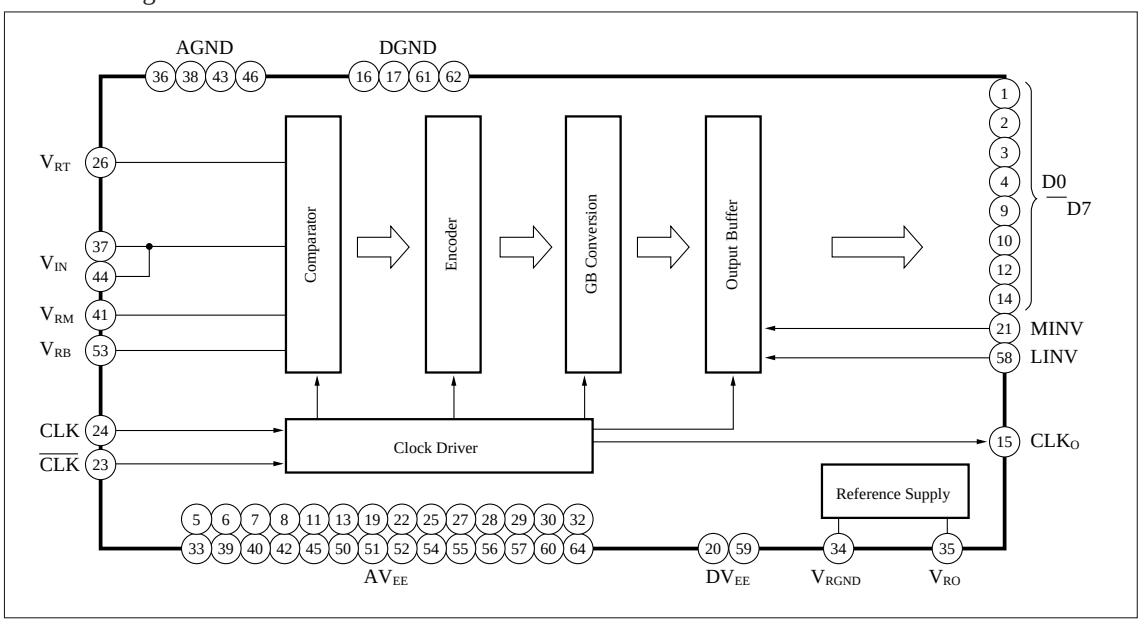
■ Application Field

- Measuring equipment such as digital oscilloscope
- Image processing



64-pin Flat Package (QFH064-P-1414)

■ Block Diagram



■ Absolute Maximum Ratings (Ta=25˚C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{EE}	–6.0 to + 0.3	V
Analogue input voltage	V_{IN}	V_{EE} to + 0.3	V
Digital input voltage	$V_{CLK}/\overline{V_{CLK}}$	V_{EE} to + 0.3	V
Digital output current	I_{CLKO}/I_{D0}—I_{D7}	–20	mA
Reference power supply output current	I_{RO}	25	mA
Reference resistive current	I_{RT}/I_{RB}	+20/–20	mA
Reference voltage	$V_{RT}/V_{RB}/V_{RM}$	V_{EE} to + 0.3	V
Power dissipation	P_D	964*	mW
Operating ambient temperature	T_{opr}	–20 to +70	˚C
Storage temperature	T_{stg}	–55 to +150	˚C

* Ta=75˚C

■ Recommended Operating Conditions (Ta=25˚C)

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V_{EE}	–5.4	–5.2	–5.0	V
Reference voltage	V_{RT}	—	0.0	—	V
	V_{RB}	—	–2.0	—	V
Analogue input voltage	V_{IN}	V_{RB}	—	V_{RT}	V
Digital input voltage	V_{IH}	–1.1	– 0.9	—	V
	V_{IL}	—	–1.7	–1.5	V
Clock input pulse width *	t_H/t_L	—	2.5	—	ns

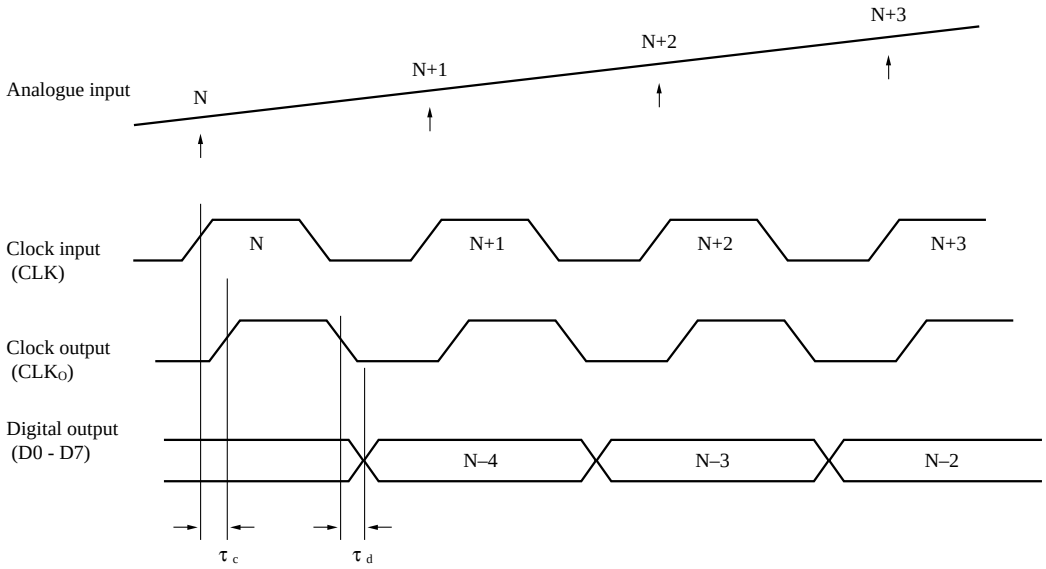
* f_{CLK}=200MHz

■ Electrical Characteristics (V_{EE}=–5.2V, Ta=25˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Supply current	I_{EE}		–300	–125	—	mA
Reference power supply output voltage	V_{RO}	I_{RO}=10mA, V_{RGND}=0V	–2.2	–2.0	–1.8	V
Reference supply current	I_{RGND}	Reference power supply output under no Load	—	0.6	5	mA
Reference resistive current	I_{RT}	V_{RT}=0V	—	9	20	mA
	I_{RB}	V_{RB}=2.0V	–20	–9	—	mA
Input bias current	I_{IN}	V_{IN}=1.0V	—	480	1000	µA
Clock input current	I_{IH}	V_{CLK}=–1.105V	—	0.5	5	µA
Digital output voltage	V_{OH}	R_L=100Ω TO V_T=–2.0V	–1.1	– 0.9	– 0.6	V
	V_{OL}		–2.0	–1.8	–1.6	V
Linearity error	E_L	V_{RT}–V_{RB}=2.0V	—	±0.25	±0.65	LSB
Differential linearity error	E_D	V_{RT}–V_{RB}=2.0V	—	±0.25	±0.65	LSB
Maximum conversion rate	F_{CMAX}		125	—	—	MHz
Input dynamic range			—	2	—	V_{p-p}
Equivalent input impedance *1	R_{IN}	V_{IN}=–1V	—	50	—	kΩ
Input capacitance *1	C_{IN}	V_{IN}=–1V	—	15	—	pF
Error rate *1		f_{CLK}=125MHz, f_{IN}=40.5MHz 8LSB or higher	—	10^{-12}	—	tps
Quantization noise *2	SINAD	f_{CLK}=125MHz, f_{IN}=10.000125MHz	—	43	—	dB
		f_{CLK}=125MHz, f_{IN}=100.000125MHz	—	34	—	dB
Input band *1	BW_F	V_{IN}=1.4V_{p-p}, –3dB	200	—	—	MHz
Clock duty *1	DTY	f_{CLK}=125MHz	—	50	—	%
Clock output delay *1	τ_c		—	6.5	—	ns
Digital output delay *1	τ_d		—	1.3	—	ns

*1 Design reference value but not guaranteed one *2 Total harmonics distortion included

■ Timing Chart



■ Output Code

Step	Input signal	Digital output		
	2.000VFS 7.8125mV STEP	MINV= L, LINV= L	MINV= H, LINV= L	MINV= L, LINV= H
		M L 76543210	M L 76543210	M L 76543210
000	–2.0000000	00000000	10000000	01111111
001	–1.9921875	00000001	10000001	01111110
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
127	–1.0078125	01111111	11111111	00000000
128	–1.0000000	10000000	00000000	11111111
129	– 0.9921875	10000001	00000001	11111110
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
254	– 0.0078125	11111110	01111110	10000001
255	0.0000000	11111111	01111111	10000000

■ Pin Descriptions

Pin No.	Symbol	Pin name	Standard waveform	Voltage level	Description
37 44	V_{IN}	Analogue input		–2 to 0V	It is an input pin of analogue signal for A/D conversion circuit.
36, 38 43, 46	AGND	Analogue ground		0V	Connect AGND and DGND with the possible lowest impedance at one point as near as possible to the chip.
5, 6, 7 8, 11, 13 19, 22, 25 27, 28, 29 30, 32, 33 39, 40, 42 45, 50, 51 52, 54, 55 56, 57, 60 64	AV_{EE}	Analogue negative power supply pin		–5.2V	It is a power supply pin for analogue circuit block. Connect tantalum capacitor of several µF and ceramic capacitor of 0.1µF as near as possible to this pin between this pin and DGND.
20, 59	DV_{EE}	Analogue negative power supply pin		–5.2V	It is a power supply pin for digital. Connect tantalum capacitor of several µF and ceramic capacitor of 0.1µF as near as possible to this pin between this pin and AGND or DGND.
26 41 53	V_{RT} V_{RM} V_{RB}	Reference voltage high level, Reference voltage middle point level, Reference voltage low level		0V –1.0V –2.0V	It is used to set the reference voltage for comparator. Normally, V_{RT} is given 0V and V_{RB} is given –2V. Connect tantalum capacitor of several µF and ceramic capacitor of 0.1µF in parallel between each pin and analogue ground. V_{RM} is provided for linearity compensation which gives middle point potential between V_{RT} and V_{RB}. However, it is normally opened.
16, 17 61, 62	DGND	Digital ground		0V	Connect AGND and DGND with the possible lowest impedance at one point as near as possible to the chip.
23 24	$\overline{CLK}$ CLK	Clock input	Refer to the timing chart.	ECL	It is a clock for sampling. For their timing, refer to the timing chart.
15	CLK_O	Clock output	Refer to the timing chart.	ECL	It is a clock output pin of ECL level.
1 2 3 4 9 10 12 14	D0 D1 D2 D3 D4 D5 D6 D7	Digital output (LSB), Digital output, Digital output, Digital output, Digital output, Digital output, Digital output, Digital output (MSB)	Refer to the timing chart.	ECL	It is an output pin of ECL Level.
21 58	MINV LINV	Digital output setting pin, Digital output setting pin		ECL	Setting the MINV pin to “H” level inverts the data output, D7. Setting the LINV pin to “H” level inverts the data outputs (D0 - D6). The output is inverts synchronously with clock.
34 35	V_{RGND} V_{RO}	Ground pin for reference Power supply, Reference power supply output		0V –2.0V	It is a GND pin for reference power supply. It is an output pin for power supply for A/D reference voltage low level.