AN8031

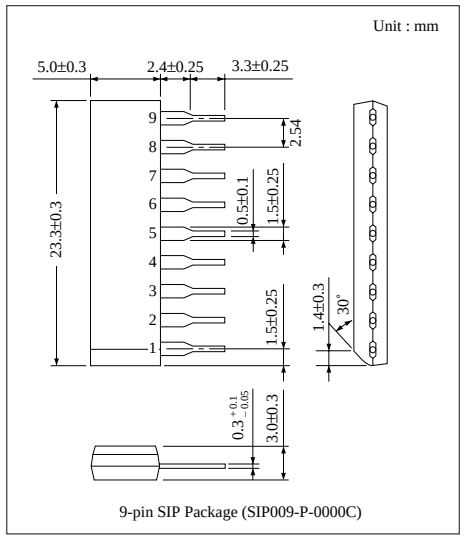
Active-Filter Control IC

■ Overview

When the power is supplied from the commercial power supply to the electrical equipment, the harmonic distortion generating in the power line may give obstruction to the power facilities or other electrical equipments.

The active filter is used to protect against such harmonic distortion problems.

The AN8031 is a monosilic IC which incorporates the control functions and protection ones into one package so that the active filter can be easily constructed. So, it is suitable for the lighting equipment, which otherwise suffers from the harmonic distortion.



9-pin SIP Package (SIP009-P-0000C)

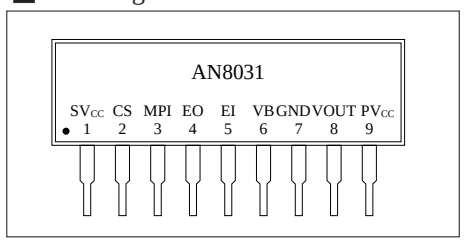
■ Features

- Automatic peak current mode employed
- Built-in circuit preventing the overvoltage generated under the small load
- Easy constant setting with enlarged dynamic range of multiplier/error amplifier.
- Employed totem pole output circuit which allows the power MOS-FET to be directly driven.
- Built-in low voltage protection circuit which ensures the ON-resistance during the power MOS-FET operation.
- Built-in timer circuit which can realize the automatic start

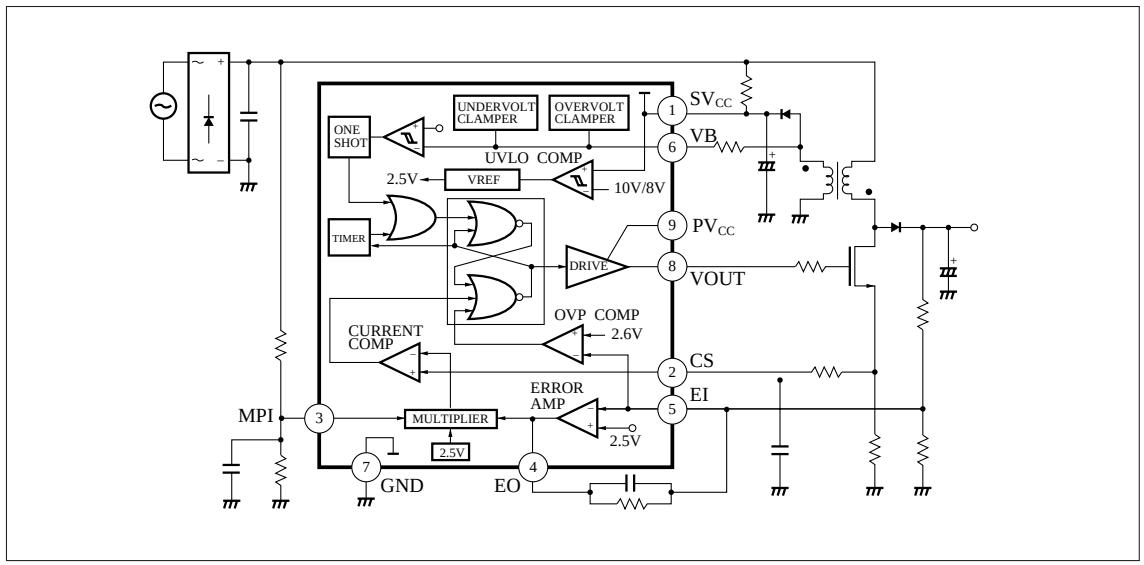
■ Application

- Lighting equipment
- Switching power supply

■ Pin Assignments



■ Block Diagram



■ Absolute Maximum Ratings (Ta=25˚C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	35	V
Output allowable current	I_O	±150	mA
Peak output current	I_{OP}	±1	A
VB allowable in current	I_{BI}	+5	mA
VB allowable out current	I_{BO}	–5	mA
VD allowable applied voltage	V_{CS}	– 0.5 to 7	V
MPI allowable applied voltage	V_{MPI}	– 0.5 to 7	V
EI allowable applied voltage	V_{EI}	– 0.5 to 7	V
Power dissipation	P_D	874	mW
Operating ambient temperature	T_{opr}	–30 to 85	˚C
Storage temperature	T_{stg}	–55 to 150	˚C

■ Recommended Operating Conditions (Ta=25˚C)

Parameter	Symbol	min	max	Unit
Supply voltage	V_{CC}	0	34	V

■ Electrical Characteristics (Ta=25±2˚C)

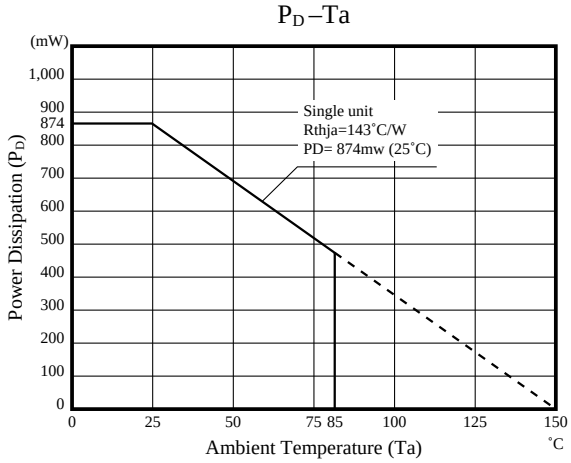
Parameter	Symbol	Condition	min	typ	max	Unit
Error detection feedback threshold voltage 1	V_{E1}^{TH1}		2.35	2.50	2.65	V
Error detection output L voltage	V_{EO}^{L}	I_{EO}=0mA, V_{EI}=5V	—	1.0	1.6	V
Error detection output H voltage	V_{EO}^{H}	I_{EO}=0mA, V_{EI}=0V	5.0	5.7	—	V
Error detection input bias current	I_{EI}	V_{EI}=0V	—	– 0.3	–1.0	µA
Error detection output supply current	I_{EO}	V_{EI}=0V, V_{EO}=1V	0.25	0.50	0.75	mA
Multiplier input D-range (upper limit)	V_{MPI}^{H}	V_{EO}=5V	4.0	4.5	—	V
Multiplier output D-range (upper limit)	V_{MPO}^{H}	V_{EO}=5V	4.8	5.4	—	V
Multiplier gain	G_{MP}		1.0	1.2	1.4	1/V
Multiplier input bias current	I_{MPI}	V_{MPI}=0V	—	–1.5	–3.0	µA
Winding detection input threshold voltage	V_B^{TH}		1.2	1.5	1.8	V
Winding detection hysteresis width	dV_B		50	100	200	mV
Winding detection H clamp voltage	V_B^{H}	I_B=5mA	7.0	7.5	8.0	V
Winding detection L clamp voltage	V_B^{L}	I_B=–5mA	– 0.3	– 0.2	0	V
Current detection input offset voltage	V_{CS}^{OFF}		—	3.5	15	mV
Current detection input bias current	I_{CS}	V_{CS}=0V	—	– 0.5	–2.0	µA
Overvoltage detection input threshold voltage	V_{OVP}		2.45	2.60	2.75	V
V_{OVP} –V_{EI}^{TH1}	—		70	100	130	mV
Output L voltage	V_{OUT}^{L}	I_{OUT}=100mA	—	0.9	1.5	V
Output H voltage	V_{OUT}^{H}	I_{OUT}=–100mA	9.2	10.2	—	V
Stand-by output voltage	V_{OUT}^{STB}	I_{OUT}=10mA	—	0.8	1.5	V
UVLO start voltage	V_{CC}^{ST}		9.2	10.0	10.8	V
UVLO stop voltage	V_{CC}^{SP}		7.0	8.0	9.0	V
UVLO start - stop voltage difference	dV_{CC}	$dV_{CC}=V_{CC}^{ST}–V_{CC}^{SP}$	1.75	2.00	2.50	V
Stand-by current	I_{CC}^{STB}	V_{CC}=7V	40	80	120	µA
No load operation current	I_{CC}	V_{CC}=12V	—	6.0	10.0	mA

■ Electrical Characteristics (for Design Reference)

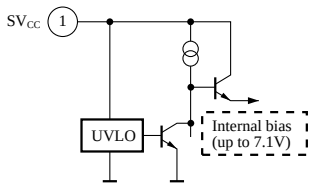
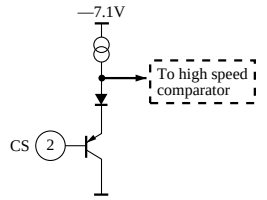
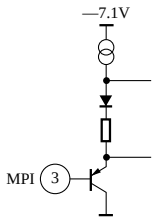
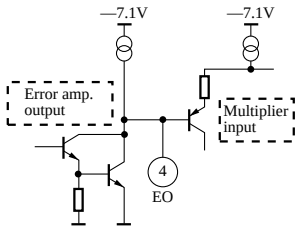
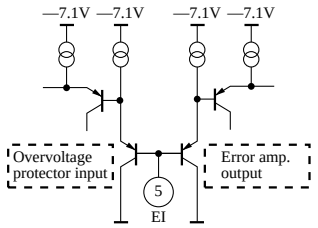
Parameter	Symbol	Condition	Reference value	Unit
Error detection feedback threshold voltage 2	V_{EI}^{TH2}	Ta= –25˚C to + 85˚C	2.3 to 2.7	V
Error detection open-loop gain	G_{AV}		85	dB
Error detection gain band width	f_{BW}		1.0	MHz
Multiplier input d-range (lower limit)	V_{MPI}^{L}	V_{EO}=5V	0	V
Multiplier output d-range (lower limit)	V_{MPO}^{L}	V_{EO}=5V	0	V
Current detection-output delay	td^{CS}		200	ns
Overvoltage detection-output delay	td^{OVP}		500	ns
Output rise time	tr	V_{CC}=12V, V_{OUT}=10→90%	50	ns
Output fall time	t_f	V_{CC}=12V, V_{OUT}=90→10%	50	ns
Timer delay time	td^{TIM}		400	µs

Note) These values are design reference values, not guaranteed ones.

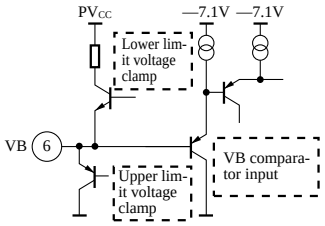
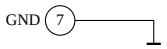
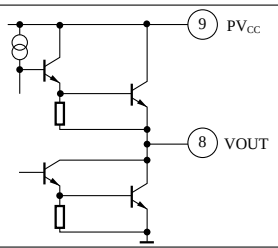
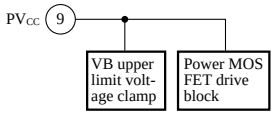
■ Characteristics Curve



■ Pin Descriptions

Pin No.	Pin name	I/O	Terminal description	Internal equivalent circuit
1	SV_{CC}	I	Supply voltage terminal for control system. It monitors the supply voltage and has operation threshold for start/stop.	
2	CS	I	Input terminal for comparator which detects the value of current flowing in power MOS FET. It compares the output level of multiplier and the current value of power MOS FET which is inputted from CS terminal. When the latter value gets larger than the former value, it sets VOUT “L” to shut off the power MOS FET.	
3	MPI	I	Input terminal for multiplier It monitors the voltage after the AC input voltage is full-wave-rectified.	
4	EO	O	Double function : Output terminal for error amp. and input terminal for multiplier For error amp, it monitors the output voltage of active filter to amplify the error for output to multiplier. It also functions as another input terminal for the multiplier.	
5	EI	I	Double function : reverse input terminal for error amp. and input terminal for overvoltage protector. The reference voltage inside the IC ($2.5V^{TYP}$) is inputted to non-reverse input terminal. The terminal monitors the output voltage of active filter : It functions as input terminal for overvoltage protector which detects the overvoltage of output voltage to shut off power MOS FET.	

■ Pin Descriptions (cont.)

Pin No.	Pin name	I/O	Terminal description	Internal equivalent circuit
6	VB	I	The terminal, which is connected through resistor with sub-winding of transformer, detects the reset of transformer to send trigger signal which turns on power MOS FET. Since the winding signal of transformer is inputted as current, the IC incorporates the circuit which clamps the upper/lower limit voltage to prevent malfunction.	
7	GND	—	Ground terminal Double function : Ground terminal for control system and power system	
8	VOUT	O	Output terminal It can directly drive the gate of power MOS FET.	
9	PV_{CC}	—	Supply voltage terminal for power system It determines the upper limit of the output drive voltage. Normally, it is used with the same potential as SV_{CC}.	

■ Operation Description

1. Normal control

(1) Application outline

As shown in Fig.1, the standard application of the AN8031 is a booster chopper circuit, which inputs the voltage rectified from the commercial supply of 100/200V (A in Fig.1)and outputs the DC voltage of 400V (B in Fig.B).

It controls so that the input current proportional to the input voltage (C, D in Fig.1) could be flown.

The output voltage of 400V is selected, considering the withstand voltage of parts and the operation limitation of booster chopper (input voltage<output voltage) under the worldwide input voltage.

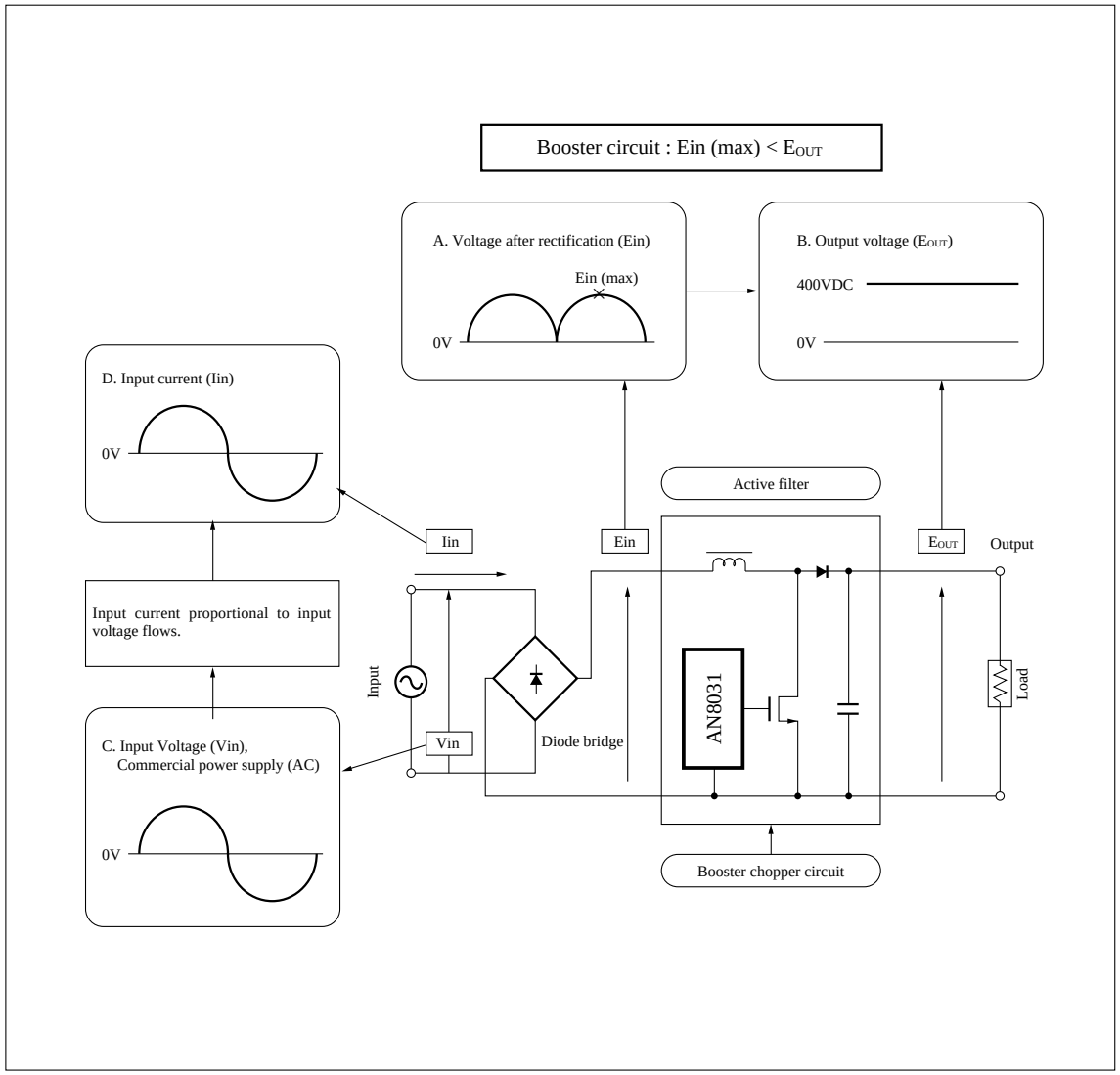


Fig. 1 Application Outline

(2) Control Outline (Refer to Fig.2 and 3)

1) Input (Ein) detection

The voltage which is divided from the input voltage of chopper circuit (Ein) by using external resistor is inputted to the multiplier input terminal of the AN8031 (MPI terminal).

2) Output (Eout) detection

The voltage which is divided from the output voltage of chopper circuit (Eout) by using external resistor is amplified by the error amplifier of the AN8031 (reverse input terminal (EI terminal) for input to another multiplier input (EO terminal, which also functions as output for error amplifier).

3) Multiplication of input voltage and output one

The signals inputted to the multiplier is multiplied and outputted from the multiplier. This output is a signal which monitors both of the input voltage and output one of the chopper circuit.

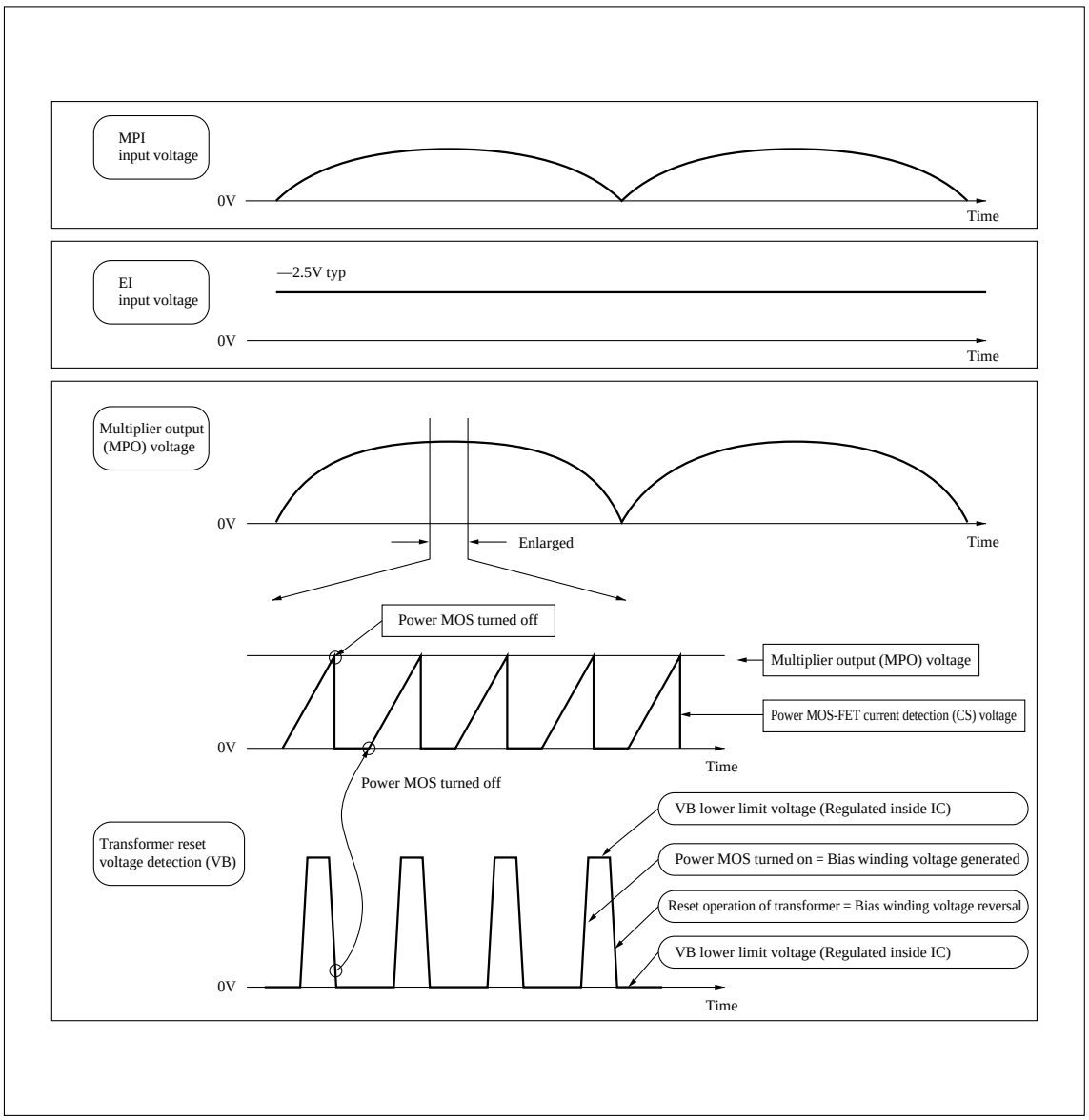


Fig.2 Normal Control Operation

4) Switching device current

The voltage generated in the current detection resistor which is connected to the switching device (power MOS FET) is detected at the CS terminal. In addition, for the above resistor, low resistance is selected, considering the power dissipation.

5) Switching device turning-off

The CS terminal voltage and the multiplier output voltage are compared by the current detection comparator. When the former value gets larger than the latter one, the current detection comparator sends the reset signal to the RS latch circuit to turn off the switching device.

6) Output current supply

When the switching device is turned off, the current flowing in the transformer is cut off. The diode is energized with inertia current of inductor to supply current to the output of chopper circuit (E_{OUT}).

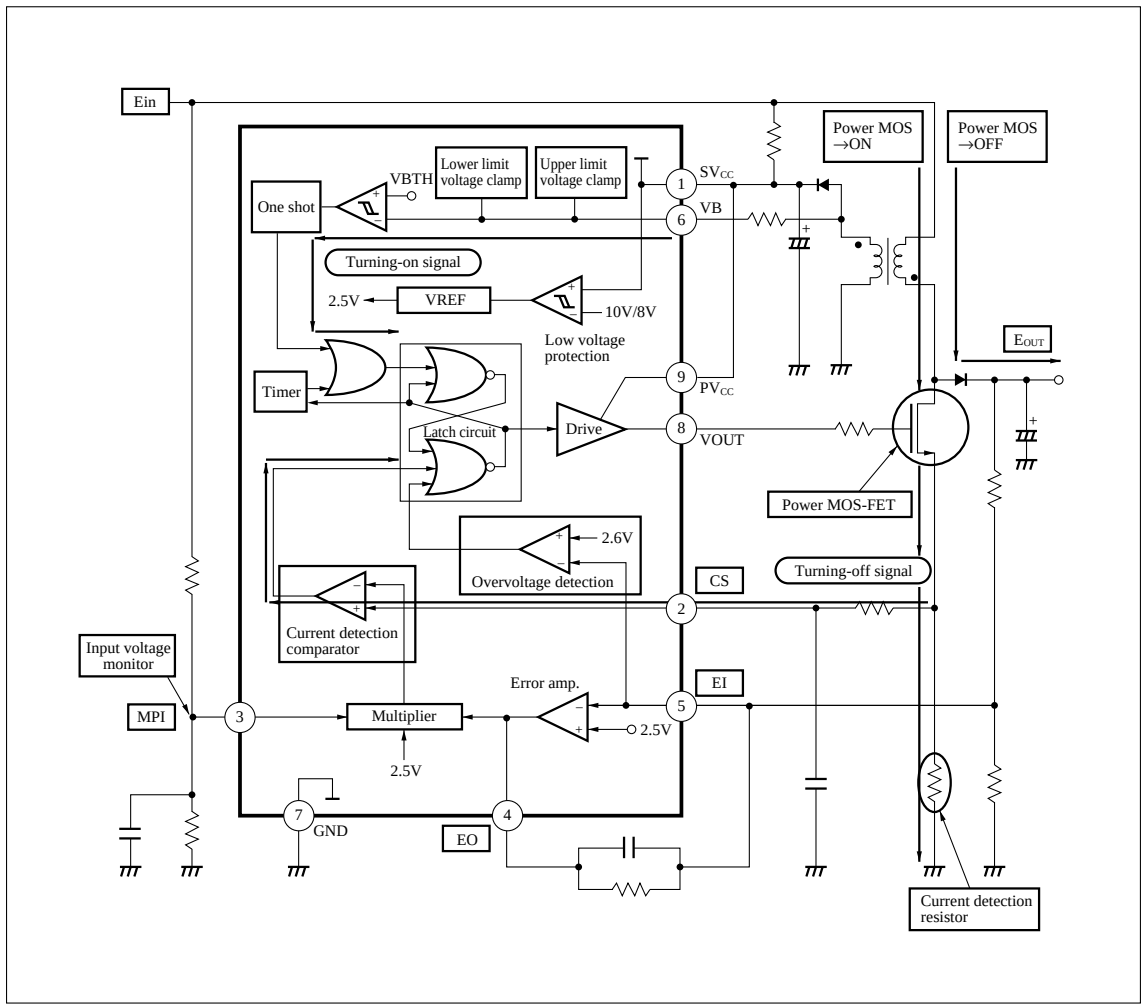


Fig.3 Block Diagram under Normal Operation

7) Transformer reset signal (VB) detection

When the excitation energy is discharged and the inertia current of the inductor is lost, the transformer starts resonance with the frequency which depends on incidental C value of the board or parts and “L” value of the inductor. This operation is detected by the VB terminal through sub-winding provided on the transformer.

8) Switching device turning-off

By resonance, the turning-on signal is sent to the switching device, timing with the operation that the voltage of the sub-winding fluctuates from “H” to “L”.

When the switching device is turned on, current flows in the inductor. Thus the above operation is repeated.

(Summary)

1) When the excitation energy of transformer is lost and the free resonance is started, the switching device is turned on.
2) The switching device is turned on, when the following two elements are crossed : the product of the input voltage (Ein) and output one (Eout) of the chopper circuit and the switching device current.
3) The fluctuation of input voltage and load current is controlled by changing the peak value height of switching device current.
4) The purpose of mixing two signals by using the multiplier :
   1) To stabilize the control system
   2) To reduce the number of parts required

(3) Description of each function

VB

Function

It detects the discharge of the excitation energy of the inductor (reset operation) and turns on the power MOS FET at the next cycle.

Method used

When the inductor is reset, the sub-winding provided on the inductor (bias winding) starts free resonance. It is difficult from the view of withstand voltage to input this voltage directly to the IC. For this reason, it is inputted to the VB terminal through resistor.

Function of upper limit voltage clamper

It prevents the damage due to the voltage of VB terminal exceeding the withstand voltage.

Function of lower limit voltage clamper

It prevents the malfunction due to fluctuation to negative voltage of the VB terminal. (Generally, for the monosilic IC, malfunction such as latch-up is caused when the terminal voltage decreases under-VBE to activate the incidental device.

IC inside

The VB terminal voltage is inputted to the comparator with hysteresis inside the IC. For this reason, if the VB terminal voltage is under the threshold, the power MOS FET is turned on. However, it is preceded by the off-signal which is given to the power MOS FET by the overvoltage protection function, if any.

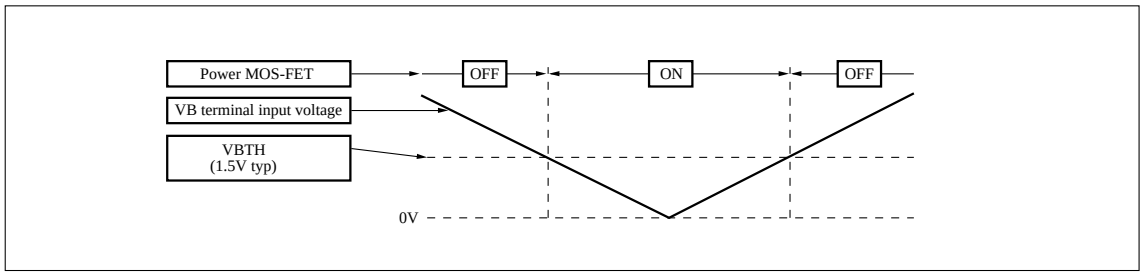


Fig.4 VB Terminal Outline

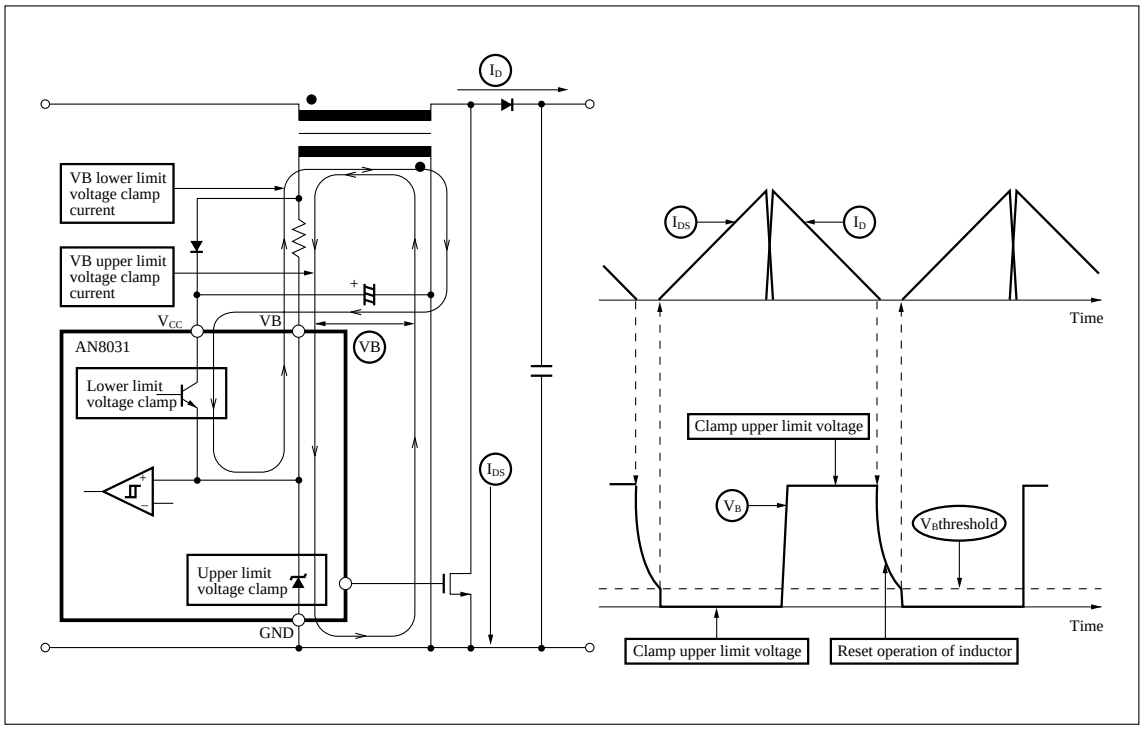
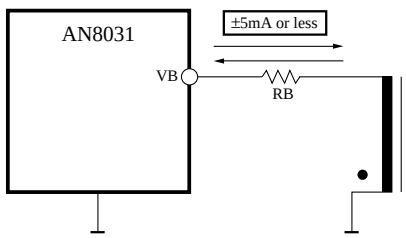


Fig.5 VB Operation

Setting the VB terminal constant

• Regulation with clamper in/out-current value

The allowable output current of the upper limit voltage clamper is –5mA and the allowable input current of the lower limit voltage clamper is +5mA. Either of these allowable values is exceeded, the voltage clamp operation of the VB terminal is not guaranteed. Therefore, RB should be set so that these values could not be exceeded.

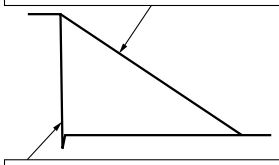


• Consumption current and delay

When the RB value is too large, the VB threshold could be exceeded. When the RB value is too small, the consumption current becomes too large.

In order to determine the RB value properly, the input voltage range and parts dispersion should be taken into consideration and it should be confirmed that stable operation can be ensured under start/overload condition or under small load.

RB too large : Consumption current becomes small, however, TOFF is extended by the delay amount because of low speed.



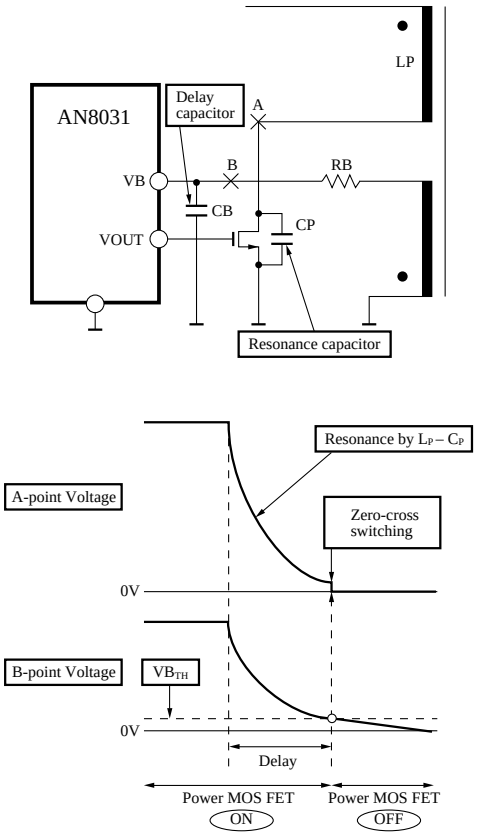
RB too small : Speed is high, however, consumption current is small and undershoot is easy to generate.

• Zero-cross switching

Zero-cross switching can be realized by using the partial resonance at turning-off of the power MOS FET, in order to suppress the dissipation.

The resonance capacitor CP is connected between the drain sources of the power MOS FET. After discharge of accumulation energy of the transformer, resonance with transformer inductance LP in the primary side is produced. Capacitor for delay is connected to the VB terminal so that the next turning-on could occur, timing with the operation that the resonance is produced and the drain voltage of the power MOS FET reaches around 0V.

However, particular care should be taken, because zero-cross conditions could deviate from the theoretical ones since the delay amount fluctuates with the conditions such as input voltage.



CS

This terminal detects the current when the power MOS FET is turned on.

The current which flows when the power MOS FET is turned on is equivalent with the current flowing in the inductor. Therefore, the necessary power value can be controlled by controlling the peak value of the above current.

The input D-range of this terminal is from 0 to 5V. However, since dissipation gets large when the resistance which detects the power MOS FET current is set large, 0.22 to 0.47Ω is recommended for the resistance value, considering relationship with the S/N.

The charging/discharging current for the incidental capacitance which is provided in the power MOS FET, transformer or printed wiring, flows in the power MOS FET detection resistor. This generates noise and may cause malfunction. Therefore, filter should be incorporated to remove such irregular element.

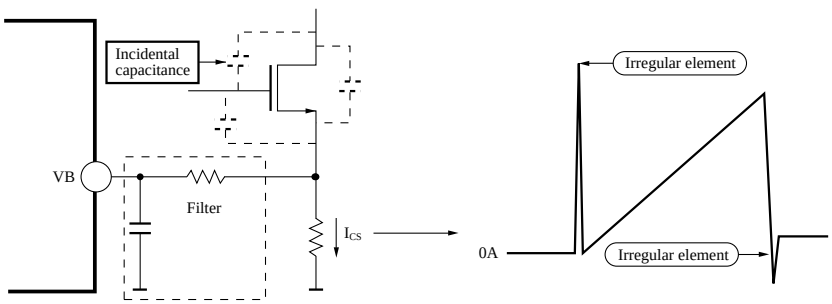


Fig.6 Pin descriptions of CS

MPI

This terminal monitors the AC input voltage. It inputs the voltage which is resistance-divided from the input voltage after full-wave rectification. Input D-range of the multiplier is from 0 to 4.5V^{TYP} and output one is from 0 to 5.4V^{TYP}.

EI/EO

The EI receives input after resistance division of output voltage of the active filter.

The EI is a reverse input for error amplifier. The reference voltage (2.5 V^{TYP}) temperature-compensated is inputted to the non-reverse input.

The error amplifier amplifies the error amount between the output voltage and the reference voltage for output to the multiplier.

Resistor connected between the EI and EO determines the gain of error amplifier.

Resistance divider decreases the output voltage of the active filter to the input D-range of the EI. If miniaturized resistor is used for it to suppress the dissipation, resistance value becomes high because of its high output voltage.

For this reason, particular care should be taken : if the capacitance for phase compensation inserted between the EI and EO is large, the delay element between it and the resistance divider of high resistance becomes large, adversely affecting the characteristics (overshoot or undershoot) at dramatic change of load.

Therefore, the value of the phase compensation capacitance should be set minimum to prevent the oscillation.

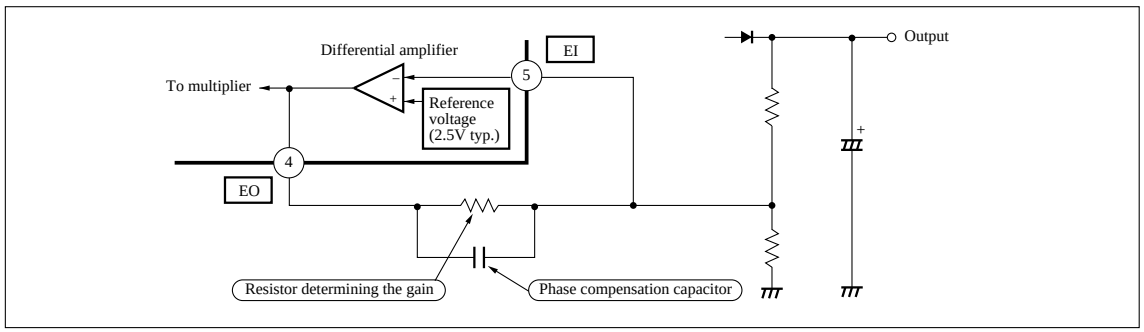


Fig.7 EI/EO Terminal Outline

VOUT

For the drive circuit, the AN8031 employs the totem pole type by which the power MOS FET can be directly driven. Since the peak output current is ±1A, the power MOS FET of TO-220 class can be driven. For the TOP-3 class, the buffer circuit should be added outside because its capability is not sufficient for that class.

The power MOS FET momentarily fluctuates to minus due to incidental capacitance between the drain gates at turning-off. And it may cause malfunction. Therefore, the shottkey diode should be inserted between the VOUT and GND, if necessary.

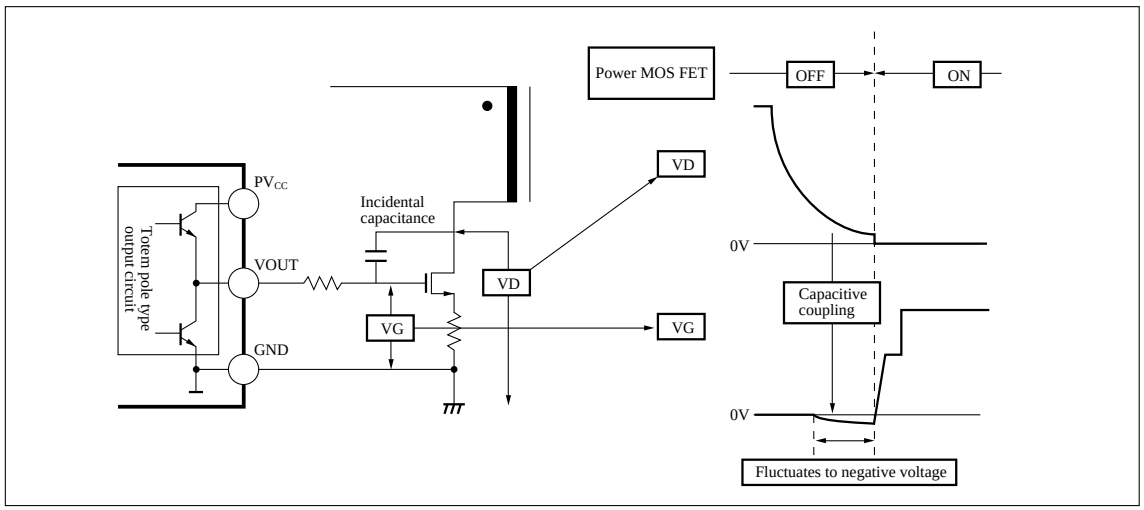
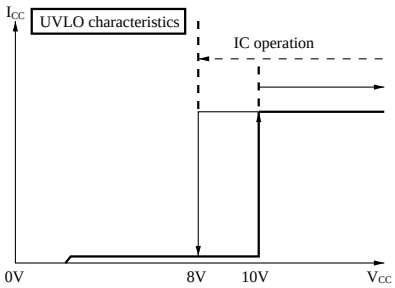


Fig.8 VOUT terminal outline

V_{CC}

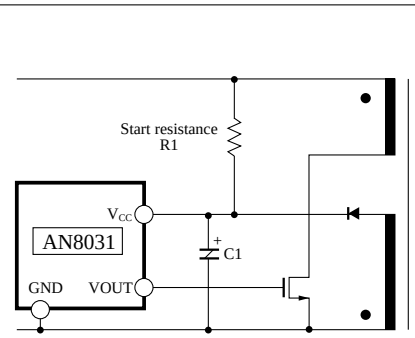
It is a supply terminal for the supply voltage other than the output. The UVLO depends on this V_{CC} voltage. (The characteristics of UVLO are shown in the right figure.)



Precautions on V_{CC} setting methods

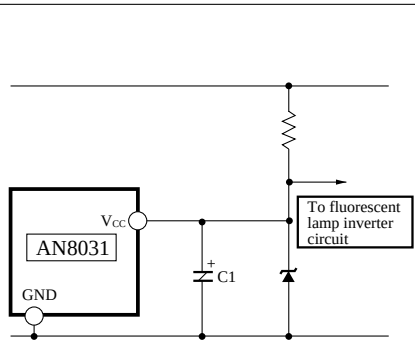
Giving bias from sub-winding

Since the difference between the start voltage ($10V^{TYP}$) and stop voltage ($8V^{TYP}$) is only $2V^{TYP}$, set the value of the C1 shown in the right figure to be large. Otherwise, the IC is hard to start operation.



Giving bias from some other power supply

For the fluorescent lamp inverter circuit, some other power supply is provided in it. Use that power supply.

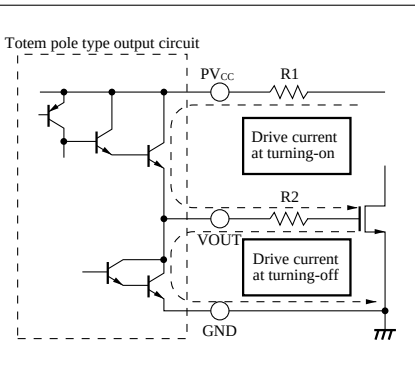


PV_{CC}

It is a drive current supply terminal for the output block.

The “H” voltage of the power MOS FET gate drive pulse depends on its terminal voltage.

In order to limit the power MOS FET drive current, as shown in the right figure R1 is connected to the PV_{CC} terminal and R2 should be connected to the VOUT terminal. By the above connection : R1 and R2 limit the drive current when the power MOS FET is turned on. R2 limits the drive current when it is turned off. Thus, the speed of turning-on and turning-off can be changed.



2. Protective circuit

(1) Timer

For control of the AN8031, the chopper circuit can not start unless the switching device receives the first ON. And, the chopper circuit can not re-start, if the turning-on timing of switching device is missed due to some abnormality.

For this reason, the AN8031 incorporates the timer circuit, with which the start pulse is generated once for approx. 400µs (typ.) when the chopper circuit stops. So, any special external parts are not required (Refer to Fig.9).

However, in order to prevent the output rise of the chopper circuit, the timer circuit does not operate while the overvoltage protector is operating.

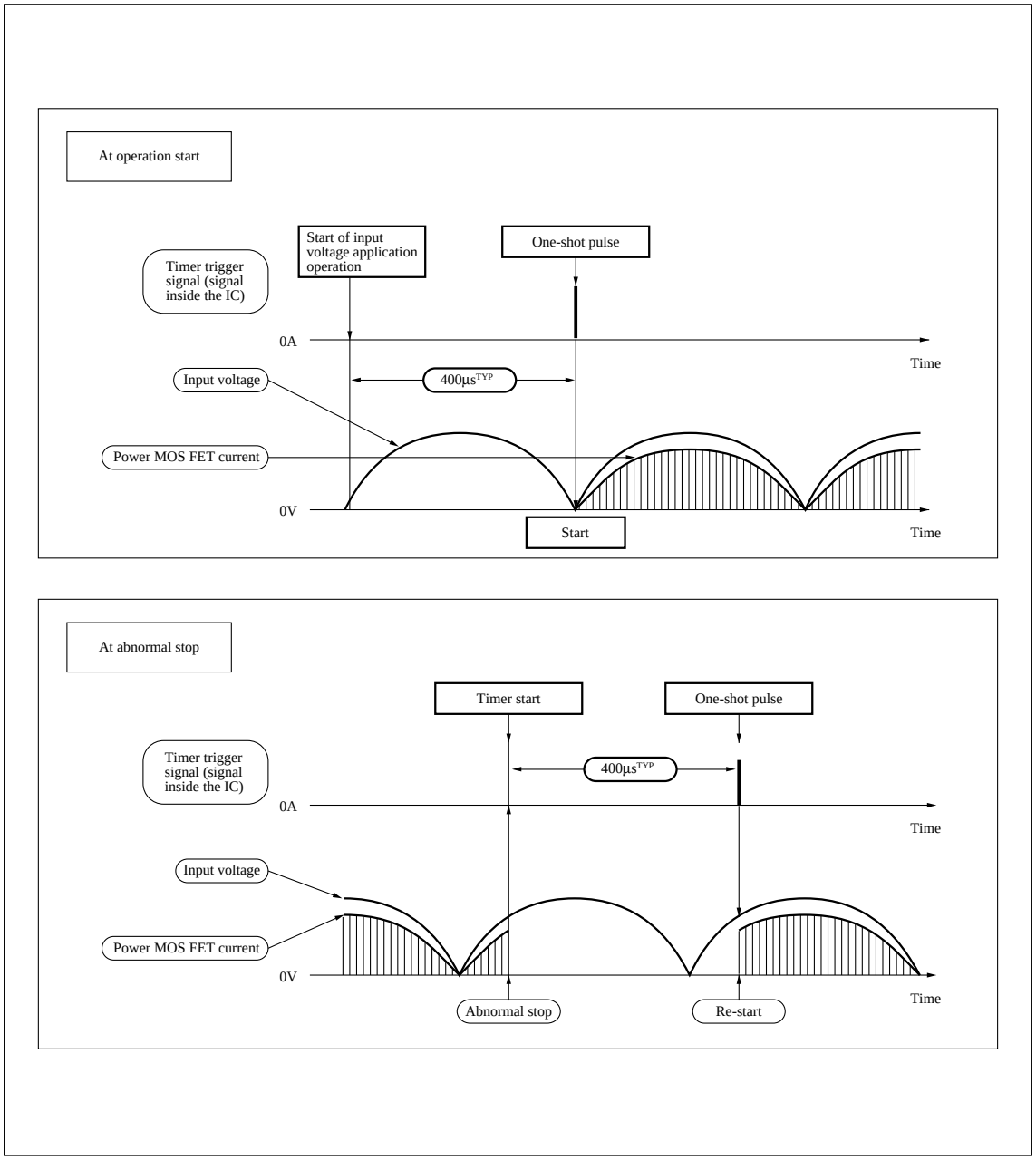


Fig.9 Timer Operation

(2) Overvoltage protection

1) Causes of overvoltage

In the booster chopper circuit, control is made so that the input power could become zero when the load current reaches zero. However, in the actual condition the input power can not be decreased to zero and the output voltage should rise, leaving control.

The above out-of-control condition is created as follows : The operation of the switching device can not be controlled for stop during delay time which exists between the turning-on to the turning-off of the switching device (Refer to Fig.10).

In order to prevent such problem, the AN8031 incorporates the overvoltage protection circuit and the necessary external parts can be much decreased.

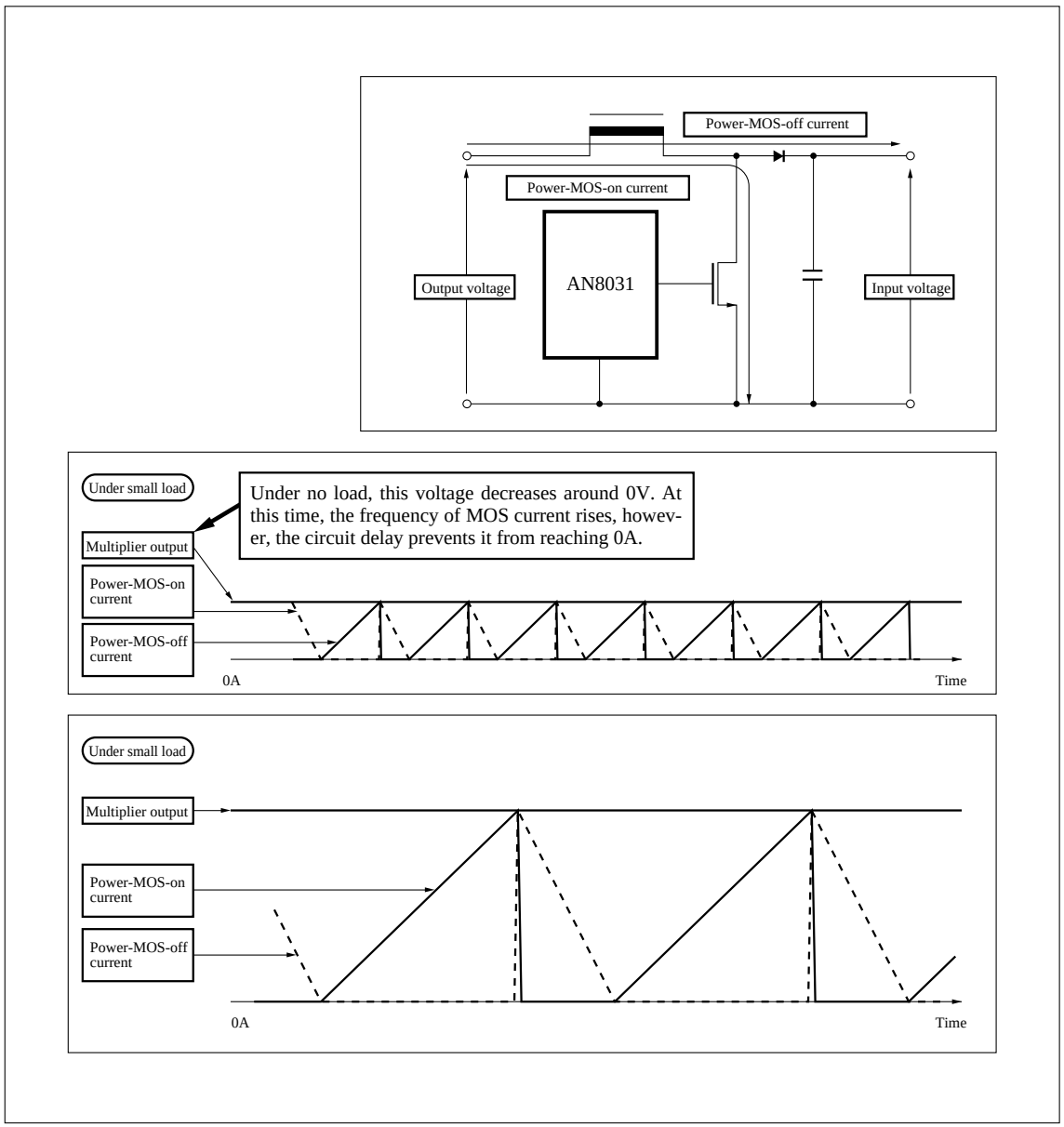


Fig.10 Operation

2) Overvoltage protector operation

For the AN8031, the input of the error amplifier which detects the output voltage also functions as the input of the overvoltage protection comparator. It is different at this point from the AN8032.

The settings are shown in the following :

- Control reference voltage of the error amplifier : 2.50V (typ.)
- Detection voltage of the overvoltage comparator : 2.63V (typ.) < Without hysteresis >

(Voltage 5% higher than the control reference voltage of the error amplifier)

When the output voltage becomes high by 5% or more, comparing with the normal control voltage, the overvoltage comparator operates to cut off the switching device.

When overvoltage is detected, the timer circuit is cut off. It prevents the operation of power MOS FET which increases the output voltage further.

Therefore, under no load, the output voltage of the chopper circuit is stabilized at the value which is 5% higher than the normal control voltage and does not exceed that value (Refer to Fig.11).

In addition, the increase/decrease of the output voltage is created by the offset amount of the overvoltage comparator.

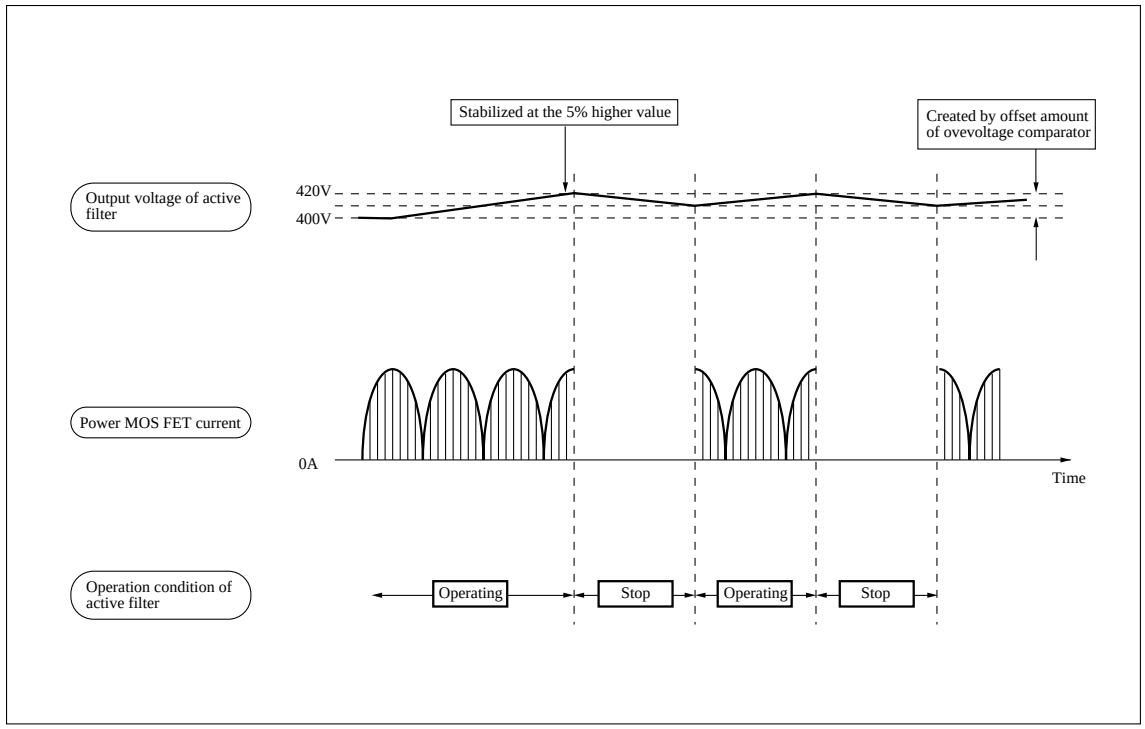


Fig.11 Overvoltage Protection Operation

3) Output voltage overshoot at start

At operation start, the output overload condition is created because the smoothing capacitor which is connected to the output is charged. Under this condition the chopper circuit operates with full power. However, it does not immediately come out of the full-power-operation due to control delay even when the proper output voltage is obtained, causing the overshoot of output voltage.

The AN8031 overvoltage protector operates even at operation starts and prevents the worst cases such as damage of used parts (Refer to Fig.12).

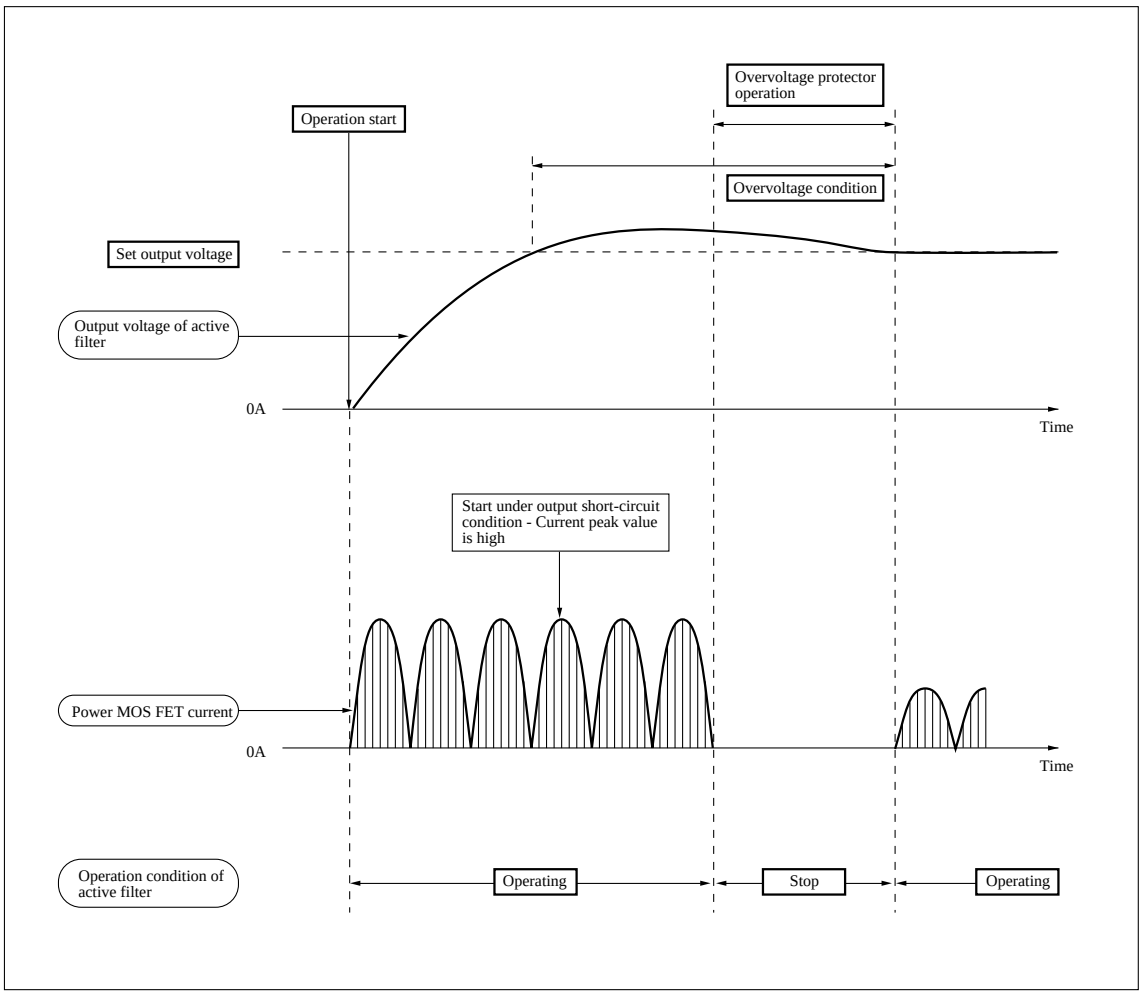
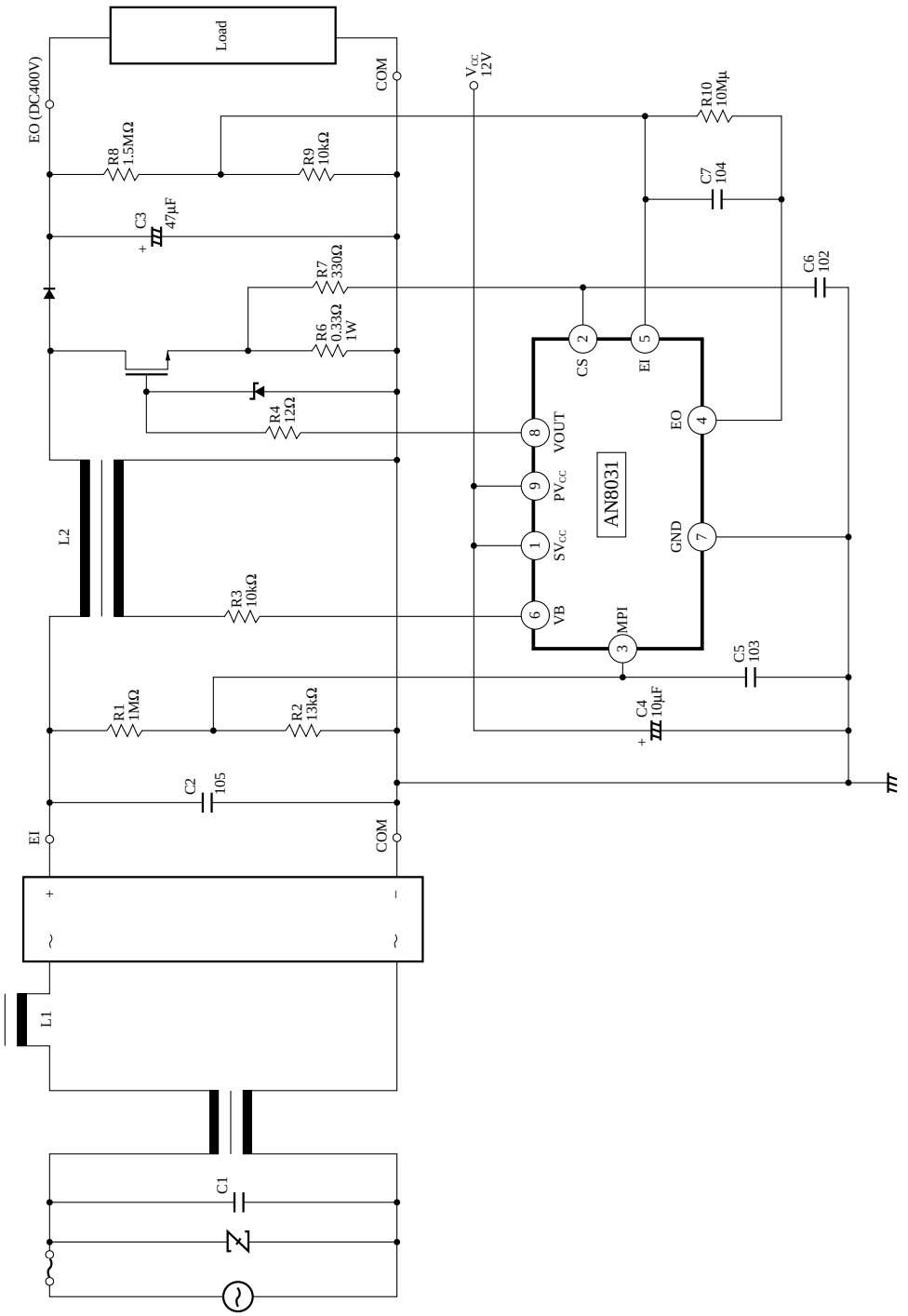
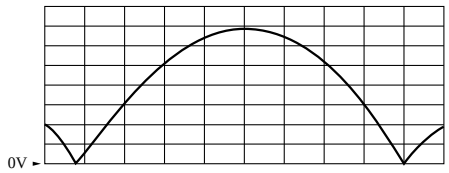
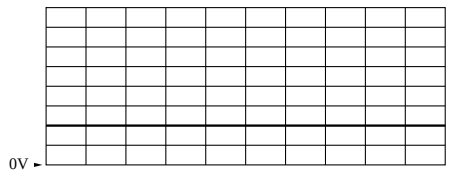
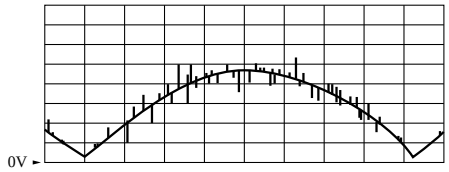
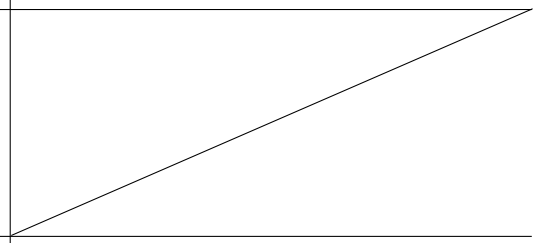
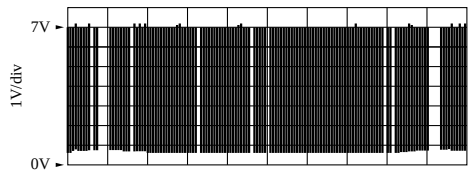
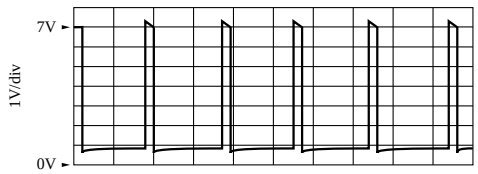
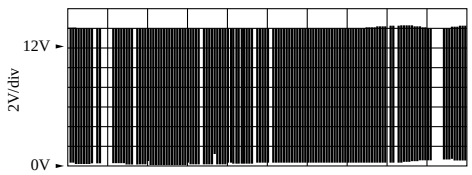
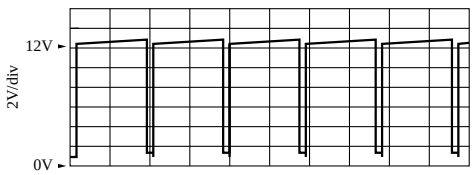
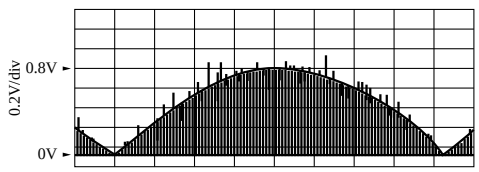
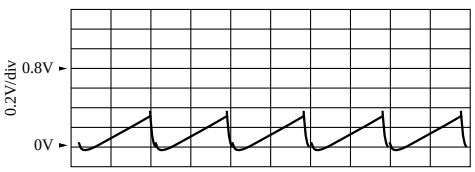
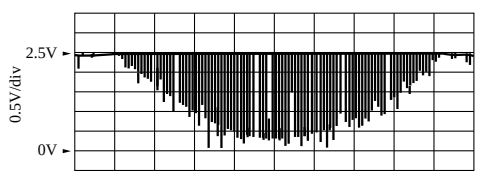
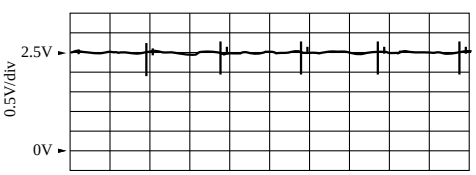
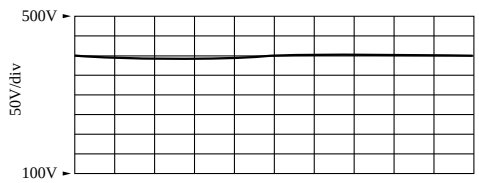
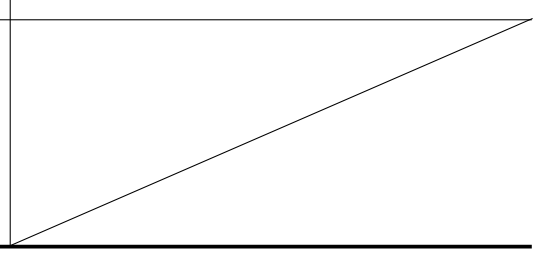


Fig.12 Output Voltage Overshoot at Operation Start

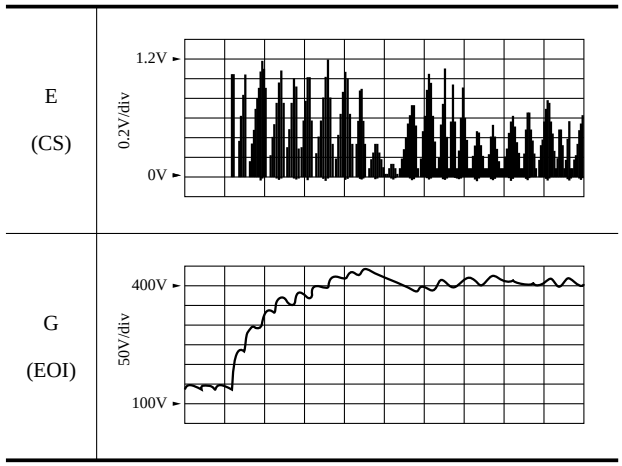
■ Application Circuit



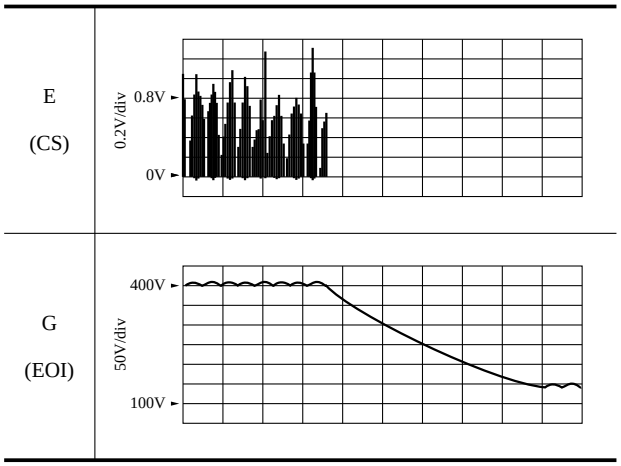
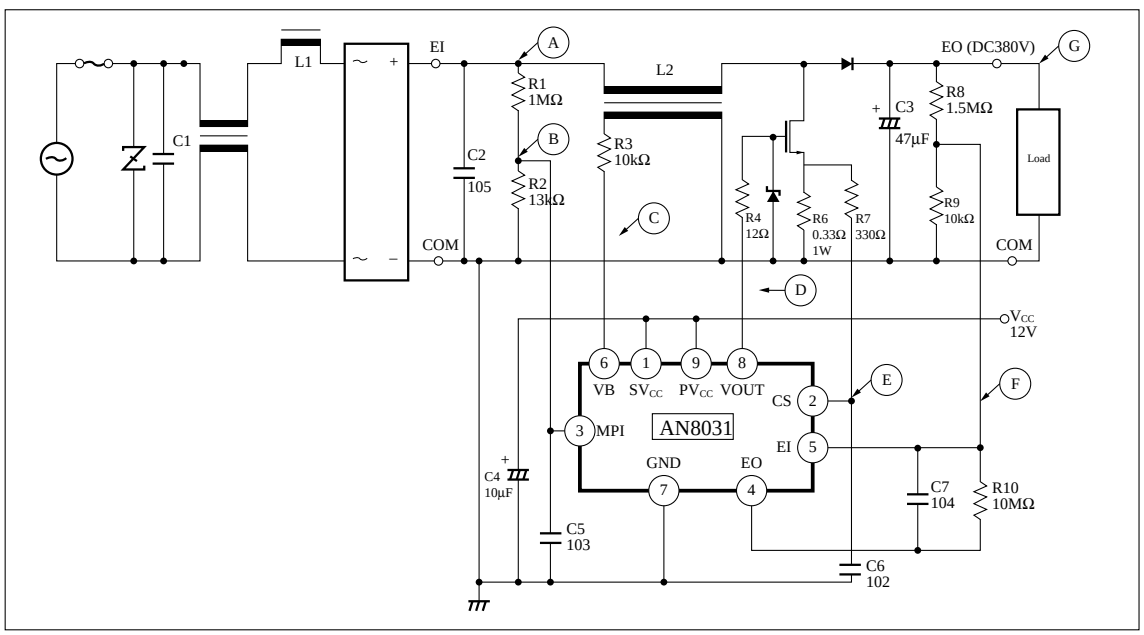
■ Normal Operation Waveform

	1ms/div	10μs/div
A (EIN)		
B (MPI)		
C (VB)		
D (V_{OUT})		
E (CS)		
F (EI)		
G (EO)		

■ Start Waveform (20ms/div)



■ Stop Waveform (20ms/div)



< Conditions >
- Input voltage : 100V (AC)
- Output voltage : 400V (DC)
- Output current : 200mA (Resistance load : 2kΩ)