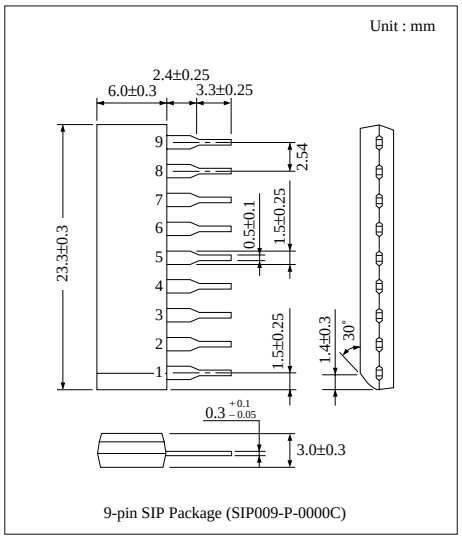
AN8029

Self-excitation RCC Artificial Resonance Type Power-supply Supporting IC for AC-DC Converter Control



9-pin SIP Package (SIP009-P-0000C)

■ Overview

The AN8029 is an IC for controlling the switching power supply, employing the RCC artificial resonance type control method.

It is compact, equipped only with the necessary minimum functions.

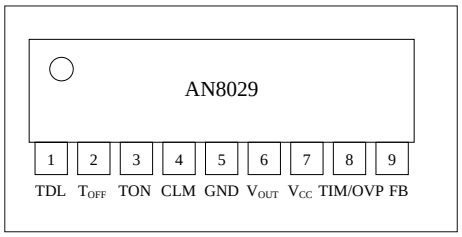
The maximum ON period and the minimum OFF period can be separately set by using the external capacitor and resistor respectively.

It is suitable for the power supply of AV equipment.

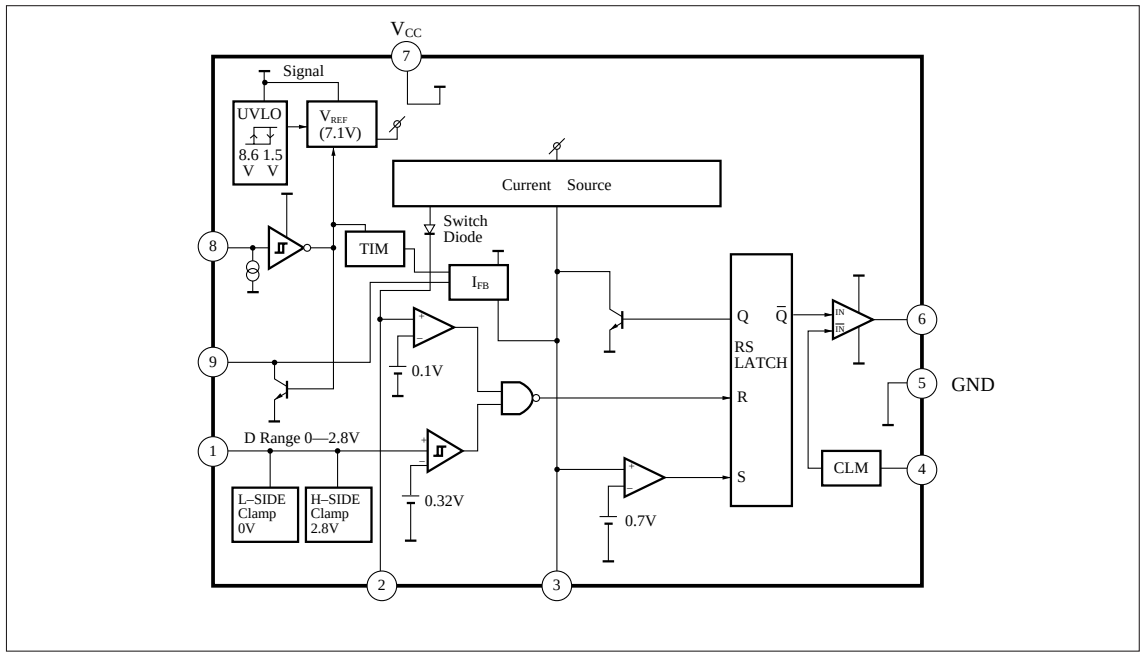
■ Features

- Operating supply voltage range : Stop voltage (8.6V typ.) to 34V
- Output block employing the totem pole system
- Power MOS-FET can be directly driven. (Output peak current :±1A max.)
- Small pre-start operating current (95μA typ.) allows the start resistor to be small-sized.
- Pulse-by-pulse overcurrent protection function built-in
- Incorporated circuit preventing malfunction under low voltage (Start/Stop : 14.9V/8.6V)
- Overvoltage protection function built-in (external reset allowed)
- Timer latch function built-in
- Frequency(VF) control function built-in
- 9-pin SIP package (overseas production allowed) employed

■ Pin Assihnmengs



■ Block Diagram



■ Absolute Maximum Ratings (Ta=25˚C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	35	V
Peak output current	$I_{6\ PEAK}$	±1	A
Power dissipation	P_D	874	mW
Operating ambient temperature	T_{opr}	–30 to + 85	˚C
Storage temperature	T_{stg}	–55 to + 150	˚C

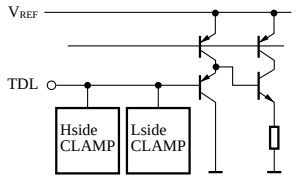
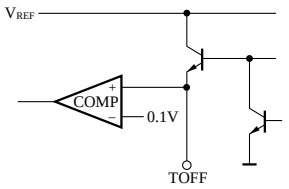
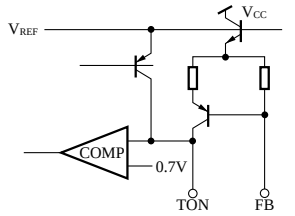
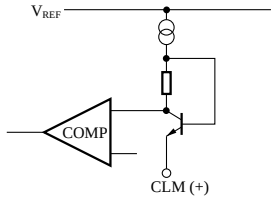
■ Operating Supply Voltage Range

Parameter	Symbol	Range
Supply voltage	V_{CC}	Stop voltage to 34V

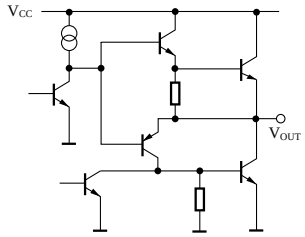
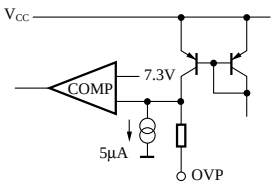
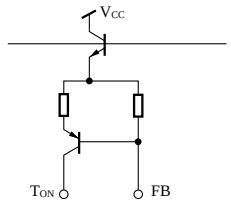
■ Electrical Characteristics (Ta=25±2˚C, V_{CC}=18V)

Parameter	Symbol	Condition	min	typ	max	Unit
UVLO start supply voltage	V_{7START}		13.4	14.9	16.4	V
UVLO operation stop supply voltage	V_{7STOP}		7.7	8.6	9.5	V
UVLO start to stop supply voltage	DV_7		5.7	6.3	6.9	V
OVP operation threshold voltage	V_{8OVP}		6.1	7.3	8.5	V
OVP release voltage	V_{7OVP}		7.4	8.2	9	V
OVP operating circuit current (1)	I_{7OVP1}	V_{CC}=9.1V, V_{OVP}=8.5V	0.56	0.79	1.02	mA
OVP operating circuit current (2)	I_{7OVP2}	V_{CC}=20V, V_{OVP}=8.5V	5.9	7.7	9.5	mA
TDL threshold voltage	V_{1TDL}		0.22	0.32	0.42	V
TDL upper-limit clamp voltage	$V_{1TDL/H}$	I_{TDL}=3mA	2	2.8	3.6	V
TDL lower-limit clamp voltage	$V_{1TDL/L}$	I_{TDL}=–3mA	– 0.3	0	0.3	V
CLM threshold voltage	V_{4CLM}		180	200	220	mV
TON max. ON-period current	I_{3TON}	FB Terminal=open, TON Terminal=GND	–135	–110	–85	V
TON upper-limit voltage	$V_{3TON/H}$	FB Terminal=open	0.55	0.7	0.85	µA
TON lower-limit voltage	$V_{3TON/L}$	FB Terminal=open	– 0.1	0.05	0.2	V
TOFF upper-limit voltage	$V_{2TOFF/H}$		0.7	0.9	1.1	V
TOFF lower-limit voltage	$V_{2TOFF/L}$		– 0.1	0.05	0.2	V
Output oscillation frequency	f_{OSC}	Con=2200pF, Roff=1.5kΩ, Coff=1000pF	55	65	75	kHz
Output current feedback current gain	G_{IFB}	I_{FB}=–1mA	5.05	6.8	8.55	
Output pre-start output L voltage	$V_{6STB/L}$	V_{CC}=10V, I_{OUT}=10mA	—	1	1.25	V
Output L voltage (1)	$V_{6L\ (1)}$	I_{OUT}=10mA	—	0.9	2	V
Output L voltage (2)	$V_{6L\ (2)}$	I_{OUT}=100mA	—	1.1	2.2	V
Output H voltage (1)	$V_{6H\ (1)}$	I_{OUT}=–10mA	15.7	16.5	—	V
Output H voltage (2)	$V_{6H\ (2)}$	I_{OUT}=–100mA	15.5	16.3	—	V
Pre-start circuit current	I_{7STB}	V_{CC}=12V	55	95	135	µA
Circuit current (1)	$I_{7OPR\ (1)}$	V_{CC}=18V, TON Terminal=GND, FB Terminal=open	8.55	11.5	14.3	mA
Circuit current (2)	$I_{7OPR\ (2)}$	V_{CC}=34V, TON Terminal=GND, FB Terminal=open	9.6	12.5	15.4	mA
TDL flowing-out current	I_{1TDL}	V_{TDL}=0.5V	–5	0	—	µA

■ Pin Descriptions

Pin No.	Pin name	I/O	Terminal description	Internal equivalent circuit
1	TDL	I	Transformer reset detection terminal When the transformer reset is detected and "L" is inputted into the terminal, it makes the output of the IC (V_{OUT}) "H" However, it ignores "L" signal, which is under the minimum off-time dete-rmined in the $T_{OFF.}$	
2	T_{OFF}	—	Terminal connecting the resistance and capacitance which determine the minimum off-time ("L") of the IC output (V_{OUT}) . For the minimum off-time (t_{OFF}) , the reference calculation is as follows : $t_{OFF}=2.2 \times C \times R$ C : External capacitance R : External resistance	
3	T_{ON}	—	Terminal connecting the capacitance which determines the maximum on-time ("H") of the IC output. For the maximum on-time (t_{ON}),the reference calculation is as follows : $t_{ON}=6500 \times C$ C : External capacitance	
4	CLM	I	Input terminal for detection of the pulse-by-pulse overcurrent protection normally, it is recommended to add a filter externally.	
5	GND	—	GND terminal	

■ Pin Descriptions (cont.)

Pin No.	Pin name	I/O	Terminal description	Internal equivalent circuit
6	V_{OUT}	O	Output terminal for direct drive of the power MOS FET It uses the totem pole type output. The maximum rating of the output current : (Peak)±1A (DC)±150mA	
7	V_{CC}	—	Power supply voltage application terminal. It monitors the supply voltage and has the operation threshold of start/stop/Over reset.	
8	TIM/OVP	I	Double functions : OVP (Overvoltage protection) and timer latch terminal 〈OVP〉 When the overvoltage signal of the supply voltage is received and "H" is inputted in the terminal, it turns off the circuit and at the same time keeps this condition (latch). To reset the OVP latch, the V_{CC} should be dec-reased under the release voltage. 〈Timer larch〉 It detects the output voltage fall due to the overcurrent condition of the power supply output with the current level IFB-inputted. When the I_{IFB} decreases under the current of certain value, the charging current flows in the capacitor which is connected to this terminal. Then, when the capacitor is charged up to the threshold voltage of the OVP, the OVP works so that the IC could keep the operation stop condition.	
9	FB	I	Terminal connecting the photo-coupler for error voltage feedback of the power supply output. Cancellation of about 180µA is possible for the photocoupler dark current.	

■ Operation Description

• Start/stop circuit block

(Start mechanism)

When AC voltage is applied and the supply voltage reaches the start voltage with current from the start resistance, the IC starts operating. Then the power MOS-FET driving starts. Thereby, bias is generated in the transformer and the supply voltage is given from the bias winding to the IC (Refer to Point a) in Fig.1).

During the period from the time when the start voltage is reached and the voltage generates in the bias winding to the time when the IC is provided sufficient supply voltage, the supply voltage of the IC is supplied by the capacitor connected to V_{CC} (C8).

Since during the above period the supply voltage continuously decreases (Area b in Fig.1), the power supply can not start (c in Fig.1), if the stop voltage of the IC is reached before the sufficient supply voltage is supplied from the bias winding.

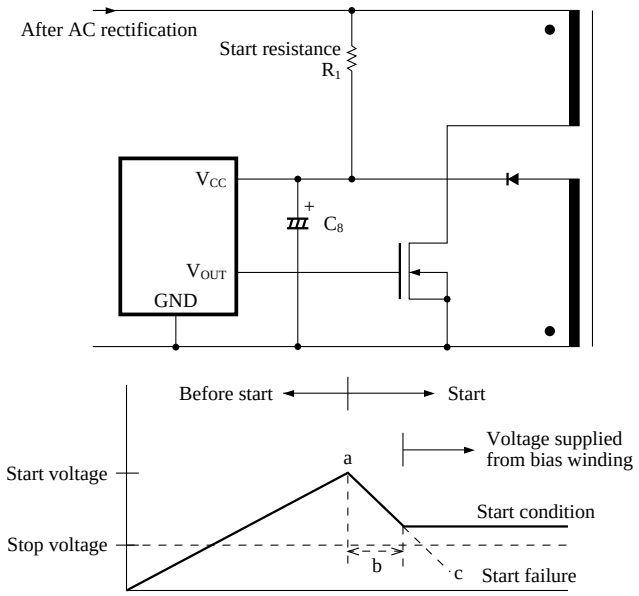


Fig.1

(Function)

The start/stop circuit block works, monitoring the V_{CC} voltage, so that the IC operation can start when V_{CC} voltage reaches the start voltage (14.9V typ.) and it can stop when it decreases under the stop voltage (8.6V typ.). It is easy to make selection for the start resistor and the capacitor connected to V_{CC}, by providing the large voltage difference between start and stop (6.3V typ.).

*Since the high voltage is applied to either end of the start resistor, the current flowing in the resistor should be suppressed to the minimum (so that the start resistor can be small-sized).

By setting the pre-start current to low value (95μA typ.), the temperature fluctuation and dispersion is suppressed.

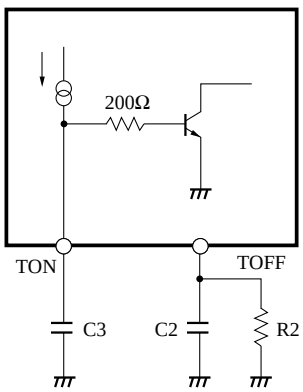
Also, by decreasing the bias current, the capacitor connected to V_{CC} can be small-sized.

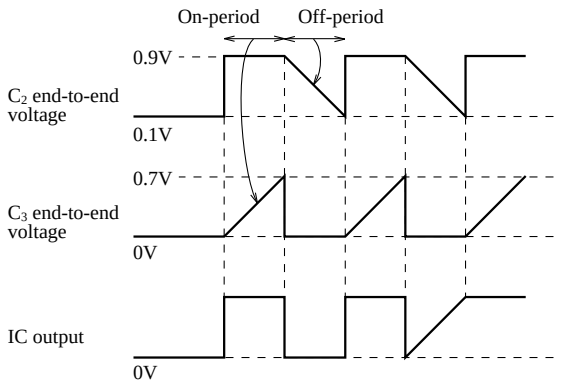
• Oscillation circuit

The oscillation circuit generates the pulse signal for turning on/off the power MOS FET, through charging/discharging of the C2, R2 and C3 which are connected to TOFF (Pin2), TON (Pin3) respectively.

The constant voltage control at the time of making up the switching power supply considers the off-time of the power MOS FET to be fixed and is achieved by changing the on-time. This on-time control directly changes the output pulse width of the oscillation circuit.

During the on-time of the power MOS FET, the C2 is charged to the constant voltage (approx. 0.9V).
On the other hand, the C3 is charged from almost 0V by the charging current from the TON terminal. When the end-to-end voltage of the C3 reaches approx. 0.7V (Ta=75˚C), the oscillation circuit output reverses to turn off the power MOS FET. At the same time, the C3 is rapidly discharged by the discharging circuit inside the IC and its end-to-end voltage becomes almost 0V. The charging current from the TON terminal is changed by the feedback signal to the FB terminal (Pin9) (Details are described below.)





The following shows the reference calculation for the maximum on-time of the power MOS FET :

$$TON\ (max.) = 6500 \times C3$$

When the power MOS FET is turned off, the TOFF terminal gets high impedance and the C2 starts discharging by the R2. When the end-to-end voltage of the C2 decreases to approx. 0.1V, the oscillation circuit output reverses again to turn on the power MOS FET. At the same time, the C2 is rapidly charged to approx. 0.9V. The following shows the reference calculation for the minimum off-time fixed with the C2 and R2:

$$TOFF\ (min.) = 2.2 \times C_2 \times R_2$$

However, when the voltage time feedbacked to the TDL terminal (Pin1) is longer than the TOFF time depending on the C2 and R2, the off-time for the artificial resonance circuit operation described below is determined by the former value. The above operation is repeated and turning-on/off of the power MOS FET continues. Fig.2 shows the oscillation waveform at the time when the TDL terminal is helped-down to the GND.

• Power supply output control system (FB : Feedback)

The constant voltage control of the power supply output considers the off-time of the power MOS FET to be fixed and is achieved by changing the on-time. The control of on-time is done by changing the charging current from the TON terminal to the C3, through the following process : The photocoupler connected to the FB terminal (Pin9) absorbs from the FB terminal, the feedback current which is corresponding to the output signal of the output voltage detection circuit provided in the secondary side output. The current approx.7 times the current flowing from the FB terminal flows from the TON terminal as the charging current for the C3 (Refer to Fig.3).

The higher the AC input voltage of the current becomes, or the smaller the load current becomes, the larger the flowing-out current from the FB terminal gets. When the flowing-out current from the FB terminal gets larger, the C3 charging time becomes shorter and the ON time becomes shorter.

In addition, the system has cancellation capability of about 180μA for the dark current of the photocoupler (Refer to Fig.4).

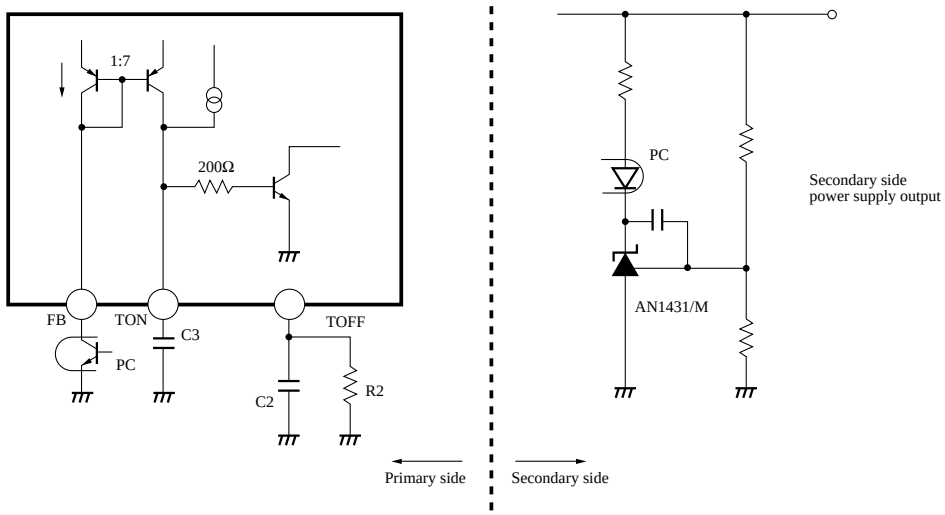


Fig.3 Power Supply Output Control System

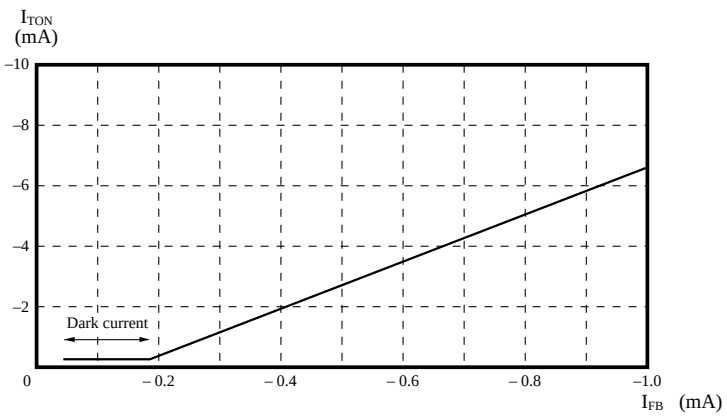


Fig.4 Feedback Current versus Charging Current Characteristics

• Artificial Resonance Operation (Power MOS FET Turning-on Delay Circuit)

For the AN8029, the artificial resonance operation can be obtained by making connection as shown in Fig. 5. The C7 is a resonance capacitor and the R9 and C9 constitute the delay circuit for regulating turning-on of the power MOS FET. When the power MOS FET is turned off, the voltage which generates in the drive winding is inputted to the TDL (Time Delay) terminal (Pin 1) through the R9 and C9. While the "H" signal (threshold voltage : 0.32V or more) is inputted, the power MOS FET remains off. Also, the TDL terminal has the H/L-side clamp capability. For the upper limit, clamping is done at 2.8V (typ.) (sink current : –3mA). For the lower limit, clamping is done at approx. 0V (typ.) (source current : 3mA). The off-time of the power MOS FET depends on the shorter time among the following : The time required for the TDL terminal input voltage to exceed the threshold voltage, and the TOFF time (min.) of the internal oscillation circuit (Refer to description on the oscillation circuit.) In addition, the TDL terminal input voltage starts to decrease, when the transformer starts resonance operation and the drive winding voltage gets lower.

The constants of the R9 and C9 should be selected to determine the delay time so that the power MOS FET be turned on at 1/2 cycle of resonance frequency. Setting the zero voltage turning-off in the voltage waveform is helpful to do this selection (Refer to Fig. 6).

The approximate value of resonance frequency can be given as follows :

$$f_{SYNC} = \frac{1}{2\pi\sqrt{L \cdot C}} \text{ [Hz]}$$

C : Resonance capacitance

L : Transformer primary side inductance

Therefore, the turning-on delay time tpd (ON) for turning-on the power MOS FET at 1/2 cycle of resonance frequency is :

$$\text{tpd (ON)} = \pi\sqrt{L \cdot C} \text{ [s]}$$

• Precautions on R9/C9 selection

If too low resistance is selected for the R9, the flowing current into the TDL terminal after start of the power supply exceeds the maximum rating value. It may result in the malfunction and in the worst case the used parts are damaged. It is recommended that about 8 to 10kΩ be selected for the R9, though it depends on the supply voltage from the bias winding.

Therefore, the resonance capacitance and inductance of the transformer used should be taken into the calculation. The tpd (ON) should be regulated with the C9.

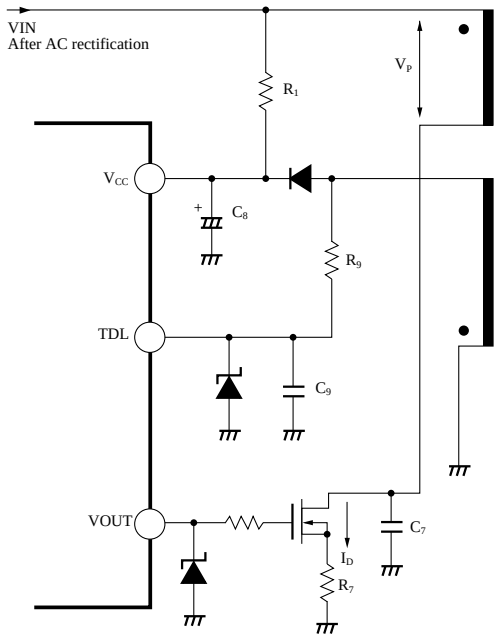


Fig.5

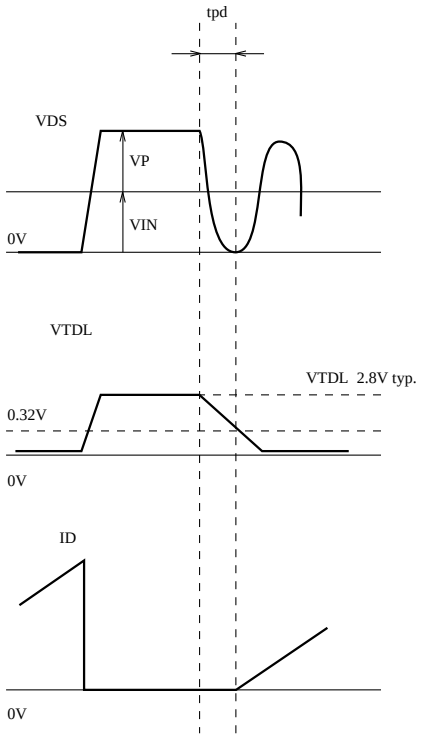


Fig.6

• Overcurrent Protective Circuit

The overcurrent of the power supply output is proportional to the value of current flowing in the main switch in the primary side (the power MOS FET). Taking advantage of the above fact, by regulating the upper limit of the pulse current flowing in the main switch, the circuit protects the parts which are easily damaged by the overcurrent.

For the current flowing in the main switch, the current detection is achieved by monitoring the voltage in either end of the low resistance, which is connected between the source of power MOS FET and the power supply GND. When the power MOS FET is turned on and the threshold voltage of CLM (Current Limit) is detected, the overcurrent protective circuit controls so that current can not further flow, by turning off the output to turn off the power MOS FET. The threshold voltage of CLM is approx. 0.2V (typ.) under Ta=25˚C with respect to GND of the IC. This control is repeated for each cycle. Once the overcurrent is detected, the off condition is kept during that cycle and it can not be turned on until the next cycle. The overcurrent detection method described in the above is called “Pulse-by-pulse overcurrent detection.”

The R6 and C6 in Fig. 7 constitute the filter circuit, which functions to remove the noise generated by the incidental capacitance which equivalently accompanies turning-on of the power MOS FET. For overcurrent detection resistance R7, the carbon resistor should be used but not the winding resistor, because the high-frequency current flows in it.

For the earth point, it is recommended that GND of the IC and GND of the AC rectifier capacitor should be connected with the shortest earth wire.

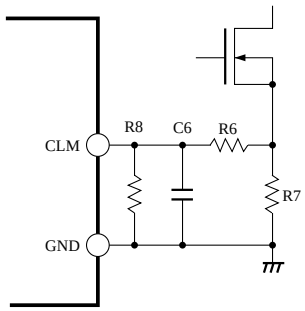


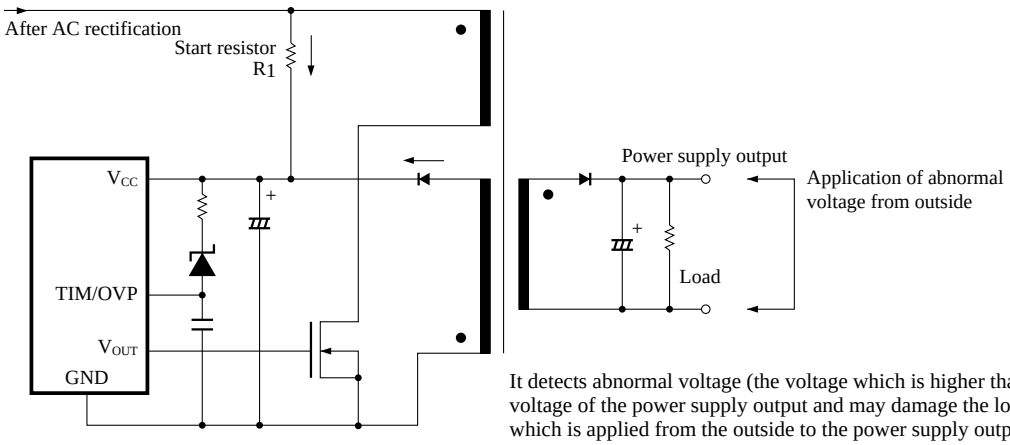
Fig. 7

[Accuracy of detective level]

This overcurrent detection level reflects on the operating current level of the power supply overcurrent protection. Therefore, if this detection level fluctuates with temperature or dispersion, the operating current level of the power supply overcurrent protection also fluctuates. Since such level fluctuation means increased necessary withstand amount of used parts and in the worst case their breakage, the accuracy of detection level is raised as far as possible for the AN8029 (Approx. ±4%).

• Overvoltage protective circuit (OVP)

OVP is an abbreviation of “Over Voltage Protection.” It refers to a self-diagnosis function, which stops the power supply to protect the load, when the power supply output generates abnormal high voltage higher than the normal output voltage due to error of the control system or application of abnormal voltage from outside (Refer to Fig. 8).



It detects abnormal voltage (the voltage which is higher than voltage of the power supply output and may damage the load) which is applied from the outside to the power supply output, in the primary side of the bias winding to operate the OVP.

Fig. 8

Basically, it is set to monitor the voltage of supply voltage V_{CC} terminal. Normally, the V_{CC} voltage is supplied from the transformer drive winding, and this voltage is proportional to the secondary side output voltage. Therefore, when the secondary side output has overvoltage, it also operates.

(1) When as a result of the power supply output abnormality, the voltage inputted to the OVP terminal exceeds the threshold voltage (7.3V typ.), the protective circuit shuts down the internal reference voltage of the IC to stop all the control and keeps this stop condition.

(2) The OVP reset is done by decreasing the supply voltage (V_{CC} < 8.2V typ. : OVP release supply voltage).

1. When the supply voltage becomes lower than the stop voltage,
2. When the supply voltage becomes lower than the OVP release voltage,

The discharging circuit is incorporated so that the electric charge which is charged in the capacitor connected to the OVP terminal can be discharged for the next re-start.

$$V_{th\,(OUT)} = \frac{\text{Secondary side output voltage under normal operation V (OUT)}}{V_{CC}\text{ terminal voltage under normal operation}} \times V7$$

$$V_7 = V_{th\,(OVP)} + Vz$$

$V_{th\,(OUT)}$: Secondary side output overvoltage threshold
$V_{th\,(OVP)}$: OVP operation threshold
V_z : Zener voltage (external parts of OVP terminal)

(Operating supply current characteristics)

While the OVP is operating, if the supply current decreases, the rise of the supply voltage V_{CC} may be resulted in, and in the worst case the guaranteed withstand voltage of the IC (35V) can be exceeded. In order to prevent the rise of supply voltage, the IC is provided such characteristics as that the supply current can rise only in the constant resistance mode. This characteristics ensure that the OVP can not be released unless the AC input is cut, if the supply voltage V_{CC} under OVP operating gets stabilized over the OVP release supply voltage (which depends on start resistor selection). Refer to Fig. 9.

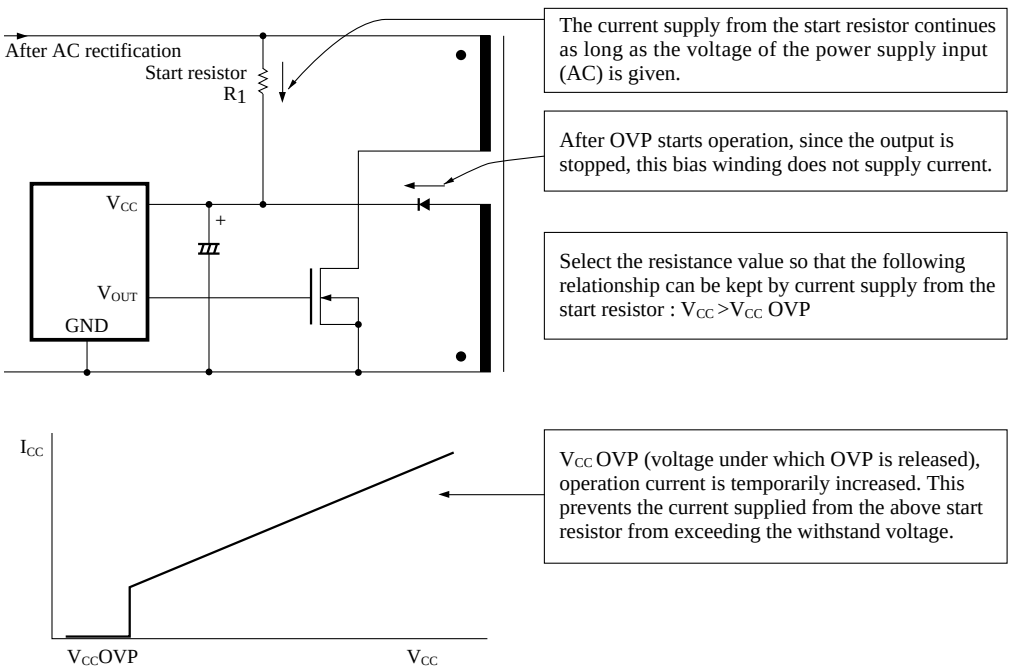


Fig. 9

• Timer Latch

When the short-circuit or overload of the power supply output continues for a certain period, the pulse-by-pulse overcurrent protection is not sufficient for protection of the transformer, and Fast Recovery Diode (FRD) and Shottkey Diode in the secondary side as well as the power MOS FET. For this reason, the timer latch function is employed, which stops the power supply by hitting the OVP, when the overcurrent condition continues for a certain period.

The short-circuit or overload of the power supply output is monitored as the decrease of the power supply output (at this time the pulse-by-pulse overcurrent protector is in the operating condition). The decrease of the power supply output is detected as the decrease of current amount from the current feedback terminal of the normal PWM control. When the decrease amount of this current exceeds a certain value, the comparator inside the IC reverses to flow the constant current to the TIM/OVP terminal.

The external capacitor is connected to the TIM/OVP terminal. Electric charges are accumulated in this capacitor to rise the OVP terminal voltage. When the OVP operating threshold voltage (7.3V typ.) is reached, the OVP starts operating to stop the IC and keeps this stop condition (Refer to Fig. 10).

(Timer period)

The period from the time when an error of the power supply output is detected to the time when the OVP starts operation (hereinafter referred to as “timer period”) should be longer than the rise time of the power supply. Since at operation start the IC is in the same condition as the overload or output short-circuit condition, if the timer period is shorter, the power supply works latch and can not start.

Therefore, the IC is designed so that the timer period can be set to any desired value with capacitance value of the external capacitor connected to the TIM/OVP terminal. However, particular care should be taken, because too large value of this capacitance may cause the breakdown of the power supply.

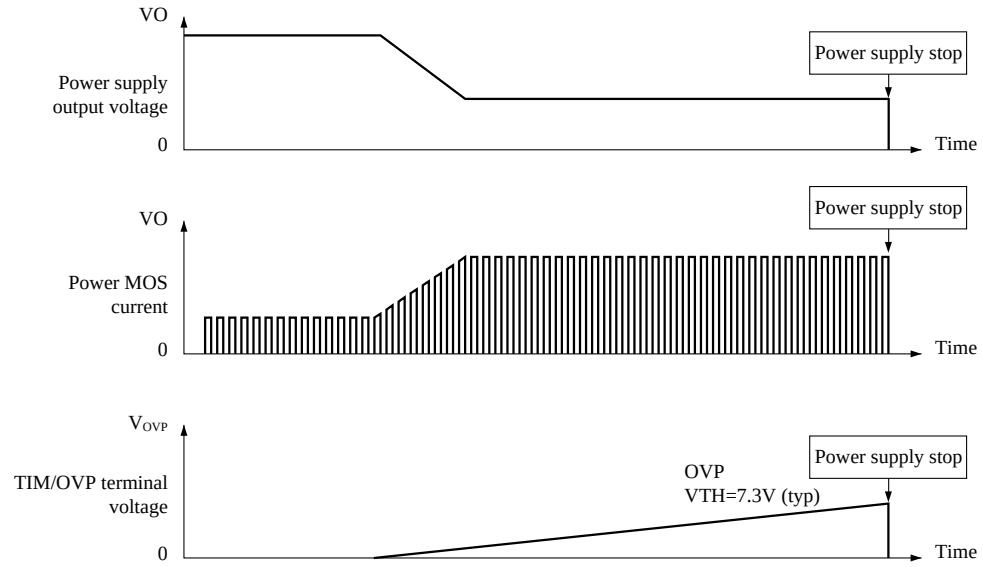


Fig. 10 Timer Latch Basic Operation

• Output Block

The AN8029 employs the output circuit using the Totem Pole (Push-Pull) method, by which sink/source of current is performed with the NPN transistor as shown in Fig. 9, in order to drive the power MOS FET at high speed.

The maximum sink/source current is ±0.1A (DC) and ±1.0A (PEAK). Even when the supply voltage V_{CC} is under the stop voltage, the sink function works to ensure that the power MOS FET be turned off.

For the current capability, the peak current is mainly considered, and the particularly large current is not required on the constant base : The power MOS FET which works as load on the output is capacitive load. Therefore, in order to drive it at high speed, the large peak current is required. However, after charging/discharging particularly large current is not required to keep that condition.

For the AN8029, capacitance value of the power MOS FET used is taking into account, and the capability of peak value ±1A is ensured.

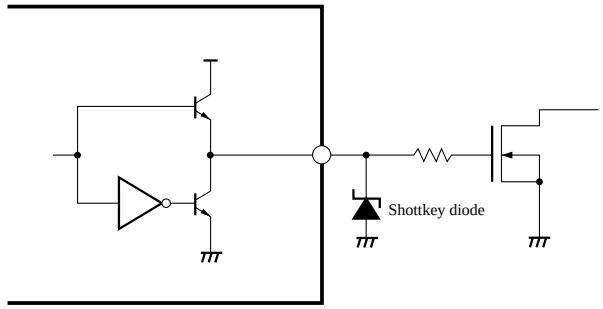


Fig. 11

The incidental LC of the power MOS FET may produce ringing to decrease the output PIN under the GND potential. When the decrease of the output PIN gets larger than the voltage fall of diode and its voltage becomes negative, the incidental diode consisting of the substrate and collector of the output NPN turns on. This phenomenon can cause the malfunction of device. In such a case, the shottkey clamp diode should be connected between the output and GND.

•Reference Materials for Design

Using the soft start function with external parts

The power supply rises under overload condition due to the capacitance connected to the power supply output. In this condition, the voltage of the power supply output is low. The normal constant voltage control attempts to rise the power supply output at the maximum duty. The control uses the pulse-by-pulse overcurrent protection, attempting to limit the current. However, pulses can not be made down to zero due to delay of filter, etc. As a result, large current flows in the main switch (the power MOS FET) or the diode in the secondary side, and in the worst case these parts are damaged. For this reason, the soft start function is used to suppress the rush current at start of the power supply.

As shown in Fig. 2 the R3 and C4 are connected between the FB terminal (Pin9) and the GND terminal (Pin5) to use the soft start function. When the supply voltage of the IC reaches the start voltage and the start circuit begins operation, the open bias is outputted to the FB terminal. By this voltage, the charging current flows in the C4 to become flowing-out current of the FB terminal (I_{FB}) and output control begins under the condition in which TON period is short. The I_{FB} decreases with elapse time, since it changes proportionally to the charging current of the C4. The CLM circuit operates, depending on the sum of the R7 end-to-end voltage by the current which flows in the power MOS FET at power-on and the R6 end-to-end voltage by the charging current of the C4.

Therefore, since the current which flows in the power MOS FET at power-on gradually increases, the rush current can be suppressed.

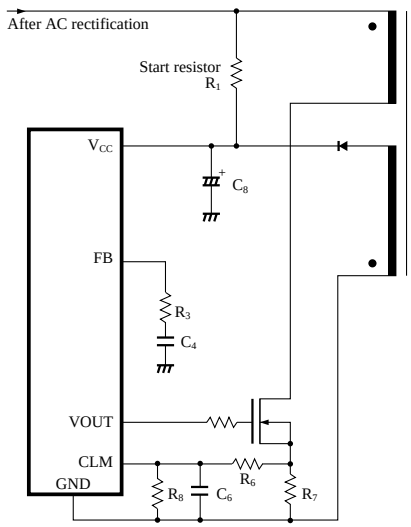


Fig. 12

■ Application Circuit (RCC)