LAMBDA ADVANCED ANALOG INC.

AHE281XD Series

Dual Output, Hybrid - High Reliability
DC/DC Converter

DESCRIPTION

The AHE Series of DC/DC converters feature high power density and an extended temperature range for use in military and industrial applications. Designed to MIL-STD-704 input requirements, these devices have nominal 28VDC inputs with ±12V and ±15V dual outputs to satisfy a wide range of requirements. The circuit design incorporates a pulse width modulated push-pull topology operating in the feed-forward mode at a nominal switching frequency of 250KHz. Input to output isolation is achieved through the use of transformers in the forward and feedback circuits.

The advanced feedback design provides fast loop response for superior line and load transient characteristics and offers greater reliability and radiation tolerance than devices incorporating optical feedback circuits.

Manufactured in a facility fully qualified to MIL-PRF-38534, these converters are available in four screening grades to satisfy a wide range of requirements. The CH grade is fully compliant to the requirements of MIL-PRF-38534 for class H. The HB grade is processed and screened to the class H requirement, but may not necessarily meet all of the other MIL-PRF-38534 requirements, e.g., element evaluation and Periodic Inspection (P.I.) not required. Both grades are tested to meet the complete group "A" test specification over the full military temperature range without output power deration. Two grades with more limited screening are also available for use in less demanding applications. Variations in electrical, mechanical and screening can be accommodated. Contact Lambda Advanced Analog for special requirements.

FEATURES

- **17 To 40 Volt Input Range (28VDC Nominal)**
- **± 12 and ± 15 Volt Outputs Available**
- **Indefinite Short Circuit and Overload Protection**
- **12.9W/in^3 Power Density**
- **15 Watts Output Power**
- **Fast Loop Response For Superior Transient Characteristics**
- **Operating Temperature Range From -55°C to +125°C Available**
- **Popular Industry Standard Pin-Out**
- **Resistance Seam Welded Case For Superior Long Term Hermeticity**
- **Efficiencies Up to 82%**
- **Shutdown From External Signal**
- **Military Screening**
- **314,000 Hour MTBF at 85°C, AUC**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	-0.5V to 50V
Soldering Temperature	300°C for 10 seconds
Case Temperature	Operating-55°C to +125°C Storage -65°C to +135°C

TABLE I. Electrical Performance Characteristics

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{IN} = 28 V dc ±5%, C_L = 0 unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output voltage	V_{OUT}	I_{OUT} = 0	1	All	±11.88	±12.12	V
			2,3		±11.76	±12.24	
Output current 9/ 11/	I_{OUT}	V_{IN} = 17, 28, and 40 V dc	1,2,3	All	0.0	±625	mA
Output ripple voltage 8/ 9/	V_{RIP}	V_{IN} = 17, 28, and 40 V dc B.W. = dc to 2 mHz	1,2,3	All		60	mV p-p
Output power 4/ 9/ 11/	P_{OUT}	V_{IN} = 17, 28, and 40 V dc	1,2,3	All	15		W
Line regulation 9/ 10/	VR_{LINE}	V_{IN} = 17, 28, and 40 V dc I_{OUT} = 0, ±313, and ±625 mA	1	All		30	mV
			2,3			60	
Load regulation 9/	VR_{LOAD}	V_{IN} = 17, 28, and 40 V dc I_{OUT} = 0, ±313, and ±625 mA	1,2,3	All		120	mV
Input current	I_{IN}	I_{OUT} = 0, inhibit (pin 2) tied to input return (pin 10)	1,2,3	All		18	mA
		I_{OUT} = 0, inhibit (pin 2) = open				40	
Input ripple current 8/	I_{RIP}	I_{OUT} = ±625 mA B.W. = dc to 2 MHz	1,2,3	All		50	mA p-p
Efficiency	E_{FF}	I_{OUT} = ±625 mA, T_C = +25°C	1	All	80		%
Isolation	ISO	Input to output or any pin to case (except pin 8) at 500 V dc, T_C = +25°C	1	All	100		MΩ
Capacitive load 6/ 12/	C_L	No effect on dc performance, T_C = +25°C	4	All		200	µF
Power dissipation load fault	P_D	Overload, T_C = +25°C 3/	1	All		6	W
		Short circuit, T_C = +25°C				6	

See footnotes at end of table

TABLE I. Electrical Performance Characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{IN} = 28 V dc ±5%, C_L = 0 unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
Switching frequency [9]	F_S	I_{OUT} = ±625 mA	4,5,6	01	225	275	KHz
				02	225	245	
				03	250	275	
Output response to step transient load changes [7]	VO_{TLOAD}	50 percent load to/from 100 percent load	4	All	-300	+300	mV pk
			5,6		-450	+450	
		No load to/from 50 percent load	4	All	-500	+500	
			5,6		-750	+750	
Recovery time step transient load changes [1/ 7]	TT_{LOAD}	50 percent load to/from 100 percent load	4	All		70	µs
			5,6			100	
		No load to 50 percent load	4,5,6	All		1500	
		50 percent load to no load	4,5,6	All		5	ms
Output response to transient step line changes [5/ 12]	VO_{TLINE}	Input step 17 TO 40 V dc	4,5,6	All		1200	mV pk
		Input step 40 TO 17 V dc	4,5,6	All		-1500	
Recovery time transient step line changes [1/ 5/ 12]	TT_{LINE}	Input step 17 TO 40 V dc	4,5,6	All		4	ms
		Input step 40 TO 17 V dc	4,5,6	All		4	
Turn on overshoot [9]	$VTon_{OS}$	I_{OUT} = 0 and ±625 mA	4,5,6	All		600	mV pk
Turn on delay [2/ 9]	Ton_D	I_{OUT} = 0 and ±625 mA	4,5,6	All		10	ms
Load fault recovery [12]	Tr_{LF}		4,5,6	All		10	ms

Notes:

1/ Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ±1 percent of V_{OUT} at 50 percent load.
2/ Turn on delay time measurement is for either a step application of power at the input or the removal of a ground signal from the inhibit pin (pin 2) while power is applied to the input.
3/ An overload is that condition with a load in excess of the rated load but less than that necessary to trigger the short circuit protection and is the condition of maximum power dissipation.
4/ Total power at both outputs. For operation at 16 V dc input, derate output power by 33 percent.
5/ Input step transition time between 2 and 10 microseconds.
6/ Capacitive load may be any value from 0 to the maximum limit without compromising dc performance. A capacitive load in excess of the maximum limit will not disturb loop stability but may interfere with the operation of the load fault detection circuitry, appearing as a short circuit during turn on.
7/ Load step transition time between 2 and 10 microseconds.
8/ Bandwidth guaranteed by design. Tested for 20 KHz to 2 MHz.
9/ Tested at each output.
10/ When operating with unbalanced loads, at least 25 percent of the load must be on the positive output to maintain regulation.
11/ Parameter guaranteed by line and load regulation tests.
12/ Parameter shall be tested as part of design characterization and after design or process changes. Thereafter parameters shall be guaranteed to the limits specified in Table I.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	-0.5V to 50V
Soldering Temperature	300°C for 10 seconds
Case Temperature	Operating-55°C to +125°C Storage -65°C to +135°C

TABLE II. Electrical Performance Characteristics

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{IN} = 28 V dc ±5%, C_L = 0 unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output voltage	V_{OUT}	I_{OUT} = 0	1	All	±14.85	±15.15	V
			2,3		±14.70	±15.30	
Output current 9/ 11/	I_{OUT}	V_{IN} = 17, 28, and 40 V dc	1,2,3	All	0.0	±500	mA
Output ripple 8/ voltage 9/	V_{RIP}	V_{IN} = 17, 28, and 40 V dc B.W. = dc to 2 mHz	1,2,3	All		60	mV p-p
Output power 4/ 9/ 11/	P_{OUT}	V_{IN} = 17, 28, and 40 V dc	1,2,3	All	15		W
Line 9/ regulation 10/	VR_{LINE}	V_{IN} = 17, 28, and 40 V dc I_{OUT} = 0, ±250, and ±500 mA	1	All		35	mV
			2,3			75	
Load regulation 9/	VR_{LOAD}	V_{IN} = 17, 28, and 40 V dc I_{OUT} = 0, ±250, and ±500 mA	1,2,3	All		150	mV
Input current	I_{IN}	I_{OUT} = 0, inhibit (pin 2) tied to input return (pin 10)	1,2,3	All		18	ma
		I_{OUT} = 0, inhibit (pin 2) = open				40	
Input ripple 8/ current	I_{RIP}	I_{OUT} = ±500 mA B.W. = dc to 2 MHz	1,2,3	All		50	mA p-p
Efficiency	E_{FF}	I_{OUT} = ±500 mA, T_C = +25°C	1	All	80		%
Isolation	ISO	Input to output or any pin to case (except pin 8) at 500 V dc, T_C = +25°C	1	All	100		MΩ
Capacitive load 6/ 12/	C_L	No effect on dc performance, T_C = +25°C	4	All		200	µF
Power dissipation load fault	P_D	Overload, T_C = +25°C 3/	1	All		6	W

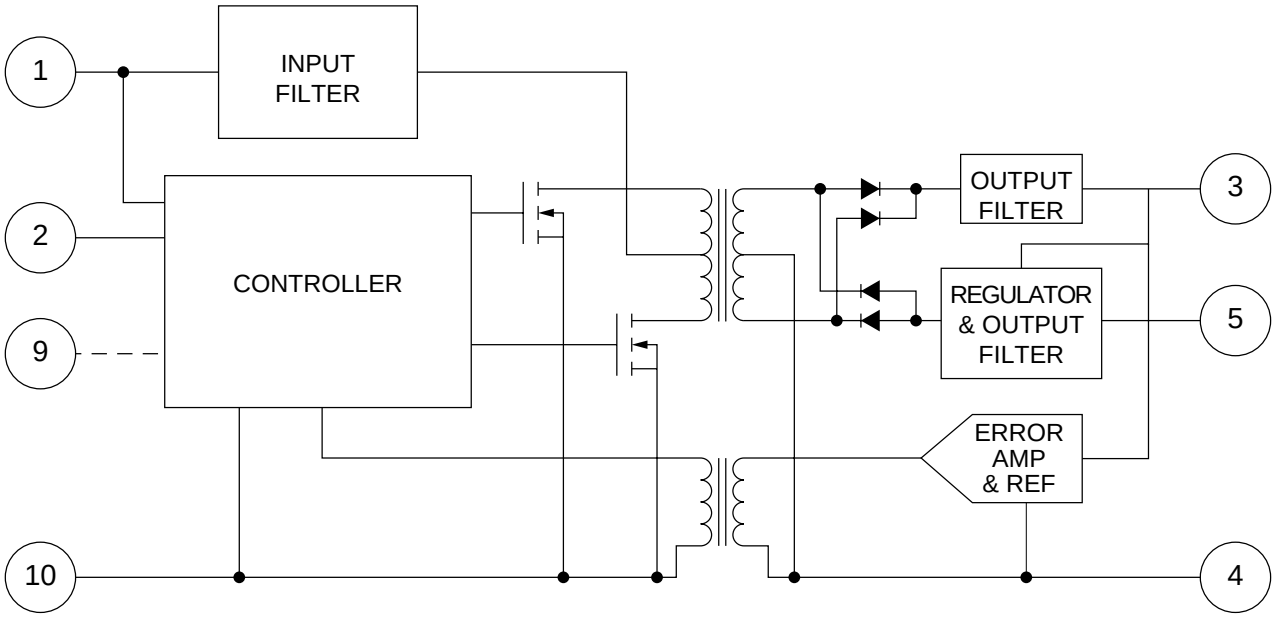
TABLE II. Electrical Performance Characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{IN} = 28 V dc ±5%, C_L = 0 unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
Switching frequency 9/	F_S	I_{OUT} = ±500 mA	4,5,6	01	225	275	KHz
				02	225	245	
				03	250	275	
Output response to step transient load changes 7/	VO_{TLOAD}	50 percent load to/from 100 percent load	4	All	-300	+300	mV pk
			5,6		-450	+450	
		No load to/from 50 percent load	4	All	-500	+500	
			5,6		-750	+750	
Recovery time step transient load changes transient load changes 1/ 7/	TT_{LOAD}	50 percent load to/from 100 percent load	4	All		70	µs
			5,6			100	
		No load to 50 percent load	4,5,6	All		1500	
		50 percent load to no load	4,5,6	All		5	ms
Output response to transient step line changes 5/ 12/	VO_{TLINE}	Input step 17 to 40 V dc	4,5,6	All		1500	mV pk
		Input step 40 to 17 V dc	4,5,6	All		-1500	
Recovery time transient step line changes 1/ 5/ 12/	TT_{LINE}	Input step 17 to 40 V dc	4,5,6	All		4	ms
		Input step 40 to 17 V dc	4,5,6	All		4	
Turn on overshoot 9/	$VTon_{OS}$	I_{OUT} = 0 and ±500 mA	4,5,6	All		600	mV pk
Turn on delay 2/ 9/	Ton_D	I_{OUT} = 0 and ±500 mA	4,5,6	All		10	ms
Load fault recovery 12/	Tr_{LF}		4,5,6	All		10	ms

Notes:

1/ Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ±1 percent of V_{OUT} at 50 percent load.
2/ Turn on delay time measurement is for either a step application of power at the input or the removal of a ground signal from the inhibit pin (pin 2) while power is applied to the input.
3/ An overload is that condition with a load in excess of the rated load but less than that necessary to trigger the short circuit protection and is the condition of maximum power dissipation.
4/ Total power at both outputs. For operation at 16 V dc input, derate output power by 33 percent.
5/ Input step transition time between 2 and 10 microseconds.
6/ Capacitive load may be any value from 0 to the maximum limit without compromising dc performance. A capacitive load in excess of the maximum limit will not disturb loop stability but may interfere with the operation of the load fault detection circuitry, appearing as a short circuit during turn on.
7/ Load step transition time between 2 and 10 microseconds.
8/ Bandwidth guaranteed by design. Tested for 20 KHz to 2 MHz.
9/ Tested at each output.
10/ When operating with unbalanced loads, at least 25 percent of the load must be on the positive output to maintain regulation.
11/ Parameter guaranteed by line and load regulation tests.
12/ Parameter shall be tested as part of design characterization and after design or process changes. Thereafter parameters shall be guaranteed to the limits specified in Table II.

BLOCK DIAGRAM (Single Output)



APPLICATION INFORMATION

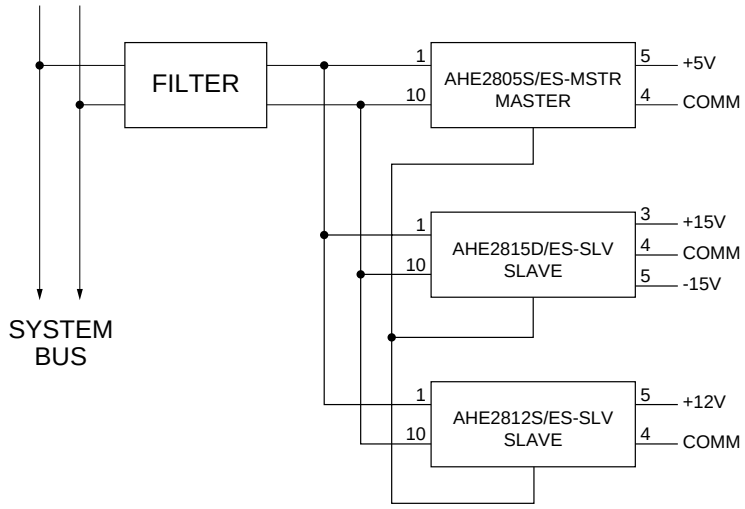
Inhibit Function
Connecting the inhibit input (Pin 2) to input common (Pin 10) will cause the converter to shut down. It is recommended that the inhibit pin be driven by an open collector device capable of sinking at least 400µA of current. The open circuit voltage of the inhibit input is 11.5 +1 V_{DC}.

EMI Filter
An optional EMI filter (AFC461) will reduce the input ripple current to levels below the limits imposed by MIL-STD-461 CEO3.

Device Synchronization
Whenever multiple DC/DC converters are utilized in a single system, significant low frequency noise may be generated due to slight difference in the switching frequencies of the converters (beat frequency noise). Because of the low frequency nature of this noise (typically less than 10 KHz), it is difficult to filter out and may interfere with proper operation of sensitive systems (communications, radar or telemetry). Lambda Advanced Analog offers an option which provides synchronization of multiple AHE/ATW converters, thus eliminating this type of noise.

To take advantage of this capability, the system designer must assign one of the converters as the master. Then, by definition, the remaining converters become slaves and will operate at the masters' switching frequency. The user should be aware that the synchronozation system is fail-safe; that is, the slaves will continue operating should the master frequency be interrupted for any reason. The layout must be such that the synchronozation output (Pin 9) of the master device is connected to the synchronozation input (Pin 9) of each slave device. It is advisable to keep this run short to minimize the possibilty of radiating the 250KHz switching frequency.

The appropriate parts must be ordered to utilize this feature. After selecting the converters required for the system, an ‘MSTR’ suffix is added for the master converter part number and an ‘SLV’ suffix is added for slave part number.



Typical Synchronization Connection Diagram

PIN DESIGNATION

AHE2812D
AHE2815D

Pin 1	Positive input	Pin 10	Input common
Pin 2	Inhibit input	Pin 9	N/C or sync.
Pin 3	Positive output	Pin 8	Case ground
Pin 4	Output common	Pin 7	N/C
Pin 5	Negative output	Pin 6	N/C

PART NUMBER

AHF 28 xx D x / x - xxx

Model
Input Voltage

Output Voltage
12–12 VDC
15–15 VDC

Dual Output

Package Option
F—Flange
Omit for standard

Synchronization Option
MSTR—Master
SLV—Slave

Temperature Range
Omit for -55°C to +85°C
ES— -55°C to +105°C
HB— -55°C to +125°C

HB Screening Process

Per MIL-PRF-38534

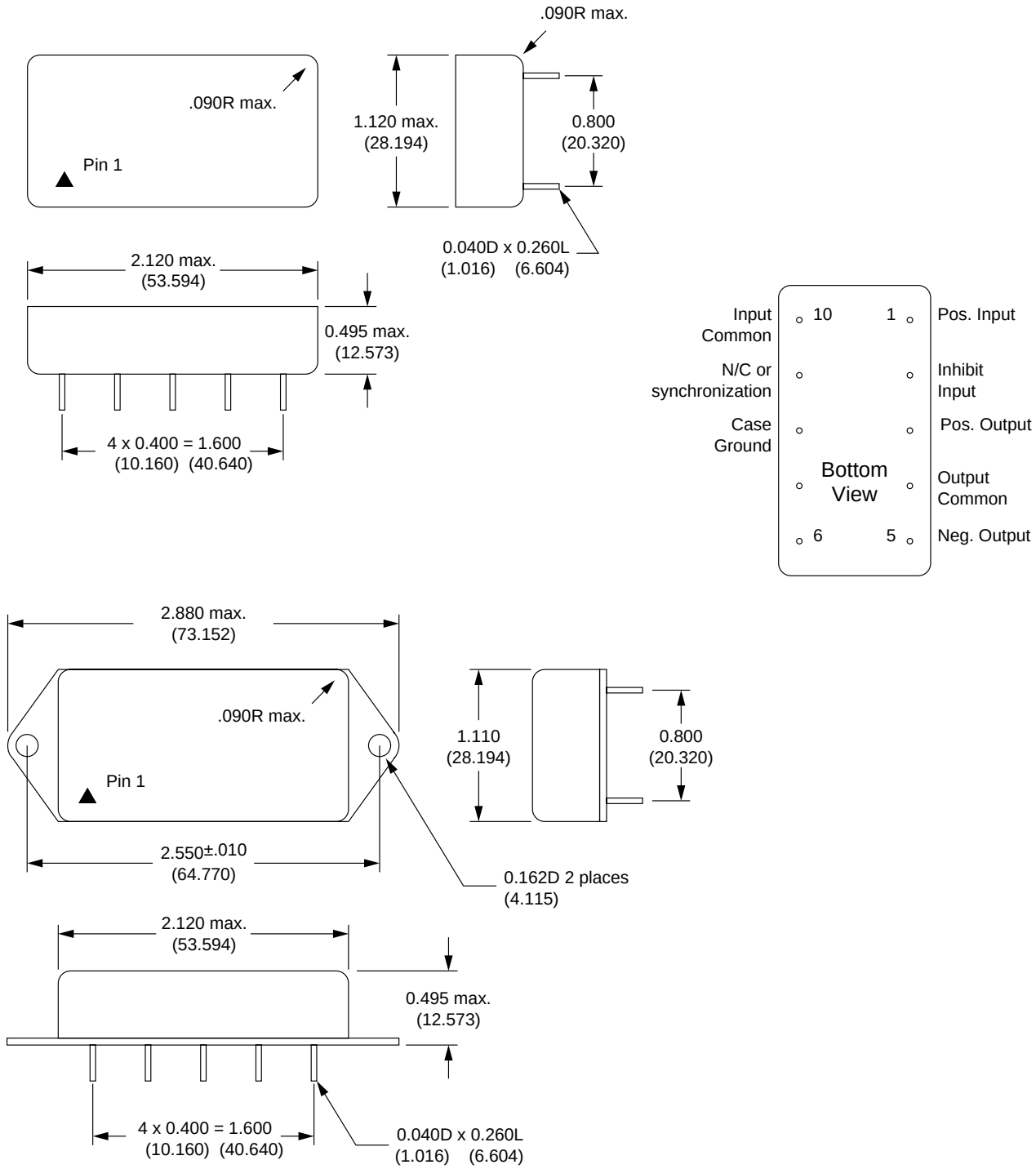
Test Inspection	Method	Conditlon
Pre-Seal Internal Visual	2017	
Stabilization Bake	1008	C
Temperature Cycling	1010	C
Constant Acceleration	2001	A, Y1 direction
Burn-in	1015	T_C = +125°C
Final Electrical Test		T_C = -55,+25,+125°C
Gross Leak	1014	C
Fine Leak	1014	A
External Visual	2009	

ES Screening Process

Same as HB screening except as follows:

Test Inspection	Method
Constant Acceleration	2001, 500g's
Burn-in	1015, 96hrs.
Final Electrical	25°C only

MECHANICAL OUTLINE



Weight

Standard—55 grams max.

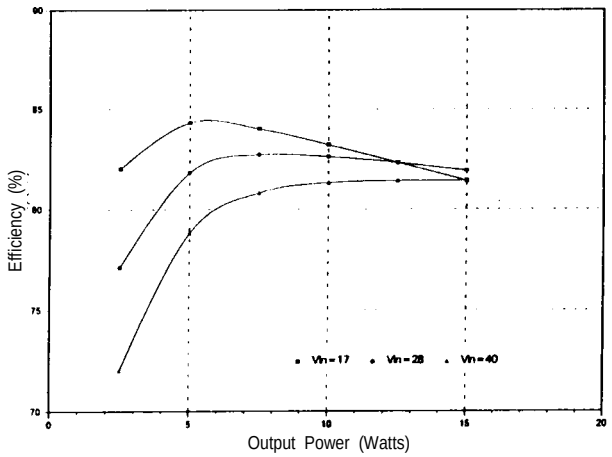
Flange—58 grams max.

STANDARDIZED MILITARY DRAWING
CROSS REFERENCE

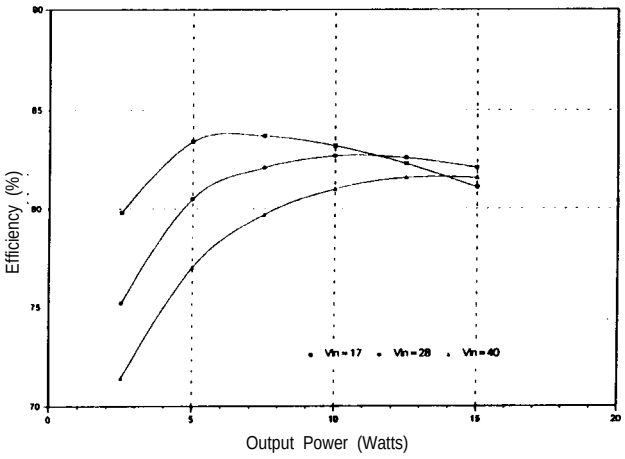
Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN
5962-9157501HXX	52467	AHE2815D/CH
5962-9157501HZX	52467	AHE2815DF/CH
5962-9157502HXX	52467	AHE2815D/CH-SLV
5962-9157502HZX	52467	AHE2815DF/CH-SLV
5962-9157503HXX	52467	AHE2815D/CH-MSTR
5962-9157503HZX	52467	AHE2815DF/CH-MSTR

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN
5962-9204001HXX	52467	AHE2812D/CH
5962-9204001HZX	52467	AHE2812DF/CH
5962-9204002HXX	52467	AHE2812D/CH-SLV
5962-9204002HZX	52467	AHE2812DF/CH-SLV
5962-9204003HXX	52467	AHE2812D/CH-MSTR
5962-9204003HZX	52467	AHE2812DF/CH-MSTR

AHE2815D EFFICIENCY



AHE2812D EFFICIENCY



 The information in this data sheet has been carefully checked and is believed to be accurate, however, no responsibility is assumed for possible errors. The specifications are subject to change without notice. 9849

LAMBDA ADVANCED ANALOG INC.

MIL-PRF-38534 Certified
ISO9001 Rgstrd

2270 Martin Avenue
Santa Clara CA 95050-2781
(408) 988-4930 FAX (408) 988-2702