LAMBDA ADVANCED ANALOG INC.

PRELIMINARY

AFL2803.3S Series

Single Output, Hybrid - High Reliability
DC/DC Converter

DESCRIPTION

The AFL Series of DC/DC converters feature high power density with no derating over the full military temperature range. This series is offered as part of a complete family of converters providing single and dual output voltages and operating from nominal +28, +50, +120 or +270 volt inputs with output power ranging from 80 to 120 watts. For applications requiring higher output power, individual converters can be operated in parallel. The internal current sharing circuits assure accurate current distribution among the paralleled converters. This series incorporates Lambda Advanced Analog's proprietary magnetic pulse feedback technology providing optimum dynamic line and load regulation response. This feedback system samples the output voltage at the pulse width modulator fixed clock frequency, nominally 550 KHz. Multiple converters can be synchronized to a system clock in the 500 KHz to 700 KHz range or to the synchronization output of one converter. Undervoltage lockout, primary and secondary referenced inhibit, soft-start and load fault protection are provided on all models.

These converters are hermetically packaged in two enclosure variations, utilizing copper core pins to minimize resistive DC losses. Three lead styles are available, each fabricated with Lambda Advanced Analog's rugged ceramic lead-to-package seal assuring long term hermeticity in the most harsh environments.

Manufactured in a facility fully qualified to MIL-PRF-38534, these converters are available in four screening grades to satisfy a wide range of requirements. The CH grade is fully compliant to the requirements of MIL-PRF-38534 for class H. The HB grade processed and screened to the class H requirement, may not necessarily meet all of the other MIL-PRF-38534 requirements, e.g., element evaluation and Periodic Inspections (P.I.) not required. Both grades are tested to meet the complete group "A" test specification over the full military temperature range without output power deration. Two grades with more limited screening are also available for use in less demanding applications. Variations in electrical, mechanical and screening can be accommodated. Contact Lambda Advanced Analog for special requirements.

FEATURES

- **16 To 40 Volt Input Range**
- **3.3 Volt Output**
- **High Power Density - 50 W / in^3**
- **66 Watt Output Power**
- **Parallel Operation with Stress and Current Sharing**
- **Low Profile (0.380") Seam Welded Package**
- **Ceramic Feedthru Copper Core Pins**
- **High Efficiency - 72%**
- **Full Military Temperature Range**
- **Continuous Short Circuit and Overload Protection**
- **Remote Sensing Terminals**
- **Primary and Secondary Referenced Inhibit Functions**
- **Line Rejection > 40 dB - DC to 50KHz**
- **External Synchronization Port**
- **Fault Tolerant Design**
- **Dual Output Versions Available**
- **Standard Military Drawings Available**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	-0.5V to 180V
Soldering Temperature	300°C for 10 seconds
Case Temperature	Operating-55°C to +125°C Storage -65°C to +135°C

TABLE I. Electrical Performance Characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{IN} = 28 V dc ±5%, C_L = 0 unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
Output voltage	V_{OUT}	I_{OUT} = 0	1	01	3.27	3.33	V
			2,3		3.23	3.37	
Output current 6/	I_{OUT}	V_{IN} = 16, 28, 40 v dc	1,2,3	01		20	A
Output ripple voltage	V_{RIP}	V_{IN} = 16, 28, 40 v dc B.W.= 20 Hz to 10 MHz	1,2,3	01		30	MV p-p
Line regulation	VR_{LINE}	V_{IN} = 16, 28, 40 v dc I_{OUT} = 0, 10 A, and 20 A	1,2,3	01		± 20	mV
Load regulation	VR_{LOAD}	V_{IN} = 16, 28, 40 v dc I_{OUT} = 0, 10 A, and 20 A	1,2,3	01		± 35	mV
Input current	I_N	I_{OUT} = No load	1	01		80	mA
			2,3,			100	
		Inhibit 1, (pin 4) shorted to input return (pin 2)	1,2,3			5	
		Inhibit 2, (pin 12) shorted to output return (pin 8)	1,2,3			50	
Input ripple current	I_{RIP}	I_{OUT} = 20 A B.W.= 20 Hz to 10 MHz	1,2,3	01		60	mA p-p
Efficiency	E_{FF}	I_{OUT} = 20 A	1,2,3	01	72		%
Isolation	ISO	Input to output or any pin to case (except pin 3) at 500 V dc, T_C = +25°C	1	01	100		MΩ
Maximum Capacitive load 1/	C_L	No effect on dc performance, T_C = +25°C	4	01	10,000		µF

See footnotes at end of table.

TABLE I. Electrical Performance Characteristics - Continued.

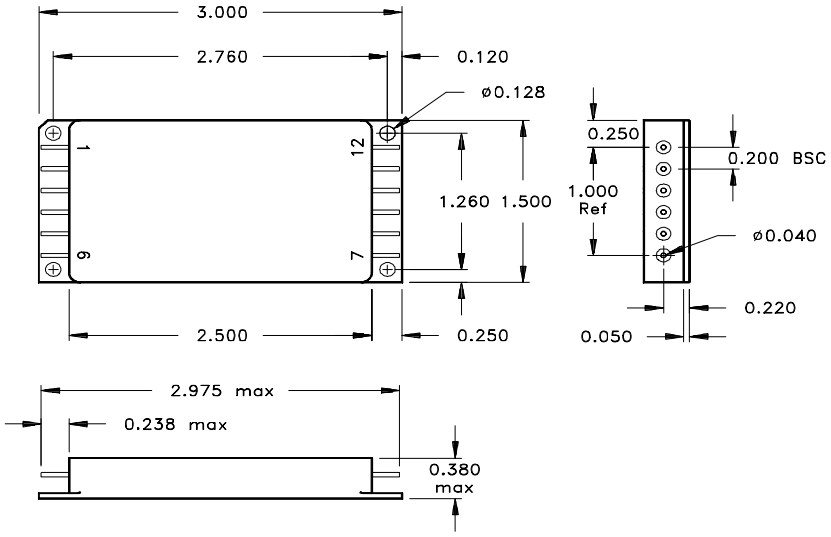
Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{IN} =28 V dc ±5%, C= 0 unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power dissipation load fault	P_D	Overload 6/	1,2,3	01		33	W
		Short circuit				33	
Current Limit Point 5/	I_{CL}	V_{OUT} = 90% V_{NOM} V_{IN} = 28 V	1	01	115	125	%
			2		105	115	
			3		125	140	
Switching frequency	F_S	I_{OUT} = 20 A	1,2,3	01	500	600	KHz
Sync frequency range	F_{sync}	I_{OUT} = 20 A	4,5,6	01	500	700	KHz
Output response to step transient load changes 2/ 8/	VO_{TLOAD}	50% to/from 100%	4,5,6	01	-450	+450	mV pk
		10% to/from 50%			-450	+450	
Recovery time, step transient load changes 2/ 8/	TT_{LOAD}	50% to/from 100%	4,5,6	01		200	µs
		10% to/from 50%				400	
Output response to transient step line changes 1/ 2/ 3/	VO_{TLINE}	Input step 16 V to/from 40 V dc, I_{OUT} = 20 A	4,5,6	01	-500	500	mV pk
Recovery time transient step line changes 1/ 2/ 3/	TT_{LINE}	Input step 16 V to/from 40 V dc, I_{OUT} = 20 A	4,5,6	01		500	µs
Turn on overshoot 4/	$VTon_{OS}$	I_{OUT} = 0 and 20 A	4,5,6	01		250	mV pk
Turn on delay 4/	Ton_D	I_{OUT} = 0 and 20 A	4,5,6	01		10	ms
Load fault recovery	Tr_{LF}		4,5,6	01		10	ms

Notes:

1/ Parameters not tested but are guaranteed to the limits specified in the table.
2/ Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ± 1 percent of V_{OUT} at 50 percent load.
3/ Line transient transition time ≥10 microseconds.
4/ Turn on delay is measured with an input voltage rise time of between 100 and 500 volts per millisecond.
5/ Current limit point is that condition of excess load causing output voltage to drop to 90% of nominal.
6/ Parameter verified as part of another test.
7/ All electrical tests are performed with remote sense leads connected to the output lead at the load.
8/ Input step transition time ≥100 microseconds.
9/ Enable inputs internally pulled high. Nominal open circuit voltage = $4.0V_{DC}$.

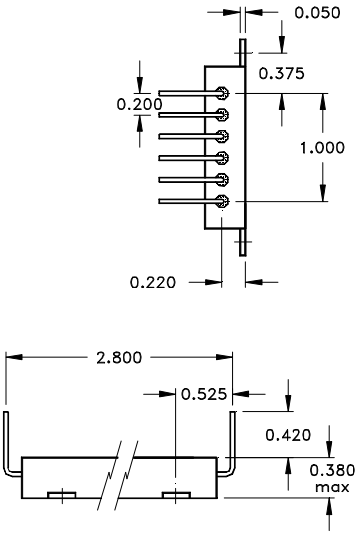
AFL2803.3S Case Outlines

Case X

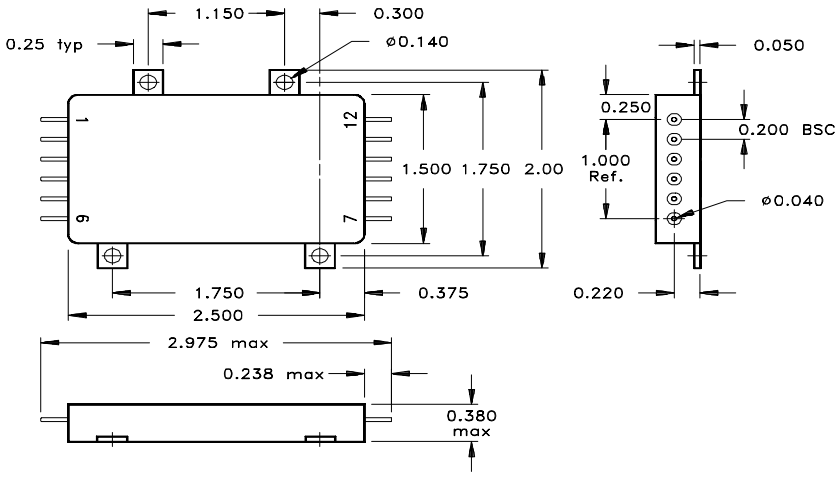


Case W

Pin Variation of Case Y



Case Y



Case Z

Pin Variation of Case Y

Tolerances, unless otherwise specified: .XX = ±0.010
.XXX = ±0.005

AFL2803.3S Pin Designation

Pin No.	Designation
1	Positive Input
2	Input Return
3	Case
4	Enable 1
5	Sync Output
6	Sync Input
7	Positive Output
8	Output Return
9	Negative Output
10	Output Voltage Trim
11	Share
12	Enable 2

Available Screening Levels and Process Variations for AFL 2803.3S Series.

Requirement	MIL-STD-883 Method	No Suffix	ES Suffix	HB Suffix	CH Suffix
Temperature Range		-20°C to +85°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C
Element Evaluation					MIL-PRF-38534
Internal Visual	2017	*	Yes	Yes	Yes
Temperature Cycle	1010		Cond B	Cond C	Cond C
Constant Acceleration	2001		500g	Cond A	Cond A
Burn-in	1015		96hrs @ 125°C	160hrs @ 125°C	160hrs @ 125°C
Final Electrical (Group A)	MIL-PRF-38534 & Specification	25°C	25°C	-55, +25, +125°C	-55, +25, +125°C
Seal, Fine & Gross	1014	Cond A	Cond A, C	Cond A, C	Cond A, C
External Visual	2009	*	Yes	Yes	Yes

* per Commercial Standards

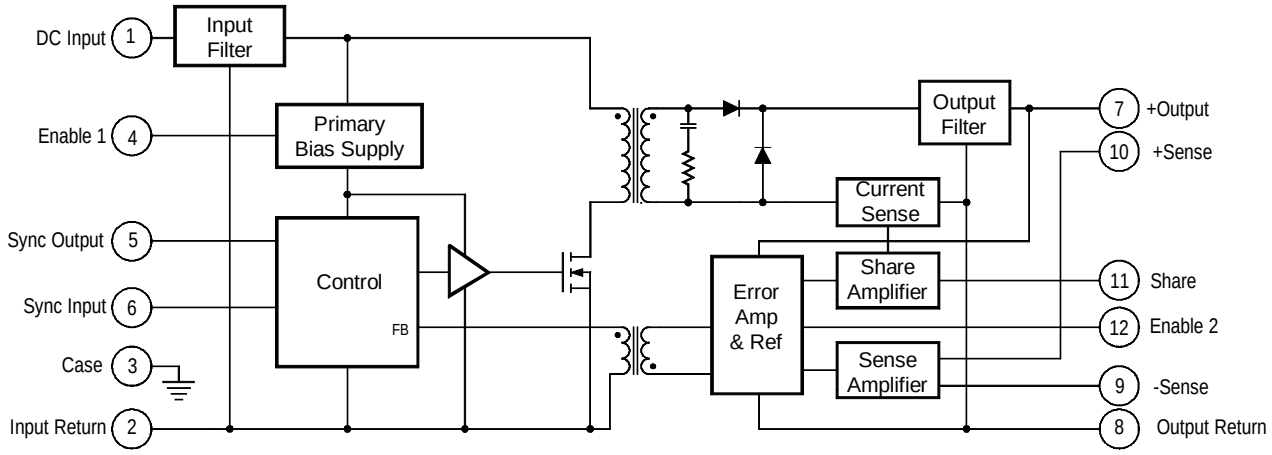
Part Numbering

AFL 28 03.3 S X / CH

- Model
- Input Voltage: 28 = 28V, 50 = 50V, 120 = 120V, 270 = 270V
- Output Voltage: 03.3 = 3.3V, 05 = 5V, 08 = 8V, 09 = 9V, 12V = 12V, 15 = 15V, 28 =28V
- Outputs: S = Single, D = Dual
- Case Style: W, X, Y, Z
- Screening: –, ES, HB, CH

AFL2800S Circuit Description

Figure I. AFL Single Output Block Diagram



Circuit Operation and Application Information

The AFL series of converters employ a forward switched mode converter topology. (refer to Figure I.) Operation of the device is initiated when a DC voltage whose magnitude is within the specified input limits is applied between pins 1 and 2. If pin 4 is enabled (at a logical 1 or open) the primary bias supply will begin generating a regulated housekeeping voltage bringing the circuitry on the primary side of the converter to life. A power MOSFET is used to chop the DC input voltage into a high frequency square wave, applying this chopped voltage to the power transformer at the nominal converter switching frequency. Maintaining a DC voltage within the specified operating range at the input assures continuous generation of the primary bias voltage.

The switched voltage impressed on the secondary output transformer winding is rectified and filtered to generate the converter DC output voltage. An error amplifier on the secondary side compares the output voltage to a precision reference and generates an error signal proportional to the difference. This error signal is magnetically coupled through the feedback transformer into the controller section of the converter varying the pulse width of the square wave signal driving the MOSFET, narrowing the width if the output voltage is too high and widening it if it is too low, thereby regulating the output voltage.

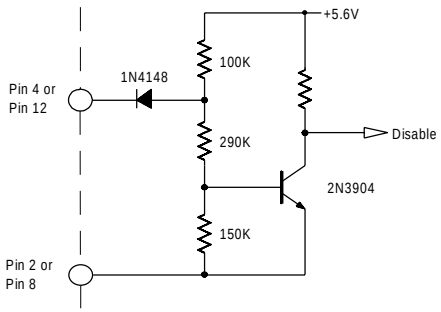
Remote Sensing

Connection of the + and - sense leads at a remotely located load permits compensation for excessive resistance between the converter output and the load when their physical separation could cause undesirable voltage drop. This connection allows regulation to the placard voltage at the point of application. When the remote sensing feature is not used, the sense leads should be connected to their respective output terminals at the converter. Figure III. illustrates a typical remotely sensed application.

Inhibiting Converter Output

As an alternative to application and removal of the DC voltage to the input, the user can control the converter output by providing TTL compatible, positive logic signals to either of two enable pins (pin 4 or 12). The distinction between these two signal ports is that enable 1 (pin 4) is referenced to the input return (pin 2) while enable 2 (pin 12) is referenced to the output return (pin 8). Thus, the user has access to an inhibit function on either side of the isolation barrier. Each port is internally pulled “high” so that when not used, an open connection on both enable pins permits normal converter operation. When their use is desired, a logical “low” on either port will shut the converter down.

Figure II. Enable Input Equivalent Circuit



Internally, these ports differ slightly in their function. In use, a low on Enable 1 completely shuts down all circuits in the converter while a low on Enable 2 shuts down the secondary side while altering the controller duty cycle to near zero. Externally, the use of either port is transparent save for minor differences in standby current. (See specification table).

Synchronization of Multiple Converters

When operating multiple converters, system requirements often dictate operation of the converters at a common frequency. To accommodate this requirement, the AFL series converters provide both a synchronization input and a synchronization output.

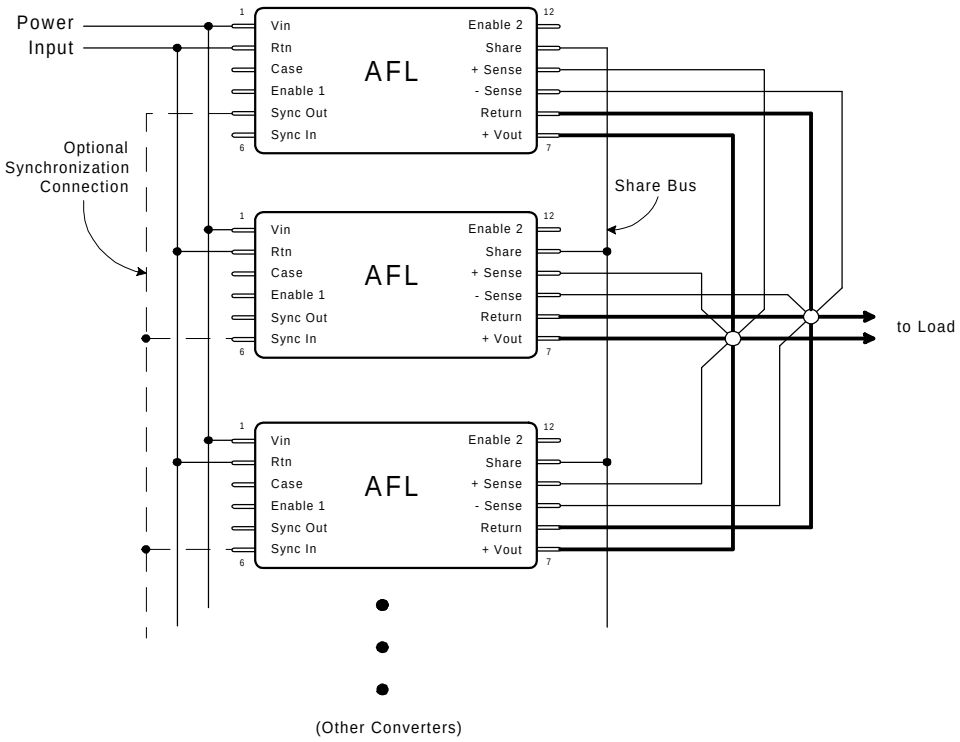
The sync input port permits synchronization of an AFL converter to any compatible external frequency source operating between 500 and 700 KHz. This input signal should be referenced to the input return and have a 10% to 90% duty cycle. Compatibility requires transition times less than 100 ns, maximum low level of +0.8 volts and a minimum high level of +2.0 volts. The sync output of another converter which has been designated as the master oscillator provides a convenient frequency source for this mode of operation. When external synchronization is not required, the sync in pin should be left open (unconnected) thereby permitting the converter to operate at its' own internally set frequency.

The sync output signal is a continuous pulse train set at 550 ±50 KHz, with a duty cycle of 15 ±5%. This signal is referenced to the input return and has been tailored to be compatible with the AFL sync input port. Transition times are less than 100 ns and the low level output impedance is less than 50 ohms. This signal is active when the DC input voltage is within the specified operating range and the converter is not inhibited. This output has adequate drive reserve to synchronize at least five additional converters. A typical connection is illustrated in Figure III.

Parallel Operation — Current and Stress Sharing

Figure III. illustrates the preferred connection scheme for operation of a set of AFL converters with outputs operating in parallel. Use of this connection permits equal sharing among the members of a set where total load current exceeds the capacity of an individual AFL. An important feature of the AFL series operating in the parallel mode is that in addition to sharing the current, the stress induced by temperature will also be shared. Thus if one member of a paralleled set is operating at a higher case temperature, the current it provides to the load will be reduced as compensation for the tempera-

Figure III. Preferred Connection for Parallel Operation



ture induced stress on that device.

When operating in the shared mode, it is important that symmetry of connection be maintained as an assurance of optimum load sharing performance. Thus, converter outputs should be connected to the load with equal lengths of wire of the same gauge and sense leads from each converter should be connected to a common physical point, preferably at the load along with the converter output and return leads. All converters in a paralleled set must have their share pins connected together. This arrangement is diagrammatically illustrated in Figure III. showing the outputs and sense pins connected at a star point which is located close as possible to the load.

As a consequence of the topology utilized in the current sharing circuit, the share pin may be used for other functions. In applications requiring only a single converter, the voltage appearing on the share pin may be used as a "current monitor". The share pin open circuit voltage is nominally +1.00v at no load and increases linearly with increasing output current to +2.20v at full load.

Thermal Considerations

Because of the incorporation of many innovative technological concepts, the AFL series of converters is capable of providing very high output power from a package of very small volume. These magnitudes of power density can only be obtained by combining high circuit efficiency with effective methods of heat removal from the die junctions. This requirement has been effectively addressed inside the device; but when operating at maximum loads, a significant amount of heat will be generated and this heat must be conducted away from the case. To maintain the case temperature at or below the specified maximum of 125°C, this heat must be transferred by conduction to an appropriate heat dissipater held in intimate contact with the converter base-plate.

Because effectiveness of this heat transfer is dependent on the intimacy of the baseplate-heatsink interface, it is strongly recommended that a high thermal conductivity heat transferring medium is inserted between the baseplate and heatsink. The material most frequently utilized at the factory during all testing and burn-in processes is sold under the trade name of Sil-PadR 400[1] . This particular product is an insulator but electrically conductive versions are also available. Use of these materials assures maximum surface contact with the heat dissipater thereby compensating for any minor surface variations. While other available types of heat conductive materials and thermal compounds provide similar effectiveness, these alternatives are often less convenient and are frequently messy to use.

A conservative aid to estimating the total heat sink surface area ($A_{HEAT\ SINK}$) required to set the maximum case temperature rise (ΔT) above ambient temperature is given by the following expression:

$$A_{\text{HEAT SINK}} \approx \left\{\frac{\Delta T}{80P^{0.85}}\right\}^{-143} - 3.0$$

where

$\Delta T =$ Case temperature rise above ambient

$P =$ Device dissipation in Watts $= P_{OUT}\left\{\frac{1}{Eff} - 1\right\}$

As an example, it is desired to maintain the case temperature of an AFL2815S at ≤ +85°C while operating in an open area whose ambient temperature is held at a constant +25°C; then
ΔT = 85 - 25 = 60°C.

From the Specification Table, the worst case full load efficiency for this device is 83%; therefore the power dissipation at full load is given by

$$P = 120 \bullet \left\{\frac{1}{.83} - 1\right\} = 120 \bullet (0.205) = 24.6\text{W}$$

and the required heat sink area is

$$A_{\text{HEAT SINK}} = \left\{\frac{60}{80 \bullet 24.6^{0.85}}\right\}^{-143} - 3.0 = 71\ \text{in}^2$$

Thus, a total heat sink surface area (including fins, if any) of 71 in^2 in this example, would limit case rise to 60°C above ambient. A flat aluminum plate, 0.25" thick and of approximate dimension 4" by 9" (36 in^2 per side) would suffice for this application in a still air environment. Note that to meet the criteria in this example, both sides of the plate require unrestricted exposure to the ambient air.

Input Filter

The AFL2800S series converters incorporate a two stage LC input filter whose elements dominate the input load impedance characteristic at turn-on. The input circuit is as shown in Figure IV.

[1]Sil-Pad is a registered Trade Mark of Bergquist, Minneapolis, MN

Figure IV. Input Filter Circuit

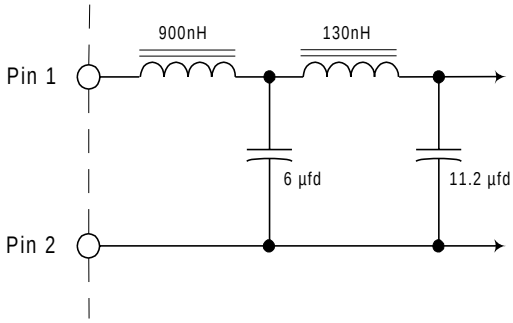
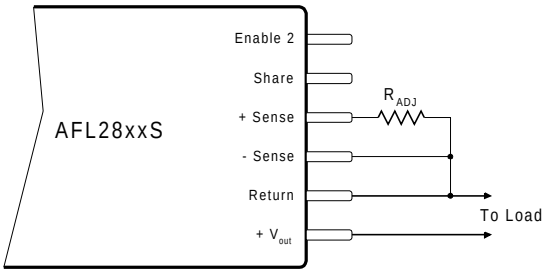


Figure V. Connection for Vout Adjustment.



Undervoltage Lockout

A minimum voltage is required at the input of the converter to initiate operation. This voltage is set to 14.0 ± 0.5 volts. To preclude the possibility of noise or other variations at the input falsely initiating and halting converter operation, a hysteresis of approximately 1.0 volts is incorporated in this circuit. Thus if the input voltage droops to 13.0 ± 0.5 volts, the converter will shut down and remain inoperative until the input voltage returns to »14.0 volts.

Output Voltage Adjust

In addition to permitting close voltage regulation of remotely located loads, it is possible to utilize the converter sense pins to incrementally increase the output voltage over a limited range. The adjustments made possible by this method are intended as a means to "trim" the output to a voltage setting for some particular application, but are not intended to create an adjustable output converter. These output voltage setting variations are obtained by connecting an appropriate resistor value between the +sense and -sense pins while connecting the -sense pin to the output return pin as shown in Figure V. below. The range of adjustment and corresponding range of resistance values can be determined by use of the following equation.

$$R_{adj} = 100 \bullet \left\{ \frac{V_{NOM}}{V_{OUT} - V_{NOM} - .025} \right\}$$

Where V_{NOM} = device nominal output voltage, and

V_{OUT} = desired output voltage

Finding a resistor value for a particular output voltage, is simply a matter of substituting the desired output voltage and the nominal device voltage into the equation and solving for the corresponding resistor value.

Attempts to adjust the output voltage to a value greater than 120% of nominal should be avoided because of the potential of exceeding internal component stress ratings and subsequent operation to failure. Under no circumstance should the external setting resistor be made less than 500W. By remaining within this specified range of values, completely safe operation fully within normal component derating limits is assured.

Examination of the equation relating output voltage and resistor value reveals a special benefit of the circuit topology utilized for remote sensing of output voltage in the AFL2800S series of converters. It is apparent that as the resistance increases, the output voltage approaches the nominal set value of the device. In fact the calculated limiting value of output voltage as the adjusting resistor becomes very large is » 25mV above nominal device voltage.

The consequence is that if the +sense connection is unintentionally broken, an AFL28xxS has a fail-safe output voltage of Vout + 25mV, where the 25mV is independent of the nominal output voltage. It can be further demonstrated that in the event of both the + and - sense connections being broken, the output will be limited to Vout + 440mV. This 440 mV is also essentially constant independent of the nominal output voltage.

General Application Information

The AFL2800 series of converters are capable of providing large transient currents to user loads on demand. Because the nominal input voltage range in this series is relatively low, the resulting input current demands will be correspondingly large. It is important therefore, that the line impedance be kept very low to prevent steady state and transient input currents from degrading the supply voltage between the voltage source and the converter input. In applications requiring high static currents and large

transients, it is recommended that the input leads be made of

adequate size to minimize resistive losses, and that a good quality capacitor of approximately 100µfd be connected directly across the input terminals to assure an adequately low impedance at the input terminals. Table I relates nominal resistance values and selected wire sizes.

Table I. Nominal Resistance Of Cu Wire

Wire Size, AWG	Resistance per ft
24 Ga	25.7 mΩ
22 Ga	16.2 mΩ
20 Ga	10.1 mΩ
18 Ga	6.4 mΩ
16 Ga	4.0 mΩ
14 Ga	2.5 mΩ
12 Ga	1.6 mΩ

As an example of the effects of parasitic resistance, consider an AFL2815S operating at full power of 120 W. From the specification sheet, this device has a minimum efficiency of 83% representing an input power of nearly 145 W. If we consider the case where line voltage is at its' minimum of 16 volts, the steady state input current necessary for this example will be slightly greater than 9 amperes. If this device were connected to a voltage source with 10 feet of 20 gauge wire, the round trip (input and return) would result in 0.2 Ω of resistance and 1.8 volts of drop from the source to the converter. To assure 16 volts at the input, a source closer to 18 volts would be required. In applications using the paralleling option, this drop will be multiplied by the number of paralleled devices. By choosing 14 or 16 gauge wire in this example the parasitic resistance and resulting voltage drop will be reduced to 25% or 31% of that with 20 gauge wire.

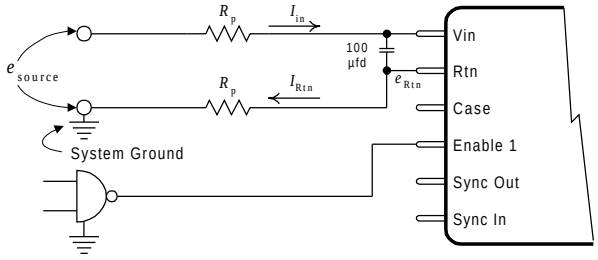
Another potential problem resulting from parasitically induced voltage drop on the input lines is with regard to operation of the enable 1 port. The minimum and maximum operating levels required to operate this port are specified with respect to the input common return line at the converter. If a logic signal is generated with respect to a 'common' that is distant from the converter, the effects of the voltage drop over the return line must be considered when establishing the worst case TTL switching levels. These drops will effectively impart a shift to the logic levels. In Figure VI, it can be seen that referred to system ground, the voltage on the input return pin is given by

$$e_{Rtn} = I_{Rtn} \bullet R_p$$

Therefore, the logic signal level generated in the system must be capable of a TTL logic high plus sufficient additional amplitude to overcome e_{Rtn}. When the converter is inhibited, I_{Rtn} diminishes to near zero and e_{Rtn} will then be at system ground.

Incorporation of a 100 µfd capacitor at the input terminals is recommended as compensation for the dynamic effects of the parasitic resistance of the input cable reacting with the complex impedance of the converter input, and to provide an energy reservoir for transient input current requirements.

Figure VI. Effects of Parasitic Resistance in Input Leads



NOTES

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