GSM Power Management System

Preliminary Technical Data — ADP3408

FEATURES
Handles all GSM Baseband Power Management
Six LDOs Optimized for Specific GSM Subsystems
Li-Ion and NiMH Battery Charge Function
Optimized for the AD20msp430 Baseband Chipset

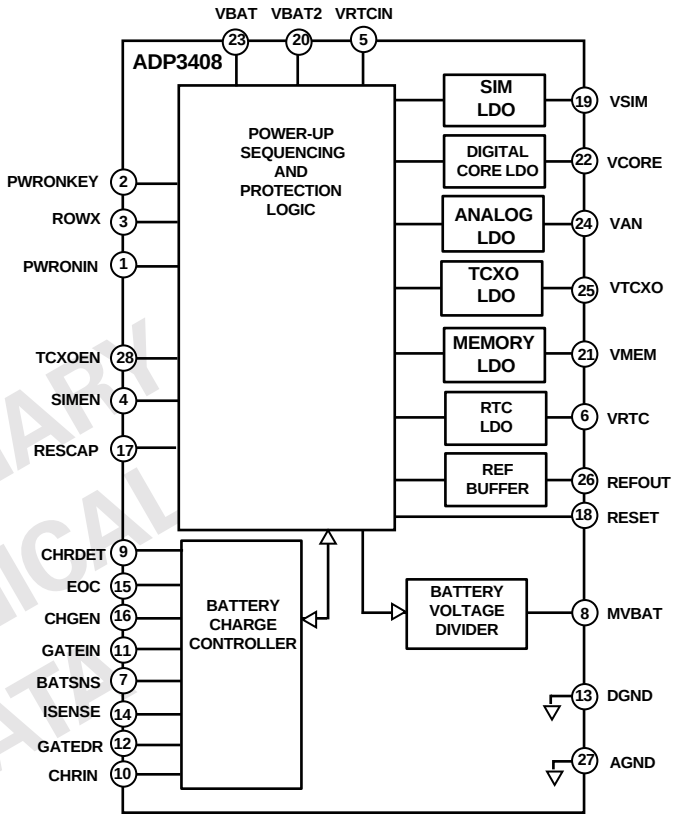
APPLICATIONS
GSM/DCS/PCS/CDMA Handsets

GENERAL DESCRIPTION

The ADP3408 is a multifunction power system chip optimized for GSM handsets, especially those based on the Analog Devices AD20msp430 system solution. It contains six LDOs, one to power each of the critical GSM sub-blocks. Sophisticated controls are available for power up during battery charging, keypad interface, and RTC alarm. The charge circuit maintains low current charging during the initial charge phase and provides an end of charge signal when a Li-Ion battery is being charged.

The ADP3408 is specified over the temperature range of –20°C to 85° C and is available in narrow body TSSOP-28 pin package.

FUNCTIONAL BLOCK DIAGRAM



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ADP3408–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS[1]

(–20°C ≤ T_A ≤ +85°C, VBAT = VBAT2 =3 V - 7.5 V, CVSIM=CVCORE=CVAN= CVMEM=2.2 µF, VTCXO=0.22 µF,CVRTC = 0.1µF, CVBAT=10 µF, min. loads applied on all outputs, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SHUTDOWN SUPPLY CURRENT	ICC					
VBAT ≤ 2.5 V (Deep Discharged Lockout Active)		VBAT=VBAT2 = 2.3 V		5	10	µA
2.5 V < VBAT ≤ 3.2 V (UVLO active)		VBAT=VBAT2 = 3.0 V		30	55	µA
VBAT >3.2 V		VBAT=VBAT2 = 4.5 V		45	80	µA
OPERATING GROUND CURRENT	IGND					
VSIM, VCORE, VMEM, VRTC On		Minimum Loads		200	240	µA
All LDOs On		Minimum Loads		230	280	µA
All LDOs On		Maximum Loads		2.0	4.0	% of max load current
UVLO ON THRESHOLD	VBAT			3.2	3.3	V
UVLO HYSTERESIS	VBAT			200		mV
DEEP DISCHARGED LOCKOUT ON THRESHOLD	VBAT			2.4	2.5	V
DEEP DISCHARGED LOCKOUT HYSTERESIS	VBAT			100		mV
INPUT HIGH VOLTAGE (PWRONIN, TCXOEN, SIMEN, CHGEN, GATEIN)	V_{IH}		2.0			V
INPUT LOW VOLTAGE (PWRONIN, TCXOEN, SIMEN, CHGEN, GATEIN)	V_{IL}				0.4	V
INPUT HIGH BIAS CURRENT (PWRONIN, TCXOEN, SIMEN, CHGEN, GATEIN)	I_{IH}				1.0	µA
INPUT LOW BIAS CURRENT (PWRONIN, TCXOEN, SIMEN, CHGEN, GATEIN)	I_{IL}		–1.0			µA
PWRONKEY INPUT HIGH VOLTAGE	V_{IH}		0.7×VBAT			V
PWRONKEY INPUT LOW VOLTAGE	V_{IL}				0.3×VBAT	V
PWRONKEY INPUT PULLUP RESISTANCE TO VBAT			75	110	145	kΩ
THERMAL SHUTDOWN THRESHOLD[2]				150		°C
THERMAL SHUTDOWN HYSTERESIS				25		°C
ROWX CHARACTERISTICS						
ROWX Output Low Voltage	V_{OL}	PWRONKEY = Low I_{OL} = 200 µA			0.4	V
ROWX Output High Leakage Current	I_{IH}	PWRONKEY = High V(ROWX) = 5 V			1	µA

NOTES

[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

[2]This feature is intended to protect against catastophic failure of the device. Maximum allowed operating junction temperature is 125°C. Operation beyond 125°C could cause permanent damage to the device.

Specifications subject to change without notice.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SIM CARD LDO (VSIM)						
Output Voltage	VSIM	Line, Load, Temp	2.80	2.86	2.92	V
Line Regulation	ΔVSIM			4		mV
Load Regulation	ΔVSIM	50 μA ≤ I_{LOAD} ≤ 20 mA		2		mV
Output Capacitor Required For Stability	C_O		2.2			μF
Dropout Voltage	V_{DO}	V_O = $V_{INITIAL}$ – 100 mV, I_{LOAD} = 20 mA			130	mV
DIGITAL CORE LDO (VCORE)						
Output Voltage						
ADP3408ARU-2.5	VCORE	Line, Load, Temp	2.40	2.45	2.50	V
ADP3408ARU-1.8	VCORE	Line, Load, Temp	1.764	1.80	1.836	V
Line Regulation	ΔVCORE			5		mV
Load Regulation	ΔVCORE	50 μA ≤ I_{LOAD} ≤ 100 mA		10		mV
Output Capacitor Required For Stability	C_O		2.2			μF
RTC LDO REAL TIME CLOCK LDO/ COIN CELL CHARGER (VRTC)						
Maximum Output Voltage						
ADP3408ARU-2.5	VRTC	I_{LOAD} ≤ 10 μA	2.40	2.45	2.50	V
ADP3408ARU-1.8	VRTC	I_{LOAD} ≤ 10 μA	1.90	2.00	2.10	V
Current Limit	I_{MAX}			175		μA
Off Reverse Input Current	I_L	2.0 V < VBAT < DDLO			1	μA
Output Capacitor Required For Stability	C_O		0.1			μF
ANALOG LDO (VAN)						
Output Voltage	VAN	Line, Load, Temp	2.40	2.45	2.50	V
Line Regulation	ΔVAN			5		mV
Load Regulation	ΔVAN	50 μA ≤ I_{LOAD} ≤ 130 mA		13		mV
Output Capacitor Required For Stability	C_O		2.2			μF
Ripple Rejection	ΔVBAT/ ΔVAN[3]	f = 217 Hz (t=4.6 ms) V_{BAT} = 3.6 V	65			dB
Output Noise Voltage	V_{NOISE}	f = 10 Hz to 100 kHz I_{LOAD} = 130 mA V_{BAT} = 3.6 V		80		μV_{rms}
TCXO LDO (VTCXO)						
Output Voltage	VTCXO	Line, Load, Temp	2.66	2.715	2.77	V
Line Regulation	ΔVTCXO			4		mV
Load Regulation	ΔVTCXO	50 μA ≤ I_{LOAD} ≤ 20 mA		2		mV
Output Capacitor Required For Stability	C_O		0.22			μF
Dropout Voltage	V_{DO}	V_O = $V_{INITIAL}$ – 100 mV I_{LOAD} = 20 mA			230	mV
Ripple Rejection	ΔVBAT/ ΔVTCXO	f = 217 Hz (t=4.6 ms) VBAT = 3.6 V	65			dB
Output Noise Voltage	V_{NOISE}	f = 10 Hz to 100 kHz I_{LOAD} = 20 mA, VBAT = 3.6 V		80		μV_{rms}

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Parameter	Symbol	Conditions	Min	Typ	Max	Units
MEMORY LDO (VMEM)						
Output Voltage	VMEM	Line, Load, Temp	2.710	2.765	2.820	V
Line Regulation	ΔVMEM			5		mV
Load Regulation	ΔVMEM	50 µA < I_{LOAD} < 60 mA		10		mV
Output Capacitor Required For Stability	C_O		2.2			µF
REFOUT						
Output Voltage	VREFOUT	Line, Load, Temp	1.192	1.210	1.228	V
Line Regulation	ΔVREFOUT	Min Load		2		mV
Load Regulation	ΔVREFOUT	0 µA < I_{LOAD} < 50 µA VBAT = 3.6 V		0.5		mV
Ripple Rejection	ΔVBAT/ ΔVREFOUT	f = 217 Hz (t=4.6 ms)	65	75		dB
Maximum Capacitive Load	C_O		100			pF
Output Noise Voltage	V_{NOISE}	f = 10 Hz to 100 kHz		40		µV rms
RESET GENERATOR (RESET)						
Output High Voltage	V_{OH}	I_{OH} = 500 µA	V_{MEM}–0.25			V
Output Low Voltage	V_{OL}	I_{OL} = –500µA			0.25	V
Output Current	I_{OL}/I_{OH}	V_{OL}= 0.25 V, V_{OH} = V_{MEM}–0.25V		1		mA
Delay Time per Unit Capacitance Applied to RESCAP Pin	T_D		1.0	1.5	3	ms/nF
BATTERY VOLTAGE DIVIDER						
Divider Ratio	BATSNS/ MVBAT	TCXOEN = High	2.94	3.00	3.06	
Divider Impedance at MVBAT	Z_O		67.5	90	112.5	kΩ
Divider Leakage Current		TCXOEN = Low			1	µA
Divider Resistance		TCXOEN = High	270	360	450	kΩ
BATTERY CHARGER						
Charger Output Voltage	BATSNS	4.35 V ≤ CHRIN ≤ 10 V CHGEN = Low	4.155	4.200	4.245	V
Load Regulation	ΔBATSNS	CHRIN = 5 V 0 ≤ CHRIN – ISENSE < Current Limit Threshold CHGEN = Low	–5		+5	mV
CHRDET on Threshold	CHRIN - VBAT	TBD	70	100	130	mV
CHRDET Hysteresis			30	40	50	mV
CHRDET Off Delay*		CHRIN < VBAT		3		ms/nF
CHRIN Supply Current		CHRIN = 5 V		0.6		mA

* Delay set by external capacitor on the RESCAP pin.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
BATTERY CHARGER						
Current Limit Threshold	CHRIN - ISENSE					
High Current Limit (100%: UVLO not active)		CHRIN = 5 V VBAT = 3.6 V CHGEN = Low	148	165	182	mV
Low Current Limit (10%: UVLO active)		VBAT = 2 V CHGEN = Low	10	20	30	mV
ISENSE Bias Current		CHRIN = 5 V		200		µA
End of Charge Signal Threshold	CHRIN - ISENSE	CHRIN = 5 V VBAT > 4.0 V CHGEN = Low	12	16	20	mV
GATEDR Transition Time	t_R, t_F	CHRIN = 5 V VBAT > 3.6 V CHGEN = High,C_L=2nF	1		10	µS
GATEDR High Voltage	V_{OH}	CHRIN = 5 V VBAT = 3.6 V CHGEN = High, GATEIN = High I_{OH} = –1 mA	4.5			V
GATEDR Low Voltage	V_{OL}	CHRIN = 5 V VBAT = 3.6 V CHGEN = High GATEIN = Low I_{OL} = 1 mA			0.5	V
Output High Voltage (EOC, CHRDET)	V_{OH}	I_{OH} = –250 µA	2.4			V
Output Low Voltage (EOC, CHRDET)	V_{OL}	I_{OL} = 250 µA			0.25	V
Battery Overvoltage Protection Threshold (GATEDR → High)	BATSNS	CHRIN = 7.5 V CHGEN = High GATEIN = Low	5.30	5.50	5.70	V
Battery Overvoltage Protection Hysteresis	BATSNS	CHRIN = 7.5 V CHGEN = High GATEIN = Low		200		mV

ABSOLUTE MAXIMUM RATINGS*

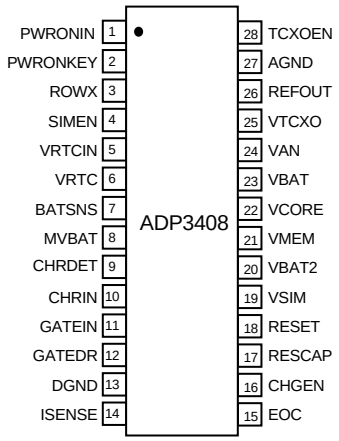
Voltage on any pin with respect to any GND Pin . . . . . –0.3 V to +10 V
Voltage on any pin may not exceed VBAT, with the following exceptions: CHRIN, GATEDR, ISENSE
Storage Temperature Range . . . . . –65°C to +150°C
Operating Ambient Temperature Range . . . . –20°C to +85°C
Maximum Junction Temperature . . . . . 125°C
θ_{JA}, Thermal Impedance (TSSOP-28)
4-Layer PCB . . . . . 68°C/W
1-Layer PCB . . . . . 98°C/W
Lead Temperature Range (Soldering, 60 sec.) . . . . . 300°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

ORDERING GUIDE

Model	Core LDO Output Voltage	Temperature Range	Pkg Option
ADP3408ARU-2.5	2.5 V	–20 °C to +85 °C	RU-28
ADP3408ARU-1.8	1.8 V	–20 °C to +85 °C	RU-28

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
1	PWRONIN	Power On/Off Signal from Microprocessor
2	PWRONKEY	Power On/Off Key
3	ROWX	Power Key Interface Output
4	SIMEN	SIM LDO Enable
5	VRTCIN	RTC LDO Input Voltage
6	VRTC	Real Time Clock Supply/ Coin Cell Battery Charger
7	BATSNS	Battery Voltage Sense Input
8	MVBAT	Divided Battery Voltage Output
9	CHRDET	Charge Detect Output
10	CHRIN	Charger Input Voltage
11	GATEIN	Microprocessor Gate Input Signal
12	GATEDR	Gate Drive Output
13	DGND	Digital Ground
14	ISENSE	Charge Current Sense Input
15	EOC	End of Charge Signal
16	CHGEN	Charger Enable for GATEIN, NiMH Pulse Charging
17	RESCAP	Reset Delay Time
18	RESET	Main Reset
19	VSIM	SIM LDO Output
20	VBAT2	Battery Input Voltage 2
21	VMEM	Memory LDO Output
22	VCORE	Digital Core LDO Output
23	VBAT	Battery Input Voltage
24	VAN	Analog LDO Output
25	VTCXO	TCXO LDO Output
26	REFOUT	Output Reference
27	AGND	Analog Ground
28	TCXOEN	TCXO LDO Enable and MVBAT Enable

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table 1. LDO Control Logic

PHONE STATUS	DDLO	UVLO*	CHRDET	PWRONKEY	PWRONIN	TCXOEN	SIMEN	VSIM	VCORE	VAN & REFOUT	VTCXO	VMEM	VRTC	MVBAT
State #1 battery deep discharged	L	X	X	X	X	L	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF
State #2 phone off	H	L	X	X	X	L	X	OFF	OFF	OFF	OFF	OFF	ON	OFF
State #3 phone off, turn on allowed	H	H	L	H	L	L	X	OFF	OFF	OFF	OFF	OFF	ON	OFF
State #4 charger applied	H	H	H	X	X	L	X	ON	ON	ON	ON	ON	ON	OFF
State #5 phone turned on by user key	H	H	X	L	X	L	X	ON	ON	ON	ON	ON	ON	OFF
State #6 phone turned on by BB	H	H	L	H	H	L	L	OFF	ON	OFF	OFF	ON	ON	OFF
State #7 enable SIM card	H	H	L	H	H	L	H	ON	ON	OFF	OFF	ON	ON	OFF
State #8 phone and TCXO LDO kept on by BB	H	H	L	H	H	H	H	ON	ON	ON	ON	ON	ON	ON

*UVLO is only active when phone is turned off. UVLO is ignored once the phone is turned on.

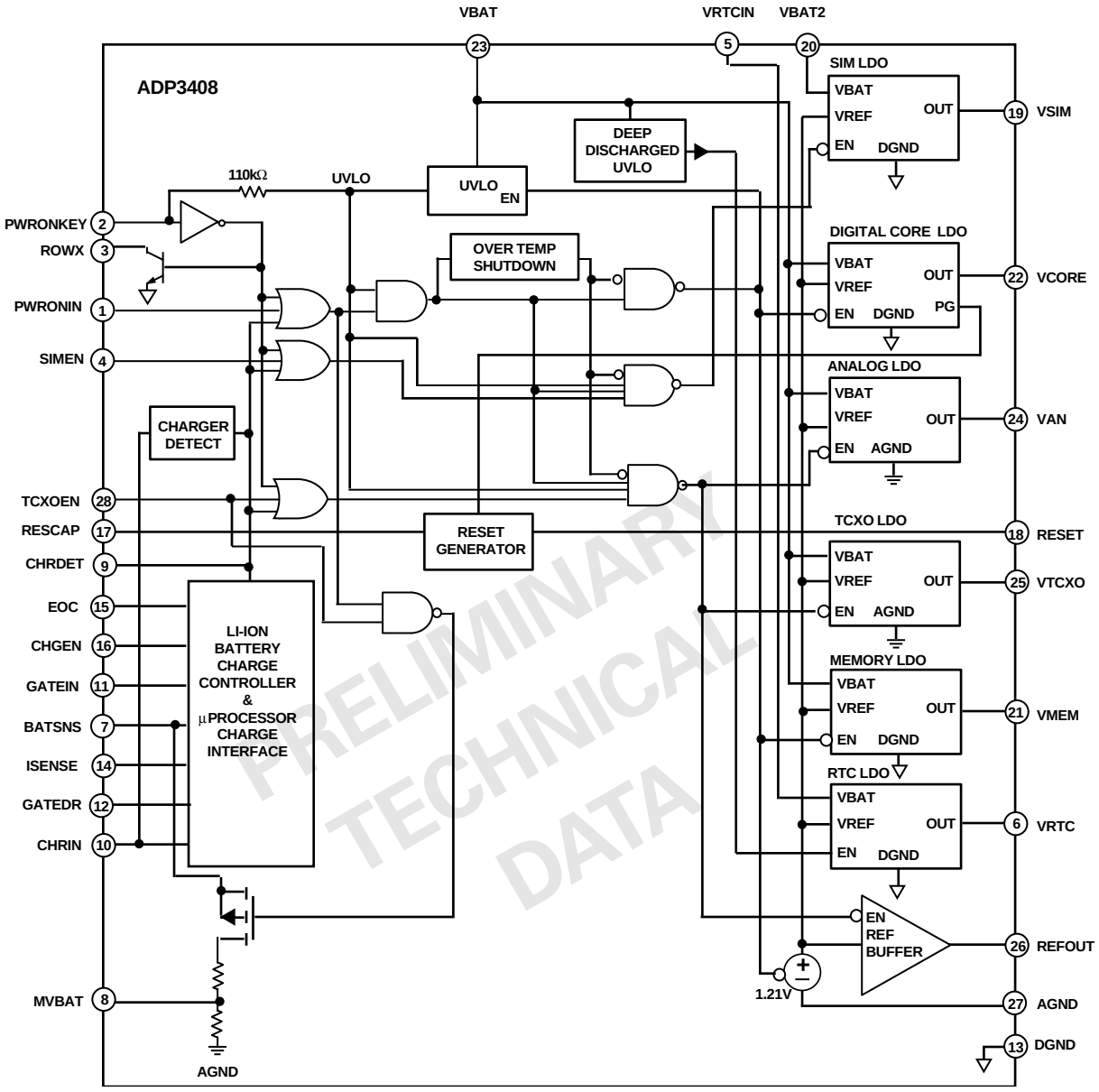


Figure 1. Functional Block Diagram

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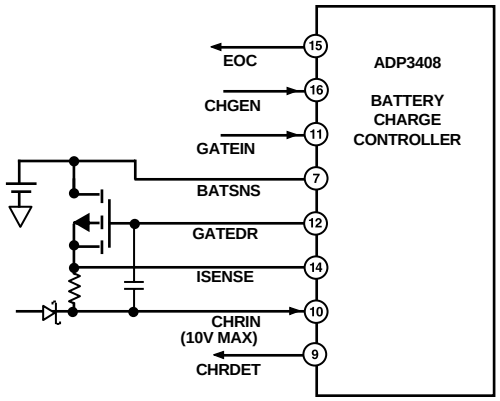

Figure 2. Battery Charger Typical Application

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Thin Shrink Small Outline (TSSOP)
(RU-28)