Dual PLL Frequency Synthesizer

Preliminary Technical Data — ADF4216/ADF4217/ADF4218

FEATURES

ADF4216: 550MHz/1.2GHz
ADF4217: 550MHz/2.0GHz
ADF4218: 550MHz/2.5GHz
+2.7 V to +5.5 V Power Supply
Selectable Charge Pump Currents
Selectable Dual Modulus Prescaler
IF: 8/9 or 16/17
RF: 32/33 or 64/65
3-Wire Serial Interface
Power Down Mode

APPLICATIONS

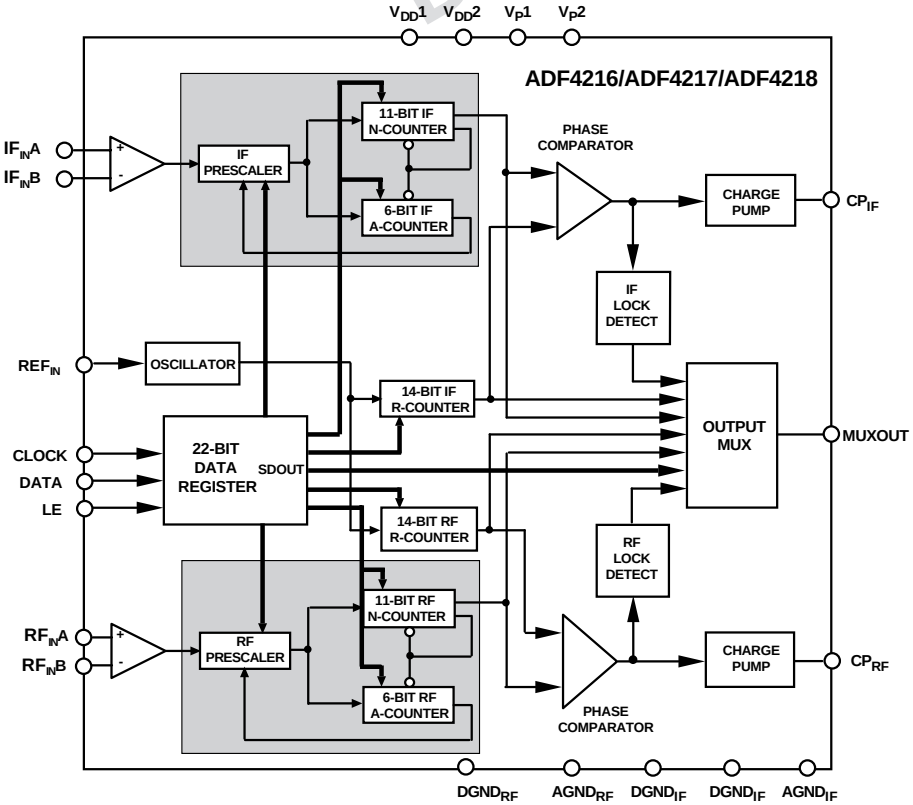
Wireless Handsets (GSM, PCS, DCS, WCDMA)
Base Stations for Wireless Radio (GSM, PCS, DCS, WCDMA)
Wireless LANS
Communications Test Equipment
CATV Equipment

GENERAL DESCRIPTION

The ADF4216/ADF4217/ADF4218 is a dual frequency synthesizer which can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. They can provide the LO for both the RF and IF sections. They consist of a low-noise digital PFD (Phase Frequency Detector), a precision charge pump, a programmable reference divider, programmable A and B counters and a dual-modulus prescaler (P/P+1). The A (6-bit) and B (11-bit) counters, in conjunction with the dual modulus prescaler (P/P+1), implement an N divider (N = BP+A). In addition, the 14-bit reference counter (R Counter), allows selectable REFIN frequencies at the PFD input. A complete PLL (Phase-Locked Loop) can be implemented if the synthesizers are used with an external loop filter and VCO's (Voltage Controlled Oscillators)

Control of all the on-chip registers is via a simple 3-wire interface. The devices operate with a power supply ranging from 2.7V to 5.5V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM



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ADF4216/17/18 – SPECIFICATIONS[1] ($V_{DD}1 = V_{DD}2 = +3$ V ± 10%, +5 V ± 10%; $V_P1, V_P2 = V_{DD}$, +5 V ± 10%; GND = 0 V; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	B Version	BChips[2] (Typical)	Units	Test Conditions/Comments
RF/IF CHARACTERISTICS				
RF Input Frequency (RF_{IN})				
ADF4216	0.1/1.2	0.1/1.2	GHz min/max	
ADF4217	0.1/2.0	0.1/2.0	GHz min/max	
ADF4218	0.1/2.5	0.1/2.5	GHz min/max	
IF Input Frequency (IF_{IN})	25/550	25/550	MHz min/max	
Reference Input Frequency	0/150	0/150	MHz min/max	
Maximum Allowable				
Prescaler Output Frequency[3]	250/200	250/200	MHz typ/max	
Phase Detector Frequency[4]	55	55	MHz max	
RF Input Sensitivity	-15/0	-15/0	dBm min/max	V_{DD} = 3V
	-10/0	-10/0	dBm min/max	V_{DD} = 5V
IF Input Sensitivity	-15/0	-15/0	dBm min/max	V_{DD} = 3V
	-10/0	-10/0	dBm min/max	V_{DD} = 5V
Reference Input Sensitivity	-5	-5	dBm min	ac coupled. Max when dc coupled: 0 to V_{DD} (CMOS compatible)
CHARGE PUMP				
I_{CP} sink/source				
High Value	4.375	4.375	mA typ	
Low Value	1.25	1.25	mA typ	
Absolute Accuracy	2	2	% typ	
	5	5	% max	
I_{CP} 3-State Leakage Current	1	1	nA max	
Sink and Source Current Matching	2	2	% typ	$0.5V < V_{CP} < V_P - 0.5$
I_{CP} vs. V_{CP}	2	2	% typ	$0.5V < V_{CP} < V_P - 0.5$
I_{CP} vs. Temperature	2	2	% typ	$V_{CP} = V_P/2$
LOGIC INPUTS				
V_{INH}, Input High Voltage	0.8 x V_{DD}	0.8 x V_{DD}	V min	
V_{INL}, Input Low Voltage	0.2 x V_{DD}	0.2 x V_{DD}	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
Oscillator Input Current	±100	±100	µA max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	V_{DD} - 0.4	V_{DD} - 0.4	V min	I_{OH} = 1mA
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 1mA
POWER SUPPLIES				
$V_{DD}1$	2.7/5.5	2.7/5.5	V min/V max	
$V_{DD}2$	$V_{CC}1$	$V_{CC}1$		
V_P	$V_{CC}1$/6.0	$V_{CC}1$/6.0	V min/V max	
I_{DD} ($I_{DD}1 + I_{DD}2$)[5]				See Figures X and Y
ADF4216	6.5	6.5	mA max	5.5mA typical
ADF4217	8.5	8.5	mA max	7.5mA typical
ADF4218	9.5	9.5	mA max	8.5mA typical
Low Power Sleep Mode	1	1	µA typ	

NOTES
1. Operating temperature range is as follows: B Version: –40°C to +85°C.
2. The BChip specifications are given as typical values.
3. This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the IF/RF input is divided down to a frequency which is less than this value.
4. Guaranteed by design. Sample tested to ensure compliance.
5. V_{DD} = 3V; P = 16; IF_{IN}/RF_{IN} for ADF4216, ADF4217, ADF4218 = 510MHz/900MHz

ADF4216/17/18 – SPECIFICATIONS[1] ($V_{DD}1 = V_{DD}2 = +3$ V ± 10%, +5 V ± 10%; $V_P1, V_P2 = V_{DD}$, +5 V ± 10%; GND = 0 V; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	B Version	BChips	Units	Test Conditions/Comments
NOISE CHARACTERISTICS				
Phase Noise Floor[2]	-171	-171	dBc/Hz typ	@ 25kHz PFD Frequency
	-164	-164	dBc/Hz typ	@ 200kHz PFD Frequency
Phase Noise Performance[3]				@ VCO Output
ADF4216, ADF4217, ADF4218 (IF)[4]	-95	-95	dBc/Hz typ	
ADF4216 (RF)[5]	-91	-91	dBc/Hz typ	
ADF4216 (RF)[6]	-81	-81	dBc/Hz typ	
ADF4217 (RF)[7]	-85	-85	dBc/Hz typ	
ADF4217 (RF)[8]	-66	-66	dBc/Hz typ	
ADF4218 (RF)[9]	-85	-85	dBc/Hz typ	
Spurious Signals				Measured at offset of $f_{PFD}/2f_{PFD}$
ADF4216, ADF4217, ADF4218 (IF)[4]	-80/-84	-80/-84	dB typ	
ADF4216 (RF)[5]	-80/-84	-80/-84	dB typ	
ADF4216 (RF)[6]	-80/-84	-80/-84	dB typ	
ADF4217 (RF)[7]	-80/-82	-80/-82	dB typ	
ADF4217 (RF)[8]	-78/-82	-78/-82	dB typ	
ADF4218 (RF)[9]	-78/-82	-78/-82	dB typ	

NOTES
1. Operating temperature range is as follows: B Version: –40°C to +85°C.
2. The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where N is the N divider value).
3. The phase noise is measured with the EVAL-ADF421XEB Evaluation Board and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer (f_{REFOUT} = 10MHz @ 0dBm).
4. f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{IF} = 540MHz; N = 2700; Loop B/W = 20kHz
5. f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 900MHz; N = 4500; Loop B/W = 20kHz
6. f_{REFIN} = 10 MHz; f_{PFD} = 30kHz; Offset frequency = 300 Hz; f_{RF} = 836MHz; N = 27867; Loop B/W = 3kHz
7. f_{REFIN} = 10 MHz; f_{PFD} = 200kHz; Offset frequency = 1 kHz; f_{RF} = 1750MHz; N = 8750; Loop B/W = 20kHz
8. f_{REFIN} = 10 MHz; f_{PFD} = 10kHz; Offset frequency = 200Hz; f_{RF} = 1750MHz; N = 175000; Loop B/W = 1kHz
9. f_{REFIN} = 10 MHz; f_{PFD} = 200kHz; Offset frequency = 1 kHz; f_{RF} = 1960MHz; N = 9800; Loop B/W = 20kHz

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADF4216BRU	–40°C to +85°C	RU-20
ADF4216BCP	–40°C to +85°C	CP-24
ADF4217BRU	–40°C to +85°C	RU-20
ADF4217BCP	–40°C to +85°C	CP-24
ADF4218BRU	–40°C to +85°C	RU-20
ADF4218BCP	–40°C to +85°C	CP-24

* RU = Thin Shrink Small Outline Package (TSSOP).
CP = Chip Scale Package
Contact the factory for chip availability

TIMING CHARACTERISTICS

($V_{DD}1 = V_{DD}2 = +3$ V ± 10%, +5 V ± 10%; $V_P1, V_P2 = V_{DD}$, +5 V ± 10%; GND = 0 V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Units	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK Set Up Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	25	ns min	CLOCK High Duration
t_4	25	ns min	CLOCK Low Duration
t_5	10	ns min	CLOCK to LE Set Up Time
t_6	20	ns min	LE Pulse Width

NOTE
Guaranteed by Design but not Production Tested.

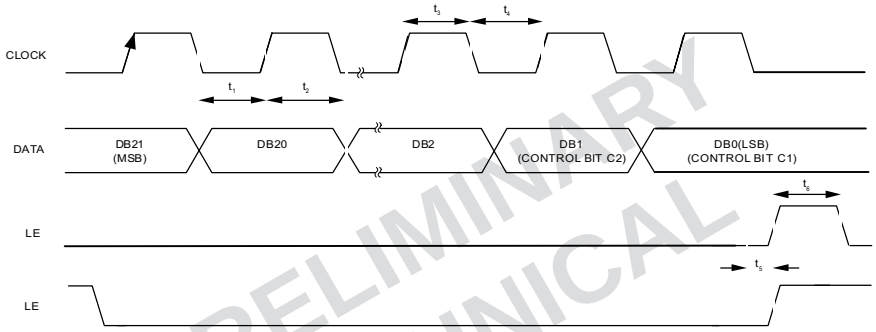


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

$V_{DD}1$ to GND . . . . . –0.3 V to +7 V
$V_{DD}1$ to $V_{DD}2$ . . . . . –0.3 V to +0.3 V
V_P1, V_P2 to GND . . . . . –0.3 V to +7 V
V_P1, V_P2 to $V_{DD}1$ . . . . . –0.3 V to +5.5 V
Digital I/O Voltage to GND . . . . . –0.3 V to DV_{DD} + 0.3 V
Analog I/O Voltage to GND . . . . . –0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$,
$IF_{IN}A$, $IF_{IN}B$ to GND . . . . . –0.3 V to V_{DD} + 0.3V
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . +150°C
TSSOP θ_{JA} Thermal Impedance . . . . . 150.4°C/W
CSP θ_{JA} Thermal Impedance . . . . . TBD°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This device is a high-performance RF integrated circuit with an ESD rating of < 2kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

CAUTION

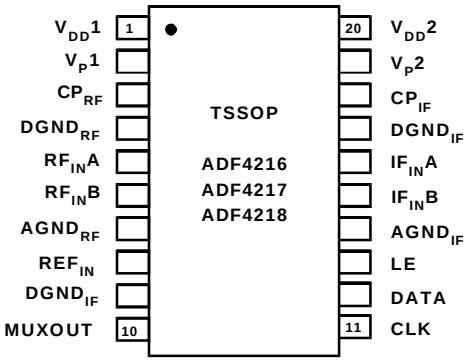
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN DESCRIPTION

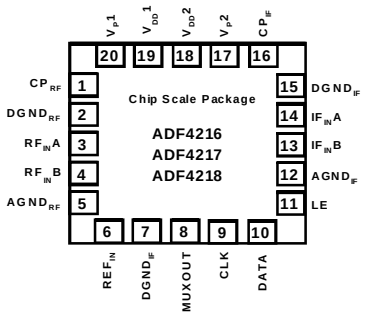
Mnemonic	Function
$V_{DD}1$	Positive power supply for the RF section. A 0.1µF capacitor should be connected between this pin and the RF ground pin, $DGND_{RF}$. $V_{DD}1$ should have a value of between 2.7V and 5.5V. $V_{DD}1$ must have the same potential as $V_{DD}2$.
V_P1	Power supply for the RF charge pump. This should be greater than or equal to V_{DD}.
CP_{RF}	Output from the RF charge pump. This is normally connected to a loop filter which drives the input to an external VCO.
$DGND_{RF}$	Ground pin for the RF digital circuitry.
$RF_{IN}A$	Input to the RF Prescaler. This low-level input signal is normally taken from the RF VCO.
$RF_{IN}B$	Complementary Input to the RF Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor.
$AGND_{RF}$	Ground pin for the RF analog circuitry.
REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100kΩ. See Figure 2. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac coupled.
$DGND_{IF}$	Ground pin for the IF digital, interface and control circuitry.
MUXOUT	This multiplexer output allows either the IF/RF Lock Detect, the scaled RF or the scaled Reference Frequency to be accessed externally. See Table 5.
CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 22-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
$AGND_{IF}$	Ground pin for the IF analog circuitry.
$IF_{IN}B$	Complementary Input to the IF Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor.
$IF_{IN}A$	Input to the IF Prescaler. This low-level input signal is normally taken from the IF VCO.
$DGND_{IF}$	Ground pin for the IF digital, interface and control circuitry.
CP_{IF}	Output from the IF charge pump. This is normally connected to a loop filter which drives the input to an external VCO.
V_P2	Power supply for the IF charge pump. This should be greater than or equal to V_{DD}.
$V_{DD}2$	Positive power supply for the IF, interface and oscillator sections. A 0.1µF capacitor should be connected between this pin and the IF ground pin, $DGND_{IF}$. $V_{DD}2$ should have a value of between 2.7V and 5.5V. $V_{DD}2$ must have the same potential as $V_{DD}1$.

PIN CONFIGURATIONS

TOP VIEW



TOP VIEW



CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The Reference Input stage is shown below in Figure 2. SW1 and SW2 are normally-closed switches. SW3 is normally-

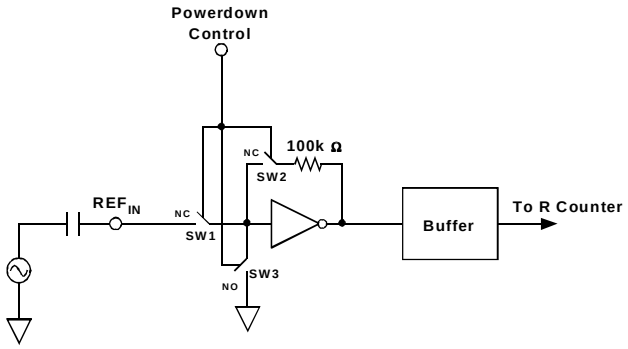


Figure 2. Reference Input Stage

open. When Powerdown is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF$_{IN}$ pin on powerdown.

IF/RF INPUT STAGE

The IF/RF input stage is shown in Figure 3. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

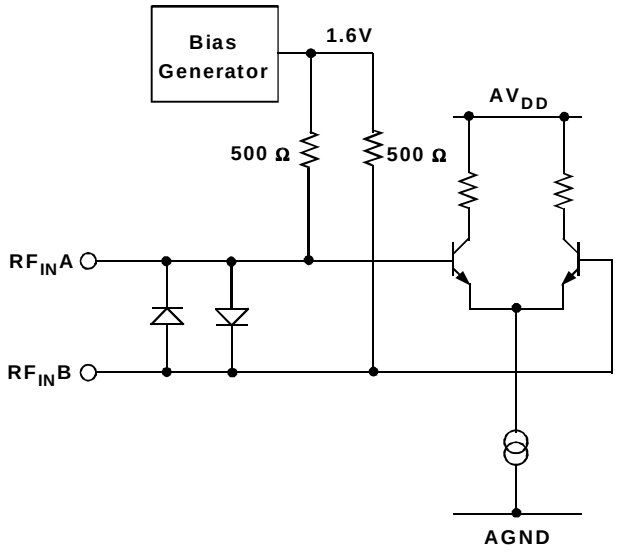


Figure 3. IF/RF Input Stage

PRESCALER

The dual-modulus prescaler takes the CML clock from the IF/RF input stage and divides it down to a manageable frequency for the CMOS A and B counters in the IF and RF sections. It is based on a synchronous 4/5 core. The prescaler is selectable. On the IF side it can be set to either 8/9 (DB20 of the IF AB Counter Latch set to 0) or 16/17 (DB20 set to 1). On the RF side it can be set to 64/65 (DB20 of the RF AB Counter Latch set to 0) or 32/33 (DB20 set to 1). See Tables 4 and 6.

A AND B COUNTERS

The A and B CMOS counters combine with the dual modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The devices are guarenteed to work with a prescaler when the prescaler output is 200MHz or less. Typically they will work with 250MHz output from the prescaler. Thus, with an RF input frequency of 2.5GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

Pulse Swallow Function

The A and B counters, in conjunction with the dual modulus prescaler make it possible to generate output frequencies which are spaced only by the Reference Frequency divided by R . The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times f_{REFIN}/R$$

f_{VCO}: Ouput Frequency of external voltage controlled oscillator (VCO).

P: Preset modulus of dual modulus prescaler.

B: Preset Divide Ratio of binary 11-bit counter (1 to 2047).

A: Preset Divide Ratio of binary 6-bit A counter (0 to 63).

f_{REFIN}: Ouput frequency of the external reference frequency oscillator.

R: Preset divide ratio of binary 14-bit programmable reference counter (1 to 16383).

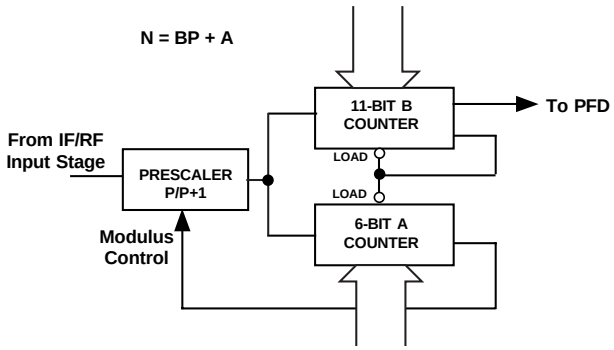


Figure 4. A and B Counters

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the input clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 5 is a simplified schematic.

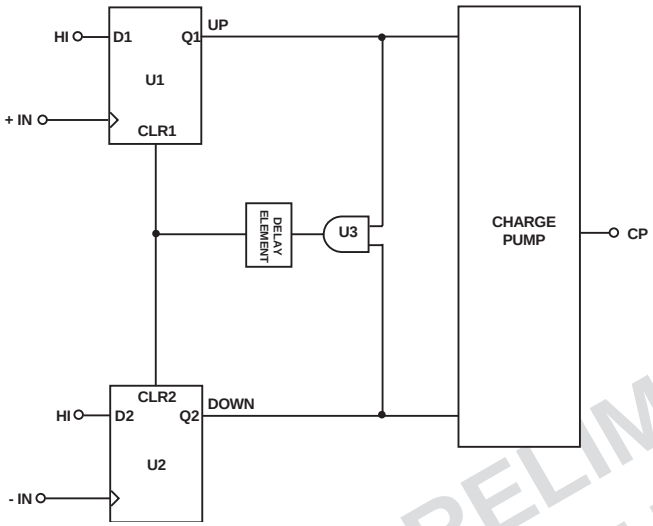


Figure 5. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4216 family allows the user to access various internal points on the chip. The state of MUXOUT is controlled by P3, P4, P11 and P12. See Tables 3 and 5. Figure 6 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for analog lock detect. The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10k nominal. When lock has been detected it is high with narrow low-going pulses .

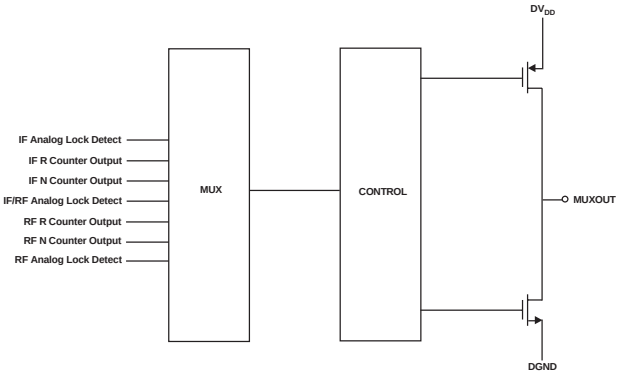


Figure 6. MUXOUT Circuit

INPUT SHIFT REGISTER

The functional block diagram for the ADF4216 family is shown below. The main blocks include a 22-bit input shift register, a 14-bit R counter and an 17-bit N counter, comprising a 6-bit A counter and a 11-bit B counter. Data is clocked into the 22-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two lsb's DB1, DB0 as shown in the timing diagram of Figure 1. The truth table for these bits is shown in Table 1.

Table 1. C2, C1 Truth Table

Control Bits C2	C1	Data Latch
0	0	IF R Counter
0	1	IF N Counter (A and B)
1	0	RF R Counter
1	1	RF N Counter (A and B)

Table 2. ADF4216 Family Latch Summary

IF Reference Counter Latch

IF F_O	IF Lock Detect	3-State CP_{IF}	IF CP Gain	IF PD Polarity	Not Used	14-Bit Reference Counter														Control Bits	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P4	P3	P2	P5	P1		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

IF N Counter Latch

IF Powerdown	IF Prescaler	11-Bit B Counter											Not Used	6-Bit A Counter						Control Bits	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P7	P6	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

RF Reference Counter Latch

RF F_O	RF Lock Detect	3-State CP_{RF}	RF CP Gain	RF PD Polarity	Not Used	14-Bit Reference Counter														Control Bits	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P4	P3	P2	P5	P1		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

RF N Counter Latch

RF Powerdown	RF Prescaler	11-Bit B Counter											Not Used	6-Bit A Counter						Control Bits	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P7	P6	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

Table 3. IF Reference Counter Latch Map

IF F_O	IF Lock Detect	3-State CP_{IF}	IF CP Gain	IF PD Polarity		14-Bit Reference Counter														Control Bits	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P4	P3	P2	P5	P1		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

R14	R13	R12	.....	R3	R2	R1	Divide Ratio
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	16380
1	1	1	.....	1	0	1	16381
1	1	1	.....	1	1	0	16382
1	1	1	.....	1	1	1	16383

P1	PD Polarity
0	Negative
1	Positive

P5	I_{CP}
0	1.25 mA
1	4.375 mA

P2	Charge Pump Output
0	Normal
1	3-State

P12 From RFR Latch	P11 From RFR Latch	P4	P3	MUXOUT
0	0	0	0	Logic Low State
0	0	0	1	IF Analog Lock Detect
0	X	1	0	IF Reference Divider Output
0	X	1	1	IF N Divider Output
0	1	0	0	RF Analog Lock Detect
0	1	0	1	RF/IF Analog Lock Detect
1	X	0	0	RF Reference Divider
1	X	0	1	RF N Divider
1	0	1	0	Fast Lock Output Switch On and connected to MUXOUT
1	0	1	1	IF Counter Reset
1	1	1	0	RF Counter Reset
1	1	1	1	IF and RF Counter Reset

Table 4. IF N Counter Latch Map

IF Power Down	IF Prescaler	11-Bit B Counter												6-Bit A Counter						Control Bits	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P7	P6	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

A6	A5	A4	A3	A2	A1	A Counter Divide Ratio
X	X	0	0	0	0	0
X	X	0	0	0	1	1
X	X	0	0	1	0	2
X	X	0	0	1	1	3
.	.	.	.	.	.	
.	.	.	.	.	.	
.	.	.	.	.	.	
X	X	1	1	1	0	14
X	X	1	1	1	1	15

B11	B10	B9	.....	B3	B2	B1	B Counter Divide Ratio
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	2044
1	1	1	.....	1	0	1	2045
1	1	1	.....	1	1	0	2046
1	1	1	.....	1	1	1	2047

P6	IF Prescaler
0	8/9
1	16/17

P7	IF Section
0	Normal Operation
1	Power Down

N = BP + A, P is prescaler value set by P6
B must be greater than or equal to A
For contiguous values of N, N_{MIN} is (P^2 - P)

Table 5. RF Reference Counter Latch Map

RF F_O	RF Lock Detect	3-State CP_{RF}	RF CP Gain	RF PD Polarity		14-Bit Reference Counter														Control Bits	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P12	P11	P10	P13	P9		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

R14	R13	R12	.....	R3	R2	R1	Divide Ratio
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	16380
1	1	1	.....	1	0	1	16381
1	1	1	.....	1	1	0	16382
1	1	1	.....	1	1	1	16383

P9	PD Polarity
0	Negative
1	Positive

P13	I_{CP}
0	1.25 mA
1	4.375 mA

P10	Charge Pump Output
0	Normal
1	3-State

P12	P11	P4 From IFR Latch	P3 From IFR Latch	MUXOUT
0	0	0	0	Logic Low State
0	0	0	1	IF Analog Lock Detect
0	X	1	0	IF Reference Divider Output
0	X	1	1	IF N Divider Output
0	1	0	0	RF Analog Lock Detect
0	1	0	1	RF/IF Analog Lock Detect
1	X	0	0	RF Reference Divider
1	X	0	1	RF N Divider
1	0	1	0	Fast Lock Output Switch On and connected to MUXOUT
1	0	1	1	IF Counter Reset
1	1	1	0	RF Counter Reset
1	1	1	1	IF and RF Counter Reset

Table 6. RF N Counter Latch Map

RF Power Down	RF Prescaler	11-Bit B Counter												6-Bit A Counter						Control Bits	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	P14	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

A6	A5	A4	A3	A2	A1	A Counter Divide Ratio
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
.	.	.	.	.	.	
.	.	.	.	.	.	
.	.	.	.	.	.	
1	1	1	1	1	0	62
1	1	1	1	1	1	63

B11	B10	B9		B3	B2	B1	B Counter Divide Ratio
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	2044
1	1	1	.....	1	0	1	2045
1	1	1	.....	1	1	0	2046
1	1	1	.....	1	1	1	2047

P14	RF Prescaler ADF4216/ADF4217	RF Prescaler ADF4218
0	64/65	32/33
1	32/33	64/65

P16	RF Section
0	Normal Operation
1	Power Down

N = BP + A, P is prescaler value set by P6
B must be greater than or equal to A
For contiguous values of N, N_{MIN} is $(P^2 - P)$

PROGRAM MODES

Table 3 and Table 5 show how to set up the Program Modes in the ADF4216 family. The following should be noted:

1. IF and RF Analog Lock Detect indicate when the PLL is in lock. When the loop is locked and either IF or RF Analog Lock Detect is selected, then the MUXOUT pin will show a logic high with narrow low-going pulses. When the IF/RF Analog Lock Detect is chosen then the locked condition is indicated only when both IF and RF loops are locked.
2. The IF Counter Reset mode resets the R and N counters in the IF section and also puts the IF charge pump into 3-state. The RF Counter Reset mode resets the R and N counters in the RF section and also puts the RF charge pump into 3-state. The IF and RF Counter Reset mode does both of the above.
   Upon removal of the reset bits, the N counter resumes counting in close alignment with the R counter (maximum error is one prescaler output cycle).
3. The Fastlock mode uses MUXOUT to switch a second loop filter damping resistor to ground during Fastlock operation. Activation of Fastlock occurs whenever RF CP Gain in the RF Reference counter is set to one.

POWERDOWN

It is possible to program the ADF4216 family for either synchronous or asynchronous powerdown on either the IF or RF side.

Synchronous IF Power Down.

Programming a “1” to P7 of the ADF4216 family will initiate a power down. If P2 of the ADF4216 family has been set to “0” (normal operation), then a synchronous power down is conducted. The device will automatically put the charge pump into 3-state and then complete the power down.

Asynchronous IF Power Down

If P2 of the ADF4216 families has been set to “1” (3-state the IF charge pump), and P7 is subsequently set to "1", then an asynchronous power down is conducted. The device will go into power down on the rising edge of LE which latches the “1” to the IF Power Down bit (P7).

Synchronous RF Power Down.

Programming a “1” to P16 of the ADF4216 family will initiate a power down. If P10 of the ADF4216 family has been set to “0” (normal operation), then a synchronous power down is conducted. The device will automatically put the charge pump into 3-state and then complete the power down.

Asynchronous RF Power Down

If P10 of the ADF4216 families has been set to “1” (3-state the RF charge pump), and P16 is subsequently set to "1", then an asynchronous power down is conducted. The device will go into power down on the rising edge of LE which latches the “1” to the RF Power Down bit (P16).

Activation of either synchronous or asynchronous power down forces the IF/RF loop’s R and N dividers to their load state conditions and the IF/RF input section is debiased to a high impedance state.

The REF_{IN} oscillator circuit is only disabled if both the IF and RF Power Downs are set.

The input register and latches remain active and are capable of loading and latching data during all the power down modes.

The IF/RF section of the devices will return to normal powered-up operation immediately upon LE latching a “0” to the appropriate Power Down bit.