Dual PLL Frequency Synthesizer

Preliminary Technical Data — ADF4210/ADF4211/ADF4212/ADF4213

FEATURES

ADF4210: 550MHz/1.2GHz
ADF4211: 550MHz/2.0GHz
ADF4212: 1.0GHz/2.7GHz
ADF4213: 1.0GHz/3GHz
+2.7 V to +5.5 V Power Supply
Separate V_p Allows Extended Tuning Voltage in 3V Systems
Programmable Dual Modulus Prescaler
RF & IF: 8/9, 16/17, 32/33, 64/65
Programmable Charge Pump Currents
3-Wire Serial Interface
Power Down Mode

APPLICATIONS

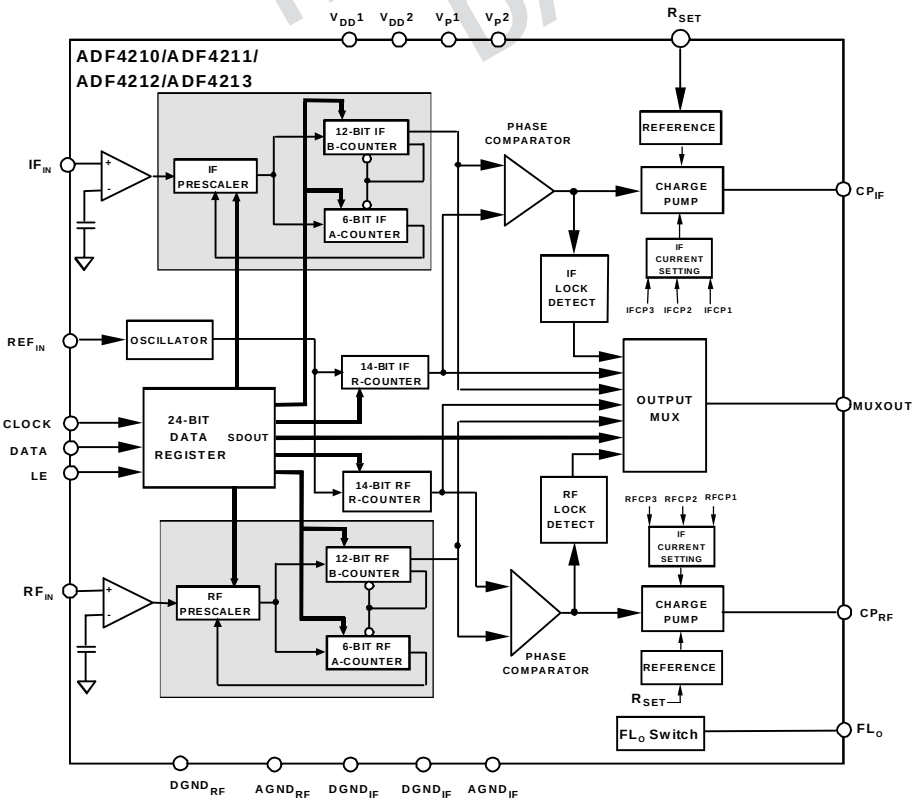
Wireless Handsets (GSM, PCS, DCS, WCDMA)
Base Stations for Wireless Radio (GSM, PCS, DCS, WCDMA)
Wireless LANS
Communications Test Equipment
Cable TV Tuners (CATV)

GENERAL DESCRIPTION

The ADF4210/ADF4211/ADF4212/ADF4213 is a dual frequency synthesizer which can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. They can provide the LO for both the RF and IF sections. They consist of a low-noise digital PFD (Phase Frequency Detector), a precision charge pump, a programmable reference divider, programmable A and B counters and a dual-modulus prescaler (P/P+1). The A (6-bit) and B (12-bit) counters, in conjunction with the dual modulus prescaler (P/P+1), implement an N divider (N= BP+A). In addition, the 14-bit reference counter (R Counter), allows selectable REFIN frequencies at the PFD input. A complete PLL (Phase-Locked Loop) can be implemented if the synthesizers are used with an external loop filter and VCO's (Voltage Controlled Oscillators)

Control of all the on-chip registers is via a simple 3-wire interface. The devices operate with a power supply ranging from 2.7V to 5V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM



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ADF4210/11/12/13 – SPECIFICATIONS[1]

($V_{DD}1 = V_{DD}2 = +3V \pm 10\%$, +5 V ± 10% $V_P1, V_P2 = V_{DD}$, +5 V ± 10%, ; AGND = DGND = 0 V; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	B Version	BChips[2] (Typical)	Units	Test Conditions/Comments
RF CHARACTERISTICS				
RF Input Frequency (RF_{IN})				See Figure 3 for input circuit
ADF4210	25/550	25/550	MHz min/max	
ADF4211	0.1/1.2	0.1/1.2	GHz min/max	
ADF4212	0.1/2.7	0.1/2.7	GHz min/max	
ADF4213	0.1/3.0	0.1/3.0	GHz min/max	
IF Input Frequency (IF_{IN})				
ADF4210	25/550	25/550	MHz min/max	
ADF4211	25/550	25/550	GHz min/max	
ADF4212	0.1/1.0	0.1/1.0	GHz min/max	
ADF4213	0.1/1.0	0.1/1.0	GHz min/max	
Reference Input Frequency	0/150	0/150	MHz min/max	
Maximum Allowable Prescaler Output Frequency[3]	200	200	MHz max	
Phase Detector Frequency[4]	55	55	MHz max	
RF Input Sensitivity	-10/0	-10/0	dBm min/max	V_{DD} = 3V
	-5/0	-5/0	dBm min/max	V_{DD} = 5V
IF Input Sensitivity	-10/0	-10/0	dBm min/max	V_{DD} = 3V
	-5/0	-5/0	dBm min/max	V_{DD} = 5V
Reference Input Sensitivity	-5	-5	dBm min	ac coupled. Max when dc coupled: 0 to V_{DD} (CMOS compatible)
CHARGE PUMP				
I_{CP} sink/source				Programmable: See table 5.
High Value	5	5	mA typ	With R_{SET} = 2.7kΩ
Low Value	625	625	µA typ	
Absolute Accuracy	2	2	% typ	With R_{SET} = 2.7kΩ
	5	5	% max	
R_{SET} Range	1.5/5.6	1.5/5.6	kΩ min/max	
I_{CP} 3-State Leakage Current	1	1	nA max	See Figure 28
Sink and Source Current Matching	2	2	% typ	$0.5V < V_{CP} < V_P - 0.5$
I_{CP} vs. V_{CP}	2	2	% typ	$0.5V < V_{CP} < V_P - 0.5$
I_{CP} vs. Temperature	2	2	% typ	$V_{CP} = V_P/2$
LOGIC INPUTS				
V_{INH}, Input High Voltage	0.8 x V_{DD}	0.8 x V_{DD}	V min	
V_{INL}, Input Low Voltage	0.2 x V_{DD}	0.2 x V_{DD}	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
Oscillator Input Current	±100	±100	µA max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	V_{DD} - 0.4	V_{DD} - 0.4	V min	I_{OH} = 1mA
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 1mA
POWER SUPPLIES				
$V_{DD}1$	2.7/5.5	2.7/5.5	V min/V max	
$V_{DD}2$	$V_{DD}1$	$V_{DD}1$		
V_P1, V_P2	$V_{DD}1$/6.0	$V_{DD}1$/6.0	V min/V max	

NOTES
1. Operating temperature range is as follows: B Version: –40°C to +85°C.
2. The BChip specifications are given as typical values.
3. This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency which is less than this value.
4. Guaranteed by deign. Sample tested to ensure compliance.

ADF4210/11/12/13–SPECIFICATIONS[1] ($V_{DD}1 = V_{DD}2 = +3V \pm 10\%$, +5 V ± 10% $V_P1, V_P2 = V_{DD,}$ +5 V ± 10%, ; AGND = DGND = 0 V; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	B Version	BChips[2] (Typical)	Units	Test Conditions/Comments
POWER SUPPLIES				
I_{DD} ($I_{DD}1 + I_{DD}2$)[3]				
(RF + IF)				See Figure X and Y
ADF4210	6.5	6.5	mA max	2.5mA typical
ADF4211	8.5	8.5	mA max	3.5mA typical
ADF4212	9.5	9.5	mA max	3.5mA typical
ADF4213	10	10	mA max	4.5mA typical
(RF only)				
ADF4210	tbd	tbd	mA max	2.5mA typical
ADF4211	tbd	tbd	mA max	3.5mA typical
ADF4212	tbd	tbd	mA max	3.5mA typical
ADF4213	tbd	tbd	mA max	4.5mA typical
(IF only)				
ADF4210	tbd	tbd	mA max	2.5mA typical
ADF4211	tbd	tbd	mA max	3.5mA typical
ADF4212	tbd	tbd	mA max	3.5mA typical
ADF4213	tbd	tbd	mA max	4.5mA typical
Low Power Sleep Mode	1	1	µA typ	
NOISE CHARACTERISTICS				
ADF4213 Phase Noise Floor[4]	-170	-170	dBc/Hz typ	@ 25kHz PFD Frequency
	-164	-164	dBc/Hz typ	@ 200kHz PFD Frequency
Phase Noise Performance[5]				@ VCO Output
ADF4210[6]	-95	-95	dBc/Hz typ	
ADF4213[7]	-90	-90	dBc/Hz typ	
ADF4212[8]	-83	-83	dBc/Hz typ	
ADF4211[9]	-86	-86	dBc/Hz typ	
ADF4212[10]	-73	-73	dBc/Hz typ	
ADF4212[11]	-85	-85	dBc/Hz typ	
ADF4213[12]	-85	-85	dBc/Hz typ	
Spurious Signals				Measured at offset of $f_{PFD}/2f_{PFD}$
ADF4210[6]	-80/-84	-80/-84	dBc typ	
ADF4211[7]	-80/-84	-80/-84	dBc typ	
ADF4212[8]	-80/-84	-80/-84	dBc typ	
ADF4212[9]	-80/-84	-80/-84	dBc typ	
ADF4212[10]	-80/-82	-80/-82	dBc typ	
ADF4212[11]	-75/-79	-75/-79	dBc typ	
ADF4213[12]	-78/-82	-78/-82	dBc typ	

NOTES

1. Operating temperature range is as follows: B Version: –40°C to +85°C.
2. The BChip specifications are given as typical values.
3. V_{DD} = 3V; P=16; IF_{IN}/RF_{IN} for ADF4210, ADF4211, ADF4212, ADF4213 = 540MHz/900MHz.
4. The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where N is the N divider value).
5. The phase noise is measured with the EVAL-ADF421XEB Evaluation Board and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer. (f_{REFOUT} = 10MHz @ 0dBm)
6. f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 540MHz; N = 2700; Loop B/W = 20kHz
7. f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 900MHz; N = 4500; Loop B/W = 20kHz
8. f_{REFIN} = 10 MHz; f_{PFD} = 30kHz; Offset frequency = 300 Hz; f_{RF} = 836MHz; N = 27867; Loop B/W = 3kHz
9. f_{REFIN} = 10 MHz; f_{PFD} = 200kHz; Offset frequency = 1 kHz; f_{RF} = 1750MHz; N = 8750; Loop B/W = 20kHz
10. f_{REFIN} = 10 MHz; f_{PFD} = 10kHz; Offset frequency = 200 Hz; f_{RF} = 1750MHz; N = 175000; Loop B/W = 1kHz
11. f_{REFIN} = 10 MHz; f_{PFD} = 200kHz; Offset frequency = 1 kHz; f_{RF} = 1960MHz; N = 9800; Loop B/W = 20kHz
12. f_{REFIN} = 10 MHz; f_{PFD} = 1MHz; Offset frequency = 1 kHz; f_{RF} = 2800MHz; N = 2800; Loop B/W = 20kHz

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADF4210BRU	–40°C to +85°C	RU-20
ADF4210BCP	–40°C to +85°C	CP-24
ADF4211BRU	–40°C to +85°C	RU-20
ADF4211BCP	–40°C to +85°C	CP-24
ADF4212BRU	–40°C to +85°C	RU-20
ADF4212BCP	–40°C to +85°C	CP-24
ADF4213BRU	–40°C to +85°C	RU-20
ADF4213BCP	–40°C to +85°C	CP-24

* RU = Thin Shrink Small Outline Package (TSSOP)
CP = Chip Scale Package
Contact the factory for chip availability

TIMING CHARACTERISTICS

($V_{DD}1 = V_{DD}2 = +3V \pm 10\%$, $+5\ V \pm 10\%$ $V_P1, V_P2 = V_{DD,}$ $+5\ V \pm 10\%$, ; AGND = DGND = 0 V; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Units	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK Set Up Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	25	ns min	CLOCK High Duration
t_4	25	ns min	CLOCK Low Duration
t_5	10	ns min	CLOCK to LE Set Up Time
t_6	20	ns min	LE Pulse Width

NOTE
Guaranteed by Design but not Production Tested.

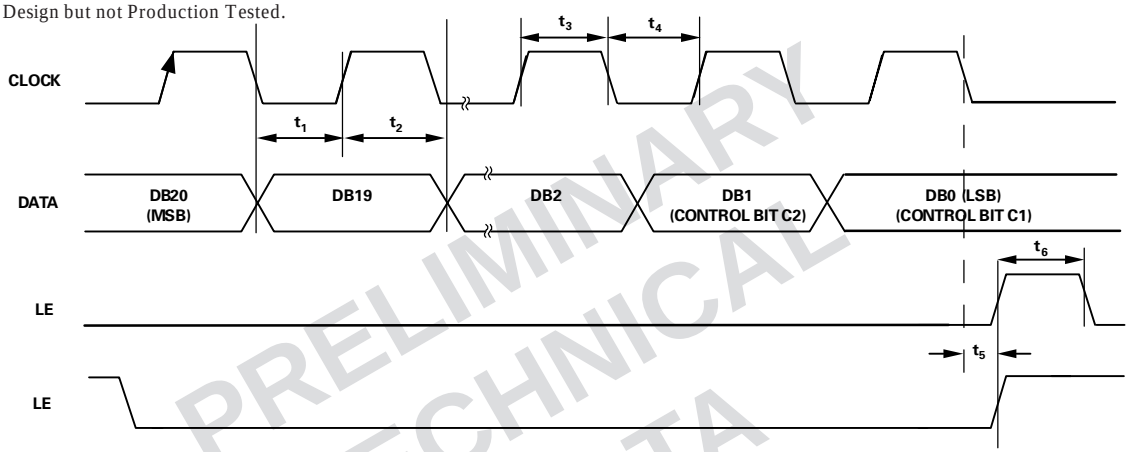


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

$V_{DD}1$ to GND ..... –0.3 V to +7 V
$V_{DD}1$ to $V_{DD}2$ ..... –0.3 V to +0.3 V
V_P1, V_P2 to GND ..... –0.3 V to +7 V
V_P1, V_P2 to $V_{DD}1$ ..... –0.3 V to +5.5 V
Digital I/O Voltage to GND ... –0.3 V to DV_{DD} + 0.3 V
Analog I/O Voltage to GND ..... –0.3 V to V_p + 0.3V
REFIN,RFIN,IFIN to GND ....–0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (B Version) .....–40°C to +85°C
Storage Temperature Range .....–65°C to +150°C
Maximum Junction Temperature .....+150°C
TSSOP θ_{JA} Thermal Impedance ..... 150.4°C/W
CSP θ_{JA} Thermal Impedance ..... TBD°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) .....+215°C
Infrared (15 sec) .....+220°C

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This device is a high-performance RF integrated circuit with an ESD rating of < 2kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.
3. AGND = DGND = 0V

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

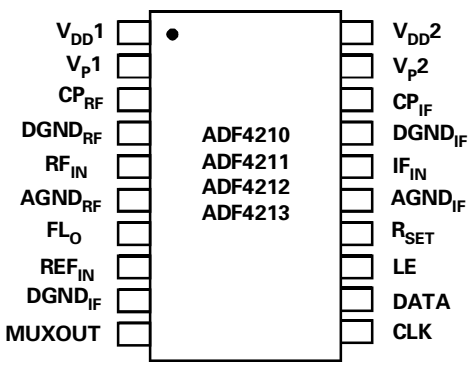
PIN DESCRIPTION

Mnemonic	Function
$V_{DD}1$	Power supply for the RF section. A 0.1uF capacitor should be connected between this pin and GND. $V_{DD}1$ has a value +5V 10% or 3V 10%. $V_{DD}1$ must have the same potential as $V_{DD}2$.
Vp1	RF Charge Pump Power Supply. This should be greater than or equal to $V_{DD}1$.
CP_{RF}	RF Charge Pump Output. This is normally connected to a loop filter which drives the input to an external VCO.
$DGND_{RF}$	Digital Ground for the RF digital circuitry.
RF_{IN}	Input to the RF Prescaler. This small signal input is normally taken from the VCO.
$AGND_{RF}$	Analog Ground for the RF analog circuitry.
FL_o	Multiplexed output of RF/IF programmable or reference dividers, RF/IF fastlock mode. CMOS output.
REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100kΩ. This input can be driven from a TTL or CMOS crystal oscillator.
$DGND_{IF}$	Digital Ground for the IF digital,interface and control circuitry
MUXOUT	This multiplexer output allows either the IF/RF Lock Detect, the scaled RF, scaled IF or the scaled Reference Frequency to be accessed externally.
CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 22-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
R_{SET}	Connecting a resistor between this pin and ground sets the maximum RF and IF charge pump output current. The relationship between I_{CP} and R_{SET} is $$I_{CP\max} = \frac{13.5}{R_{SET}}$$ So, with R_{SET} = 2.7kΩ, I_{CPmax} = 5mA for both the RF and IF Charge Pumps.
$AGND_{IF}$	Analog Ground for the IF analog circuitry.
IF_{IN}	Input to the RF Prescaler. This small signal input is normally taken from the VCO.
$DGND_{IF}$	Digital Ground for the IF digital,interface and control circuitry
CP_{IF}	IF Charge Pump Output. This is normally connected to a loop filter which drives the input to an external VCO.
Vp2	IF Charge Pump Power Supply. This should be greater than or equal to V_{DD}.
$V_{DD}2$	Power supply for the IF section. A 0.1uF capacitor should be connected between this pin and GND. $V_{DD}2$ has a value +5V ±10% or 3V ±10%. $V_{DD}2$ must have the same potential as $V_{DD}1$.

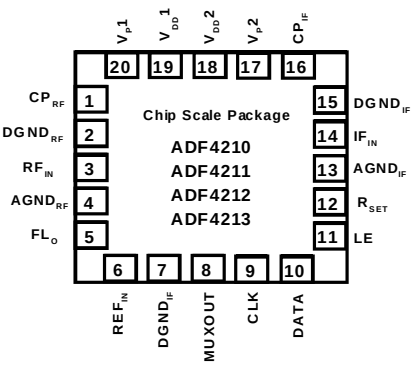
NOTES
1. MUXOUT is also used for Test Modes on the devices. These Test modes will be detailed in TNXXX available from Analog Devices Inc.

PIN CONFIGURATION

TOP VIEW



TOP VIEW



CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The Reference Input stage is shown below in Figure 2. SW1 and SW2 are normally-closed switches. SW3 is

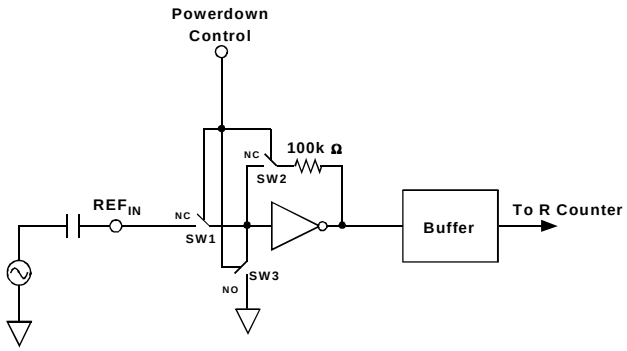


Figure 2. Reference Input Stage

normally-open. When Powerdown is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF$_{IN}$ pin on powerdown.

RF/IF INPUT STAGE

The RF/IF input stage is shown in Figure 3. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

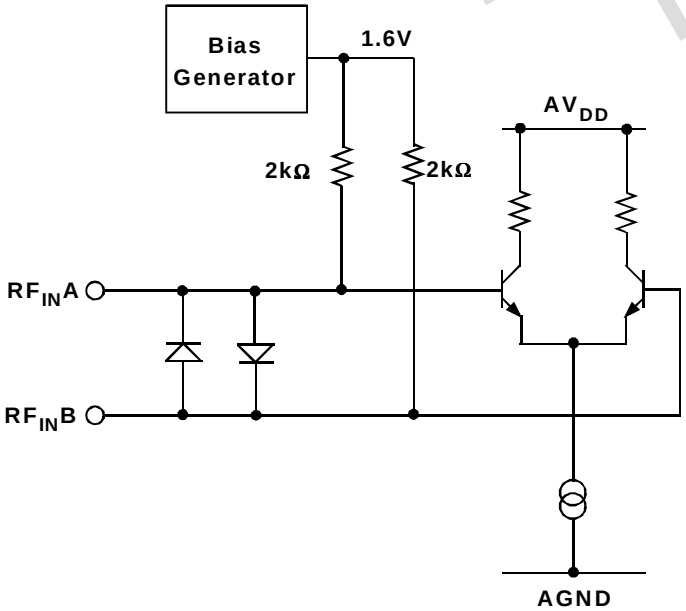


Figure 3. RF/IF Input Stage

PRESCALER

The dual-modulus prescaler takes the CML clock from the RF/IF input stage and divides it down to a manageable frequency for the CMOS A and B counters in the RF and IF sections. It is based on a synchronous 4/5 core. The prescaler in both sections is selectable. It can be set in software to 8/9, 16/17, 32/33 or 64/65. See tables 4 and 6.

RF/IF A AND B COUNTERS

The A and B CMOS counters combine with the dual modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are guaranteed to work when the prescaler output is 200MHz or less. Typically, they will work with 250MHz output from the prescaler. Thus, with an RF input frequency of 2.5GHz, a prescaler value of 16/17 is valid, but a value of 8/9 is not valid.

Pulse Swallow Function

The A and B counters, in conjunction with the dual modulus prescaler make it possible to generate output frequencies which are spaced only by the Reference Frequency divided by R . The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times f_{REFIN}/R$$

f_{VCO}: Ouput Frequency of external voltage controlled oscillator (VCO).

P: Preset modulus of dual modulus prescaler.

B: Preset Divide Ratio of binary 13-bit counter (3 to 8191).

A: Preset Divide Ratio of binary 6-bit swallow counter (0 to 63).

f_{REFIN}: Ouput frequency of the external reference frequency oscillator.

R: Preset divide ratio of binary 14-bit programmable reference counter (1 to 16383)

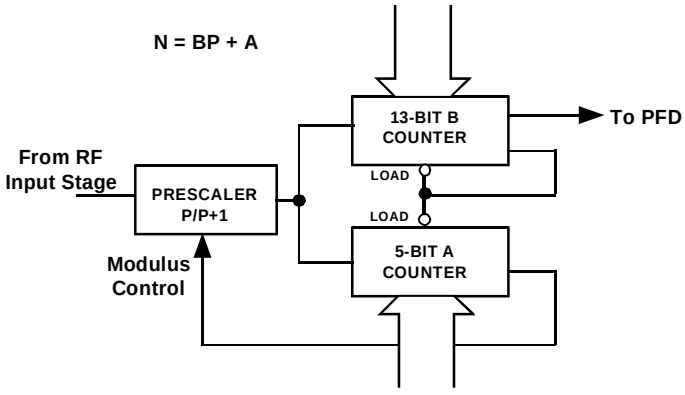


Figure 4. RF/IF A and B Counters

RF/IF R COUNTER

The 14-bit RF/IF R counter allows the input reference frequency to be divided down to produce the input clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 5 is a simplified schematic. The PFD includes a fixed delay element

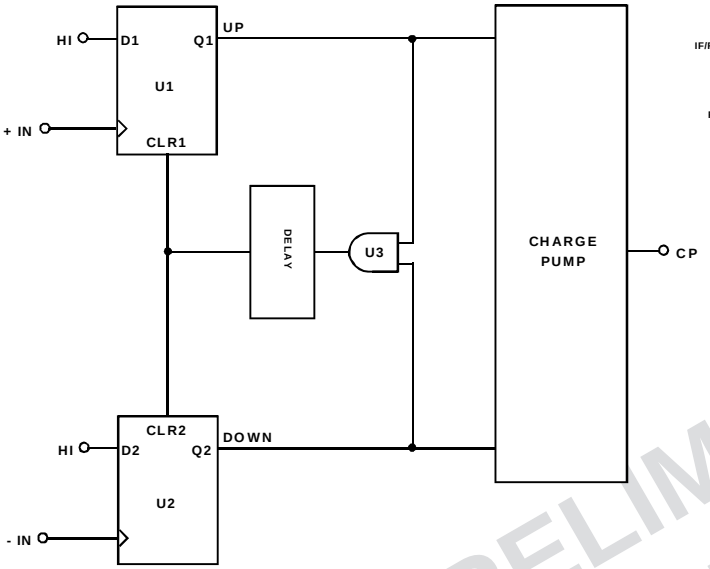


Figure 5. RF/IF PFD Simplified Schematic

which sets the width of the anti-backlash pulse. This is typically 3ns. This pulse ensures that there is no deadzone in the PFD transfer function and gives a consistent reference spur level.

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4210 family allows the user to access various internal points on the chip. The state of MUXOUT is controlled by P3, P4, P11 and P12. See Table 3 and Table 5. Figure 6 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for two types of lock detect:

Digital Lock Detect and Analog Lock Detect

Digital Lock Detect is active high. It is set high when the phase error on three consecutive Phase Detector cycles is less than 15ns. It will stay set high until a phase error of greater than 25ns is detected on any subsequent PD cycle. The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10k nominal. When lock has been detected it is high with narrow low-going pulses.

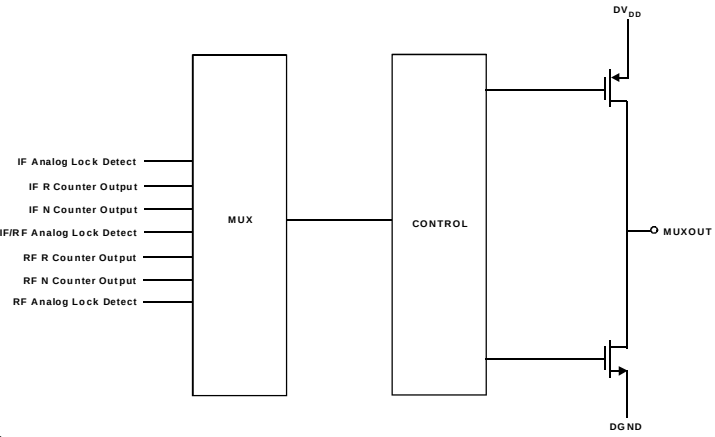


Figure 6. MUXOUT Schematic

RF/IF INPUT SHIFT REGISTER

The ADF4210 family digital section includes a 24-bit input shift register, a 14-bit IF R counter and a 18-bit IF N counter, comprising a 6-bit IF A counter and a 12-bit IF B counter. Also present is a 14-bit RF R counter and a 18-bit RF N counter, comprising a 6-bit RF A counter and a 12-bit RF B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two lsb's DB1, DB0 as shown in the timing diagram of Figure 1. The truth table for these bits is shown in Table 6. Table 1 shows a summary of how the latches are programmed.

Table 1. C2, C1 Truth Table

Control Bits C2	C1	Data Latch
0	0	IF R Counter
0	1	IF N Counter (A and B)
1	0	RF R Counter
1	1	RF N Counter (A and B)

Table 2. ADF4210 Family Latch Summary

IF R Counter Latch

IF CP Current Setting			IF Fo	Lock Detect Precision	3-State CP	IF PD Polarity		14-Bit Reference Counter												Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
IFCP 2	IFCP 1	IFCP 0	P4	P3	P2	P1		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

IF N Counter Latch

IF CP Gain	IF Power Down	IF Prescaler		12-Bit B Counter												6-Bit A Counter						Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P8	P7	P6	P5	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

RF R Counter Latch

RF CP Current Setting			RF Fo	RF Lock Detect	3-State CP	RF PD Polarity		14-Bit RF Reference Counter												Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RFCP 2	RFCP 1	RFCP 0	P12	P11	P10	P9		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

RF N Counter Latch

RF CP Gain	RF Power Down	RF Prescaler		12-Bit B Counter												6-Bit A Counter						Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P17	P16	P15	P14	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

IF R COUNTER LATCH

Table 3. IF R Counter Latch Map

IF CP Current Setting			IF Fo	Lock Detect Precision	3-State CP	IF PD Polarity		14-Bit Reference Counter														Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
IFCP 2	IFCP 1	IFCP 0	P4	P3	P2	P1		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

R14	R13	R12	.....	R3	R2	R1	Divide Ratio
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	16380
1	1	1	.....	1	0	1	16381
1	1	1	.....	1	1	0	16382
1	1	1	.....	1	1	1	16383

F3	IF PD Polarity
0	Negative
1	Positive

F3	Charge Pump Output
0	Normal
1	3-State

P12	P11	P4	P3	Muxout
From RF R Latch				
0	0	0	0	Logic Low State
0	0	0	1	IF Analog Lock Detect
0	0	1	0	IF Reference Divider Output
0	0	1	1	IF N Divider Ouput
0	1	0	0	RF Analog Lock Detect
0	1	0	1	RF/IF Analog Lock Detect
0	1	1	0	IF Digital Lock Detect
0	1	1	1	Logic High State
1	0	0	0	RF Reference Divider Output
1	0	0	1	RF N Divider Output
1	0	1	0	3-State Output
1	0	1	1	IF Counter Reset
1	1	0	0	RF Digital Lock Detect
1	1	0	1	RF/IF Digital Lock Detect
1	1	1	0	RF Counter Reset
1	1	1	1	IF and RF Counter Reset

CPI6	CPI5	CP14	I_{CP} (mA)		
CPI3	CPI2	CPI1	2.7kΩ	4.7kΩ	10kΩ
0	0	0	1.088	0.625	0.294
0	0	1	2.176	1.25	0.588
0	1	0	3.264	1.875	0.882
0	1	1	4.352	2.5	1.176
1	0	0	5.44	3.125	1.47
1	0	1	6.528	3.75	1.764
1	1	0	7.616	4.375	2.058
1	1	1	8.704	5.0	2.352

IF N COUNTER LATCH

Table 4. IF N Counter Latch Map

IF CP Gain	IF Power Down	IF Prescaler		12-Bit B Counter												6-Bit A Counter						Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P8	P7	P6	P5	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

P6	P5	Prescaler Value
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

P7	IF Power Down
0	Disable
1	Enabled

A6	A5	.....	A2	A1	A Counter Divide Ratio
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
0	0	.....	0	0	4
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	60
1	1	.....	0	1	61
1	1	.....	1	0	62
1	1	.....	1	1	63

B12	B11	B10	.....	B3	B2	B1	B Counter Divide Ratio
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	4092
1	1	1	.....	1	0	1	4093
1	1	1	.....	1	1	0	4094
1	1	1	.....	1	1	1	4095

P8	IF CP Gain
0	Disable
1	Enabled

N = BP + A, P is prescaler value set in the Function Latch
B must be greater than or equal to A
For contiguous values of , N_{MIN} is $(P^2 - P)$

RF R COUNTER LATCH

Table 5. RF R Counter Latch Map

RF CP Current Setting			RF Fo	RF Lock Detect	3-State CP	RF PD Polarity		14-Bit RF Reference Counter													Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RFCP 2	RFCP 1	RFCP 0	P12	P11	P10	P9		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

R14	R13	R12	.....	R3	R2	R1	Divide Ratio
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	16380
1	1	1	.....	1	0	1	16381
1	1	1	.....	1	1	0	16382
1	1	1	.....	1	1	1	16383

P9	RF PD Polarity
0	Negative
1	Positive

P10	RF Charge Pump Output
0	Normal
1	3-State

P12	P11	P4	P3	Muxout
		From IF R Latch		
0	0	0	0	Logic Low State
0	0	0	1	IF Analog Lock Detect
0	0	1	0	IF Reference Divider Output
0	0	1	1	IF N Divider Ouput
0	1	0	0	RF Analog Lock Detect
0	1	0	1	RF/IF Analog Lock Detec
0	1	1	0	IF Digital Lock Detect
0	1	1	1	Logic High State
1	0	0	0	RF Reference Divider Output
1	0	0	1	RF N Divider Output
1	0	1	0	3-State Output
1	0	1	1	IF Counter Reset
1	1	0	0	RF Digital Lock Detect
1	1	0	1	RF/IF Digital Lock Detect
1	1	1	0	RF Counter Reset
1	1	1	1	IF and RF Counter Reset

RF CP2	RF CP1	RF CP0	I_{CP} (mA)		
			1.5kΩ	2.7kΩ	5.6kΩ
0	0	0	1.125	0.625	0.301
0	0	1	2.25	1.25	0.602
0	1	0	3.375	1.875	0.904
0	1	1	4.5	2.5	1.205
1	0	0	5.625	3.125	1.506
1	0	1	6.75	3.75	1.808
1	1	0	7.7875	4.375	2.109
1	1	1	9	5.0	2.411

RF N COUNTER LATCH

Table 6. RFN Counter Latch Map

RF CP Gain	RF Power Down	RF Prescaler		12-Bit B Counter												6-Bit A Counter						Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P17	P16	P15	P14	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

P15	P14	Prescaler Value
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

P16	RF Power Down
0	Disabled
1	Enabled

A6	A5	.....	A2	A1	A Counter Divide Ratio
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
0	0	.....	0	0	4
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	60
1	1	.....	0	1	61
1	1	.....	1	0	62
1	1	.....	1	1	63

B12	B11	B10	.....	B3	B2	B1	B Counter Divide Ratio
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	4092
1	1	1	.....	1	0	1	4093
1	1	1	.....	1	1	0	4094
1	1	1	.....	1	1	1	4095

P17	RF CP Gain
0	Disabled
1	Enabled

N = BP + A, P is prescaler value set in the Function Latch
B must be greater than or equal to A
For contiguous values of , N_{MIN} is $(P^2 - P)$

PROGRAM MODES

Table 3 and Table 5 show how to set up the Program Modes in the ADF4210 family. The following should be noted:

1. IF and RF Analog Lock Detect indicate when the PLL is in lock. When the loop is locked and either IF or RFAnalog Lock Detect is selected, then the MUXOUT pin will show a logic high with narrow low-going pulses. When the IF/RF Analog Lock Detect is chosen then the locked condition is indicated only when both IF and RF loops are locked.
2. The IF Counter Reset mode resets the R and N counters in the IF section and also puts the IF charge pump into 3-state. The RF Counter Reset mode resets the R and N counters in the RF section and also puts the RF charge pump into 3-state. The IF and RF Counter Reset mode does both of the above. Upon removal of the reset bits, the N counter resumes counting in close alignment with the R counter (maximum error is one prescaler output cycle).
3. The Fastlock mode uses MUXOUT to switch a second loop filter damping resistor to ground during Fastlock operation. Activation of Fastlock occurs whenever RF CP Gain in the RF Reference counter is set to one.

IF Power Down

It is possible to program the ADF4210 family for either synchronous or asynchronous powerdown on either the IF or RF side.

Synchronous IF Power Down.

Programming a “1” to P7 of the ADF4216 family will initiate a power down. If P2 of the ADF4216 family has been set to “0” (normal operation), then a synchronous power down is conducted. The device will automatically put the charge pump into 3-state and then complete the power down.

Asynchronous IF Power Down

If P2 of the ADF4210 family has been set to “1” (3-state the IF charge pump), and P7 is subsequently set to “1”, then an asynchronous power down is conducted. The device will go into power down on the rising edge of LE which latches the “1” to the IF Power Down bit (P7).

Synchronous RF Power Down.

Programming a “1” to P16 of the ADF4210 family will ini-tiate a power down. If P10 of the ADF4210 family has been set to “0” (normal operation), then a synchronous power down is conducted. The device will automatically put the charge pump into 3-state and then complete the power down.

Asynchronous RF Power Down

If P10 of the ADF4210 families has been set to “1” (3-state the RF charge pump), and P16 is subsequently set to “1”, then an asynchronous power down is conducted. The device will go into power down on the rising edge of LE which latches the “1” to the RF Power Down bit (P16).

Activation of either synchronous or asynchronous powerdown forces the IF/RF loop's R and N dividers to their load state conditions and the IF/RF input section is debiased to a high impedance state

The REF oscillator circuit is only disabled if both the IF and RF Powerdowns are set.

The RF section of the devicewill return to normal powered-up operation immediately on LE latching a "0" to the RF powerdown bit (P16). See Table 6.

The REFIN oscillator circuit is only disabled if both the IF and RF Power Downs are set.
The input register and latches remain active and are capable of loading and latching data during all the power down modes.
The IF/RF section of the devices will return to normal powered-up operation immediately upon LE latching a “0” to the appropriate Power Down bit.

IF SECTION:

PROGRAMMABLE IF REFERENCE (R) COUNTER

If control bits C2, C1 are 0,0 then the data is transferred from the input shift register to the 14 Bit IFR counter. Table 3 shows the input shift register data format for the IFR counter and the divide ratios possible.

IF Phase Detector Polarity
P1 sets the IF Phase Detector Polarity. When the IF VCO characteristics are positive this should be set to "1". When they are negative it should be set to "0". See Table 3.

IF Charge Pump 3-State
P2 puts the IF charge pump into 3-state mode when programmed to a "1". It should be set to "0" for normal operation. See Table 3.

IF PROGRAM MODES
Table 3 and Table 5 show how to set up the Program Modes in the ADF4210 family. See page 13 for functional description.

IF Charge Pump Currents
IFCP2, IFCP1, IFCP0 program Current Setting for the IF charge pump. See Table 3.

PROGRAMMABLE IF N COUNTER

If control bits C2, C1 are 0, 1 then the data in the input register is used to program the IFN (A + B) counter. The N counter consists of a 6-bit swallow counter (A counter) and 12-bit programmable counter (B counter). Table 4 shows the input register data format for programming the IF N counter and the divide ratios possible.

IF Prescaler Value
P5 and P6 in the IF A,B Counter Latch set the IF prescaler values. See Table 4.

IF Power Down
Table 3 and Table 5 show the powerdown bits in the ADF4210 family. See page 13 for functional description.

IF Fastlock
The IF CP Gain bit (P8) of the IF N register in the ADF4210 family is the Fastlock Enable Bit. Only when this is "1" is IF Fastlock enabled. When Fastlock is enabled, the IF CP current is set to it's maximum value. Also an extra loop filter damping resistor to ground is switched in using the FL_O pin. thus compensating for the change in loop characteristics while in Fastlock. Since the IF CP Gain bit is contained in the IF N Counter, only one write is needed to both program a new output frequency and also initiate Fastlock. To come out of fastlock, the IF CP Gain bit on the IF N register must be set to "0". See Table 4.

RF SECTION:

PROGRAMMABLE RF REFERENCE (R) COUNTER

If control bits C2, C1 are 1,0 then the data is transferred from the input shift register to the 14 Bit RFR counter. Table 5 shows the input shift register data format for the RFR counter and the divide ratios possible.

RF Phase Detector Polarity
P9 sets the IF Phase Detector Polarity. When the RF VCO characteristics are positive this should be set to "1". When they are negative it should be set to "0". See Table 5.

RF Charge Pump 3-State
P10 puts the RF charge pump into 3-state mode when programmed to a "1". It should be set to "0" for normal operation. See Table 5.

RF PROGRAM MODES
Table 3 and Table 5 show how to set up the Program Modes in the ADF4210 family. See page 13 for functional description.

RF Charge Pump Currents
RFCP2, RFCP1, RFCP0 program Current Setting for the RF charge pump. See Table 5.

PROGRAMMABLE RF N COUNTER

If control bits C2, C1 are 1, 1 then the data in the input register is used to program the RF N (A + B) counter. The N counter consists of a 6-bit swallow counter (A counter) and 12-bit programmable counter (B counter). Table 4 shows the input register data format for programming the RF N counter and the divide ratios possible. See Table 6.

RF Prescaler Value
P14 and P15 in the RF A,B Counter Latch set the RF prescaler values. See Table 6.

RF Power Down
Table 3 and Table 5 show the powerdown bits in the ADF4210 family. See page 13 for functional description.

RF Fastlock
The RF CP Gain bit (P17) of the RF N register in the ADF4210 family is the Fastlock Enable Bit. Only when this is "1" is IF Fastlock enabled. When Fastlock is enabled, the RF CP current is set to it's maximum value. Also an extra loop filter damping resistor to ground is switched in using the FL_O pin. thus compensating for the change in loop characteristics while in Fastlock. Since the RF CP Gain bit is contained in the RF N Counter, only one write is needed to both program a new output frequency and also initiate Fastlock. To come out of fastlock, the RF CP Gain bit on the RF N register must be set to "0". See Table 6.