PLL Frequency Synthesizer

Preliminary Technical Data — ADF4110/ADF4111/ADF4112/ADF4113

FEATURES

ADF4110: 550 MHz
ADF4111: 1.2 GHz
ADF4112: 2.8 GHz
ADF4113: 3.7GHz
+2.7 V to +5.5 V Power Supply
Separate V_P Allows Extended Tuning Voltage in 3V Systems
Programmable Dual Modulus Prescaler 8/9, 16/17, 32/33, 64/65
Programmable Charge Pump Currents
Programmable Anti-Backlash Pulse Width
3-Wire Serial Interface
Digital Lock Detect
Power Down Mode

APPLICATIONS

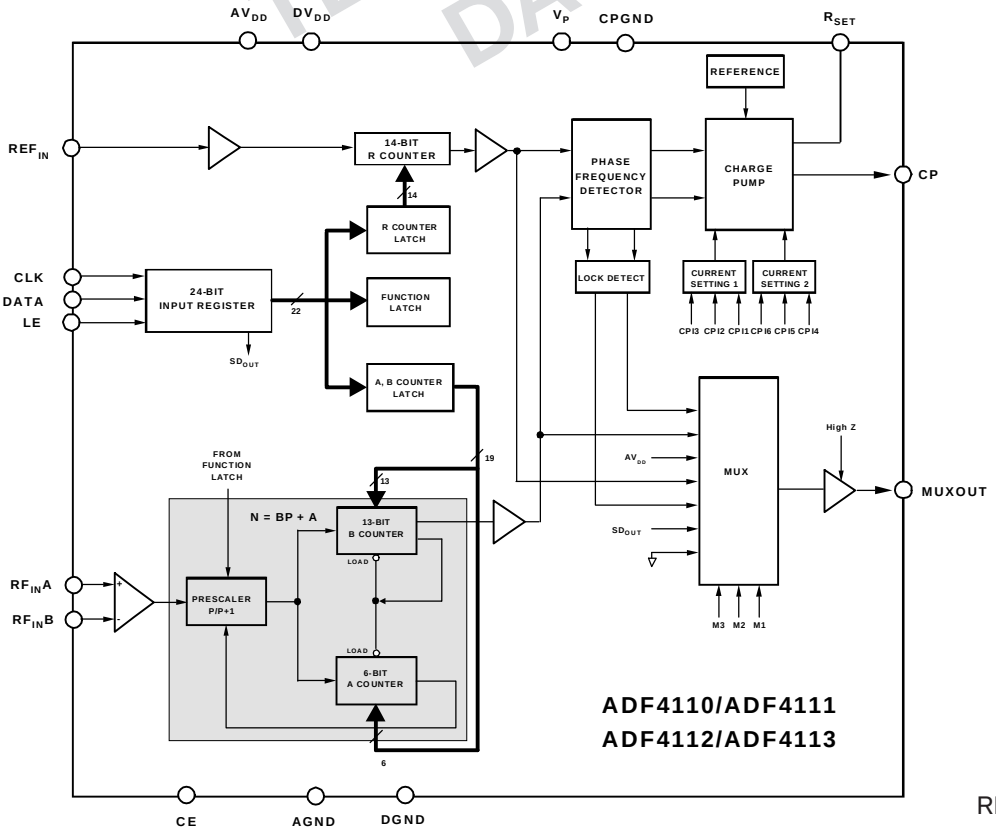
Base Stations for Wireless Radio (GSM, PCS, DCS, WCDMA)
Wireless Handsets (GSM, PCS, DCS, WCDMA)
Wireless LANS
Communications Test Equipment
CATV Equipment

GENERAL DESCRIPTION

The ADF4110 family of frequency synthesizers can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. They consist of a low-noise digital PFD (Phase Frequency Detector), a precision charge pump, a programmable reference divider, programmable A and B counters and a dual-modulus prescaler (P/P+1). The A (6-bit) and B (13-bit) counters, in conjunction with the dual modulus prescaler (P/P+1), implement an N divider (N= BP+A). In addition, the 14-bit reference counter (R Counter), allows selectable REFIN frequencies at the PFD input. A complete PLL (Phase-Locked Loop) can be implemented if the synthesizer is used with an external loop filter and VCO (Voltage Controlled Oscillator)

Control of all the on-chip registers is via a simple 3-wire interface. The devices operate with a power supply ranging from 2.7V to 5.5V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM



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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781-329-4700 **Fax: 781-326-8703**

ADF4110/11/12/13 – SPECIFICATIONS[1] (AV_{DD} = DV_{DD} = +3 V ± 10%, +5 V ± 10%; V_P = AV_{DD}, +5 V ± 10%; GND = 0 V; R_{SET} = 4.7kΩ; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	B Version	BChips[2] (Typical)	Units	Test Conditions/Comments
RF CHARACTERISTICS				
RF Input Frequency				See Figure 3 for input circuit.
ADF4110	25/550	25/550	MHz min/max	
ADF4111	0.1/1.2	0.1/1.2	GHz min/max	
ADF4112	0.1/2.8	0.1/2.8	GHz min/max	
ADF4113	0.2/3.7	0.2/3.7	GHz min/max	
Reference Input Frequency	0/150	0/150	MHz min/max	
Maximum Allowable Prescaler Output Frequency[3]	250/200	250/200	MHz typ/max	
Phase Detector Frequency[4]	55	55	MHz max	
RF Input Sensitivity	-15/0	-15/0	dBm min/max	AV_{DD} = 3V
	-10/0	-10/0	dBm min/max	AV_{DD} = 5V
Reference Input Sensitivity	-5	-5	dBm min	ac coupled. Max when dc coupled: 0 to V_{DD} (CMOS compatible)
CHARGE PUMP				
I_{CP} sink/source				Programmable: See Table 5
High Value	5	5	mA typ	With R_{SET} = 4.7kΩ
Low Value	625	625	µA typ	
Absolute Accuracy	2	2	% typ	With R_{SET} = 4.7kΩ
	5	5	% max	
R_{SET} Range	2.7/10	2.7/10	kΩ typ	See Table 5
I_{CP} 3-State Leakage Current	1	1	nA max	See Figure 28
Sink and Source Current Matching	2	2	% typ	0.5V < V_{CP} < V_P - 0.5
I_{CP} vs. V_{CP}	2	2	% typ	0.5V < V_{CP} < V_P - 0.5
I_{CP} vs. Temperature	2	2	% typ	V_{CP} = V_P/2
LOGIC INPUTS				
V_{INH}, Input High Voltage	0.8 x DV_{DD}	0.8 x DV_{DD}	V min	
V_{INL}, Input Low Voltage	0.2 x DV_{DD}	0.2 x DV_{DD}	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
Reference Input Current	±100	±100	µA max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	DV_{DD} - 0.4	DV_{DD} - 0.4	V min	I_{OH} = 1mA
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 1mA
POWER SUPPLIES				
AV_{DD}	2.7/5.5	2.7/5.5	V min/V max	
DV_{DD}	AV_{DD}	AV_{DD}		
V_P	AV_{DD}/6.0	AV_{DD}/6.0	V min/V max	
I_{DD}[5] (AI_{DD} + DI_{DD})				See Figures 26 and 27
ADF4110	2.7	2.7	mA max	2.2mA typical
ADF4111	4.2	4.2	mA max	3.5mA typical
ADF4112	6.5	6.5	mA max	5.3mA typical
ADF4113	10	10	mA max	8.5mA typical
Low Power Sleep Mode	1	1	µA typ	

NOTES
1. Operating temperature range is as follows: B Version: –40°C to +85°C.
2. The BChip specifications are given as typical values.
3. This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency which is less than this value.
4. Guaranteed by design. Sample tested to ensure compliance.
5. AV_{DD} = DV_{DD} = 3V; P = 16; SYNC = 0; DLY = 0; RF_{IN} for ADF4110 = 540MHz; RF_{IN} for ADF4111, ADF4112, ADF4113 = 900MHz.

ADF4110/11/12/13 – SPECIFICATIONS[1]

(AV_{DD} = DV_{DD} = +3 V ± 10%, +5 V ± 10%; V_P = AV_{DD}, +5 V ± 10%; GND = 0 V; R_{SET} = 4.7kΩ; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	B Version	BChips	Units	Test Conditions/Comments
NOISE CHARACTERISTICS				
Phase Noise Floor[2]	-171	-171	dBc/Hz typ	@ 25kHz PFD Frequency
	-164	-164	dBc/Hz typ	@ 200kHz PFD Frequency
Phase Noise Performance[3]				@ VCO Output
ADF4110[4]	-96	-96	dBc/Hz typ	
ADF4111[5]	-89	-89	dBc/Hz typ	
ADF4112[5]	-90	-90	dBc/Hz typ	
ADF4113[5]	-91	-91	dBc/Hz typ	
ADF4111[6]	-81	-81	dBc/Hz typ	
ADF4112[7]	-86	-86	dBc/Hz typ	
ADF4112[8]	-66	-66	dBc/Hz typ	
ADF4112[9]	-84	-84	dBc/Hz typ	
ADF4113[9]	-85	-85	dBc/Hz typ	
ADF4113[10]	-85	-85	dBc/Hz typ	
Spurious Signals				Measured at offset of $f_{PFD}/2f_{PFD}$
ADF4110[4]	-80/-84	-80/-84	dBc typ	
ADF4111[5]	-80/-84	-80/-84	dBc typ	
ADF4112[5]	-80/-84	-80/-84	dBc typ	
ADF4113[5]	-80/-84	-80/-84	dBc typ	
ADF4111[6]	-80/-84	-80/-84	dBc typ	
ADF4112[7]	-80/-82	-80/-82	dBc typ	
ADF4112[8]	-78/-82	-78/-82	dBc typ	
ADF4112[9]	-78/-82	-78/-82	dBc typ	
ADF4113[9]	-78/-82	-78/-82	dBc typ	
ADF4113[10]	-78/-82	-78/-82	dBc typ	

NOTES

1. Operating temperature range is as follows: B Version: –40°C to +85°C.
2. The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where N is the N divider value).
3. The phase noise is measured with the EVAL-ADF411XEB Evaluation Board and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer (f_{REFOUT} = 10MHz @ 0dBm). SYNC = 0; DLY = 0 (See Table 3).
4. f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 540MHz; N = 2700; Loop B/W = 20kHz
5. f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 900MHz; N = 4500; Loop B/W = 20kHz
6. f_{REFIN} = 10 MHz; f_{PFD} = 30kHz; Offset frequency = 300 Hz; f_{RF} = 836MHz; N = 27867; Loop B/W = 3kHz
7. f_{REFIN} = 10 MHz; f_{PFD} = 200kHz; Offset frequency = 1 kHz; f_{RF} = 1750MHz; N = 8750; Loop B/W = 20kHz
8. f_{REFIN} = 10 MHz; f_{PFD} = 10kHz; Offset frequency = 200 Hz; f_{RF} = 1750MHz; N = 175000; Loop B/W = 1kHz
9. f_{REFIN} = 10 MHz; f_{PFD} = 200kHz; Offset frequency = 1 kHz; f_{RF} = 1960MHz; N = 9800; Loop B/W = 20kHz
10. f_{REFIN} = 10 MHz; f_{PFD} = 1MHz; Offset frequency = 1 kHz; f_{RF} = 3100MHz; N = 3100; Loop B/W = 20kHz

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADF4110BRU	–40°C to +85°C	RU-16
ADF4110BCP	–40°C to +85°C	CP-24
ADF4111BRU	–40°C to +85°C	RU-16
ADF4111BCP	–40°C to +85°C	CP-24
ADF4112BRU	–40°C to +85°C	RU-16
ADF4112BCP	–40°C to +85°C	CP-24
ADF4113BRU	–40°C to +85°C	RU-16
ADF4113BCP	–40°C to +85°C	CP-24

* RU = Thin Shrink Small Outline Package (TSSOP)
CP = Chip Scale Package
Contact the factory for chip availability

TIMING CHARACTERISTICS (V_{DD} = +5 V 10%, +3 V ± 10%; GND = 0 V, unless otherwise noted)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Units	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK Set Up Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	25	ns min	CLOCK High Duration
t_4	25	ns min	CLOCK Low Duration
t_5	10	ns min	CLOCK to LE Set Up Time
t_6	20	ns min	LE Pulse Width

NOTE
Guaranteed by Design but not Production Tested.

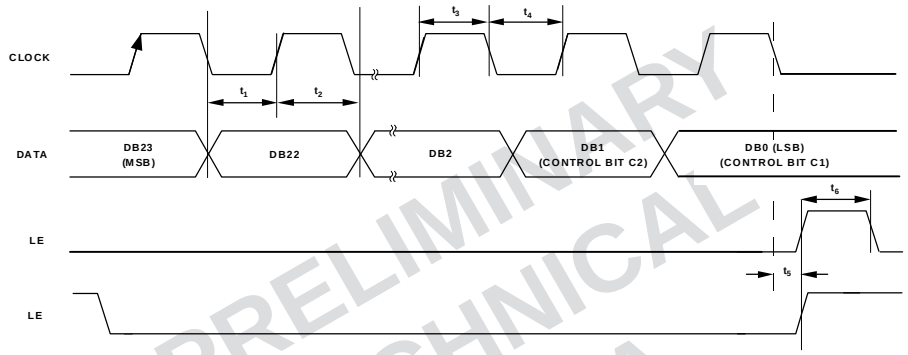


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

AV_{DD} to GND . . . . . –0.3 V to +7 V
AV_{DD} to DV_{DD} . . . . . –0.3 V to +0.3 V
V_P to AGND . . . . . –0.3 V to +7 V
V_P to AV_{DD} . . . . . –0.3 V to +5.5 V
Digital I/O Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND . . . . . –0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$ to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . +150°C
TSSOP θ_{JA} Thermal Impedance . . . . . 150.4°C/W
CSP θ_{JA} Thermal Impedance . . . . . TBD°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This device is a high-performance RF integrated circuit with an ESD rating of < 2kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

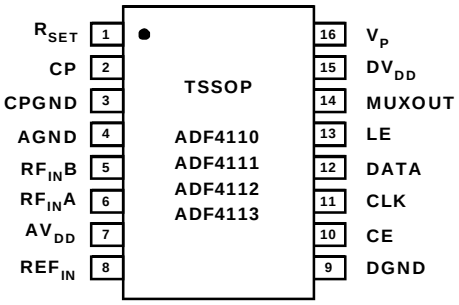
PIN DESCRIPTION

Mnemonic	Function
R_{SET}	Connecting a resistor between this pin and ground sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.66V. The relationship between I_{CP} and R_{SET} is $$I_{CP\max} = \frac{23.5}{R_{SET}}$$ So, with R_{SET} = 4.7kΩ, I_{CPmax} = 5mA.
CP	Charge Pump Output. This is normally connected to a loop filter which drives the input to an external VCO.
CPGND	Charge Pump Ground
AGND	Analog Ground
$RF_{IN}B$	Complementary Input to the RF Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor.
$RF_{IN}A$	Input to the RF Prescaler. This small signal input is normally ac coupled from the VCO.
AV_{DD}	Analog Power Supply. This may range from 2.7V to 5.5V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV_{DD} must be the same value as DV_{DD}
REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of V_{DD}/2 and an equivalent input resistance of 100kΩ. See Figure 2. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac coupled.
DGND	Digital Ground.
CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking the pin high will power up the device depending on the status of the power-down bit F2.
CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
MUXOUT[1]	This multiplexer output allows either the Lock Detect, the scaled RF or the scaled Reference Frequency to be accessed externally.
DV_{DD}	Digital Power Supply. This may range from 2.7V to 5.5V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} must be the same value as AV_{DD}.
V_P	Charge Pump Power Supply. This should be greater than or equal to V_{DD}. In systems where V_{DD} is 3V, it can be set to 5V and used to drive a VCO with a tuning range of up to 5V.

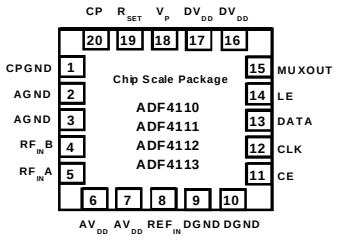
NOTES
1. MUXOUT is also used for Test Modes on the devices. These Test Modes will be detailed in TNXXX available from Analog Devices Inc.

PIN CONFIGURATIONS

TOP VIEW



TOP VIEW



TRANSISTOR COUNT: 6425 (CMOS) and 303 (Bipolar).

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The Reference Input stage is shown below in Figure 2. SW1 and SW2 are normally-closed switches. SW3 is normally-

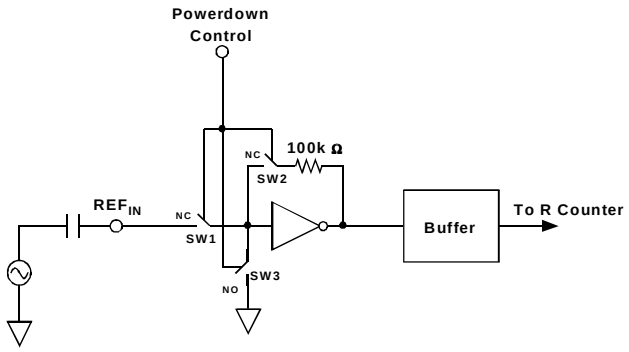


Figure 2. Reference Input Stage

open. When Powerdown is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on powerdown.

RF INPUT STAGE

The RF input stage is shown in Figure 3. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

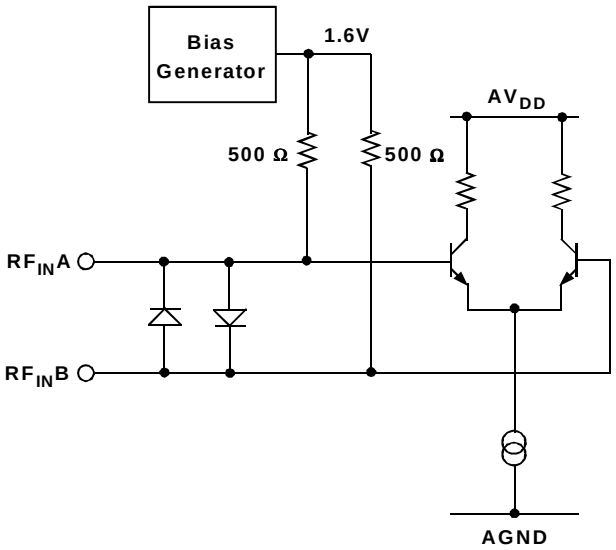


Figure 3. RF Input Stage

PRESCALER

The dual-modulus prescaler takes the CML clock from the RF input stage and divides it down to a manageable frequency for the CMOS A and B counters. The prescaler is programmable. It can be set in software to 8/9, 16/17, 32/33 or 64/65. It is based on a synchronous 4/5 core.

A AND B COUNTERS

The A and B CMOS counters combine with the dual modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The devices are guarenteed to work with a prescaler when the prescaler output is 200MHz or less. Typically they will work with 250MHz output from the prescaler. Thus, with an RF input frequency of 2.5GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

Pulse Swallow Function

The A and B counters, in conjunction with the dual modulus prescaler make it possible to generate output frequencies which are spaced only by the Reference Frequency divided by R . The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times f_{REFIN}/R$$

f_{VCO}: Ouput Frequency of external voltage controlled oscillator (VCO).

P: Preset modulus of dual modulus prescaler.

B: Preset Divide Ratio of binary 13-bit counter (1 to 8191).

A: Preset Divide Ratio of binary 6-bit swallow counter (0 to 63).

f_{REFIN}: Ouput frequency of the external reference frequency oscillator.

R: Preset divide ratio of binary 14-bit programmable reference counter (1 to 16383).

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the input clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

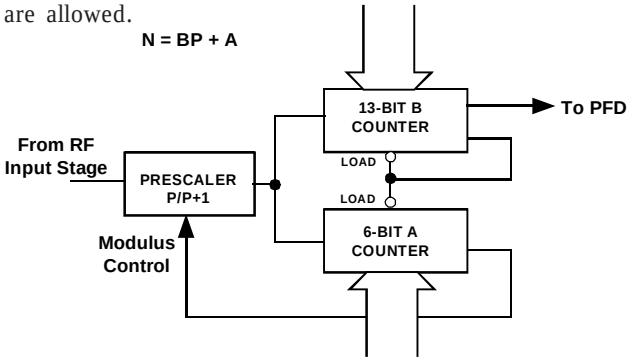


Figure 4. A and B Counters

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 5 is a simplified schematic. The PFD includes a programmable delay element which

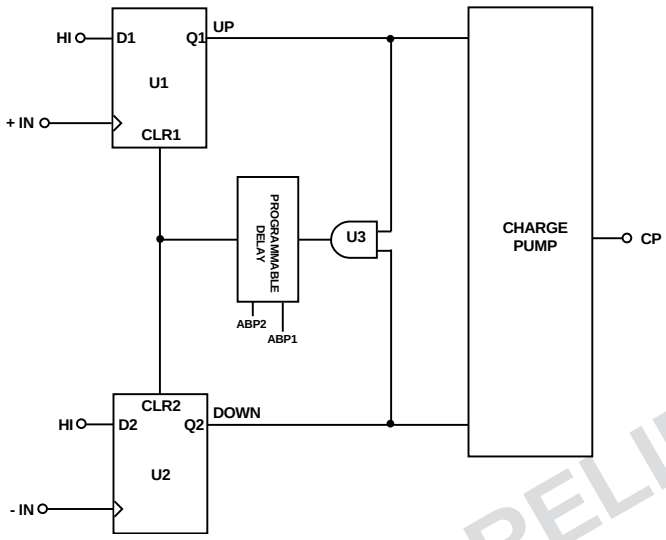


Figure 5. PFD Simplified Schematic

controls the width of the anti-backlash pulse. This pulse ensures that there is no deadzone in the PFD transfer function and gives a consistent reference spur level. Two bits in the Reference Counter Latch, ABP2 and ABP1 control the width of the pulse. See Table 3.

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4110 family allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2 and M1 in the Function Latch. Table 5 shows the full truth table. Figure 6 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for two types of lock detect: Digital Lock Detect and Analog Lock Detect

Digital Lock Detect is active high. It is set high when the phase error on three consecutive Phase Detector cycles is less than 15ns. It will stay set high until a phase error of greater than 25ns is detected on any subsequent PD cycle.

The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10k nominal. When lock has been detected it is high with narrow low-going pulses .

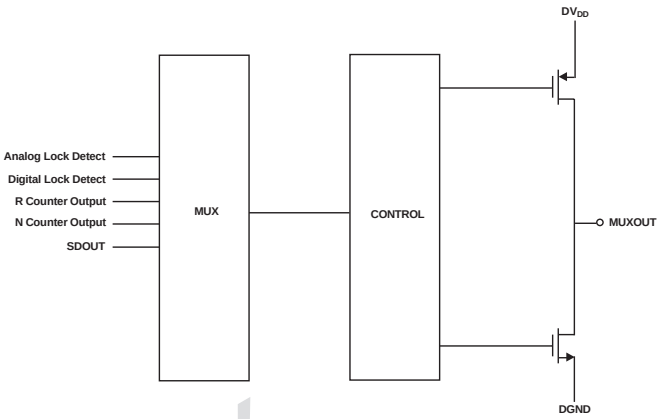


Figure 6. MUXOUT Circuit

INPUT SHIFT REGISTER

The ADF4110 family digital section includes a 24-bit input shift register, a 14-bit R counter and a 19-bit N counter, comprising a 6-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two lsb's DB1, DB0 as shown in the timing diagram of Figure 1. The truth table for these bits is shown in Table 6. Table 1 shows a summary of how the latches are programmed.

Table 1. C2, C1 Truth Table

Control Bits C2	Control Bits C1	Data Latch
0	0	R Counter
0	1	N Counter (A and B)
1	0	Function Latch
1	1	Initialization Latch

Table 2. ADF4110 Family Latch Summary

Reference Counter Latch

Reserved	DLY	SYNC	Lock Detect Precision	Test Mode Bits		Anti Backlash Width		14-Bit Reference Counter														Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	DLY	SYNC	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

N Counter Latch

Reserved		CP Gain	13-Bit B Counter												6-Bit A Counter						Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

Function Latch

Prescaler Value		Power Down 2	Current Setting 2			Current Setting 1			Timer Counter Control				FastLock Mode	Fastlock Enable	CP 3-State	PD Polarity	MUXOUT Control			Power Down 1	Counter Reset	Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

Initialisation Latch

Prescaler Value		Power Down 2	Current Setting 2			Current Setting 1			Timer Counter Control				FastLock Mode	Fastlock Enable	CP 3-State	PD Polarity	MUXOUT Control			Power Down 1	Counter Reset	Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

REFERENCE COUNTER LATCH

Table 3. Reference Counter Latch Map

Reserved	DLY	SYNC	Lock Detec Precision	Test Mode Bits		Anti Backlash Width		14-Bit Reference Counter												Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	DLY	SYNC	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

R14	R13	R12	.....	R3	R2	R1	Divide Ratio
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	16 80
1	1	1	.....	1	0	1	16 81
1	1	1	.....	1	1	0	16 82
1	1	1	.....	1	1	1	16 83

ABP2	ABP1	Anti-Backlash Pulse Width
0	0	2.9ns
0	1	1.3ns
1	0	6.0ns
1	1	2.9ns

Test Mode Bits shoul be set to 00 for Normal Operation

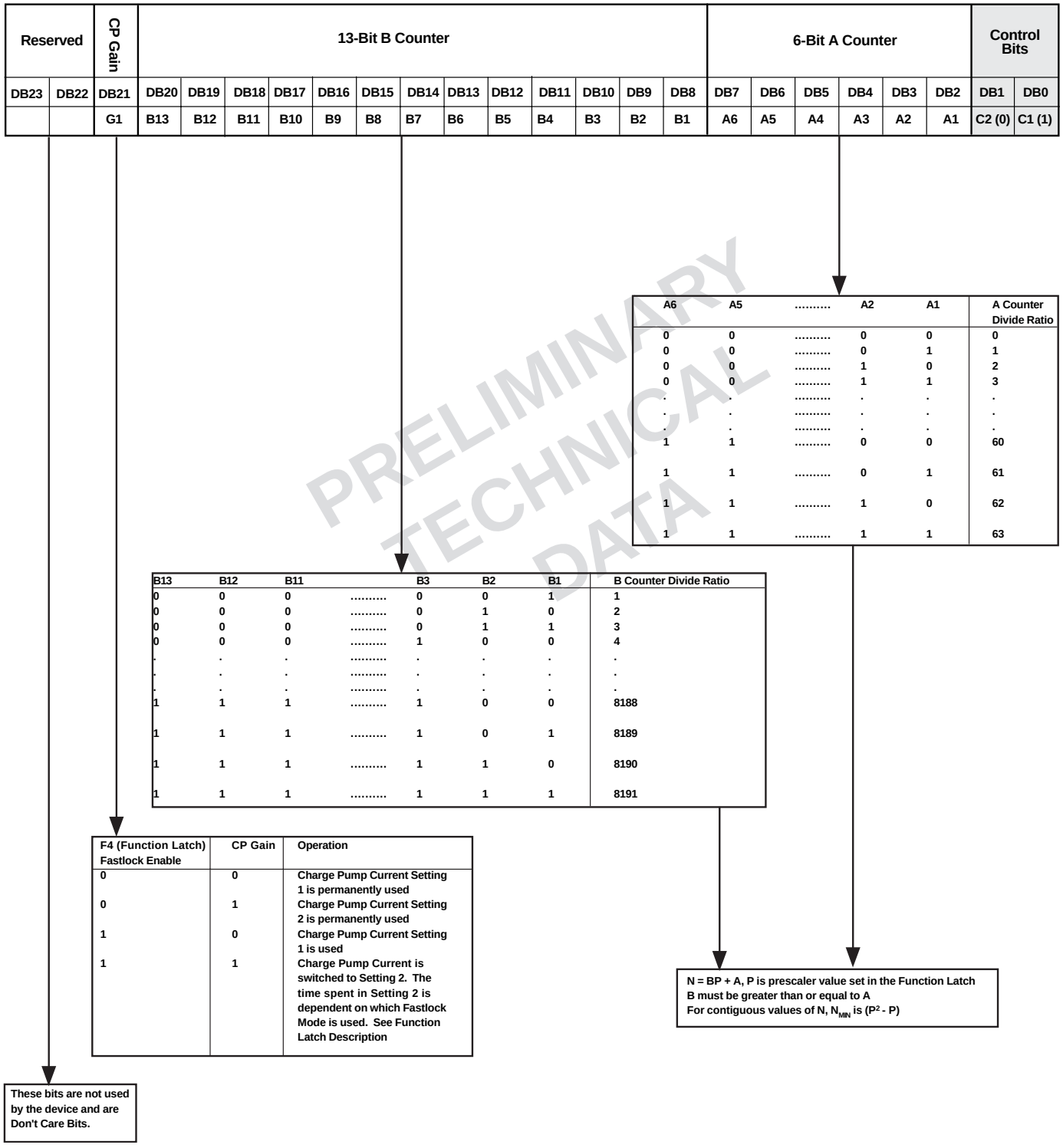
LDP	Operation
0	3 consecutive cycles of hase delay less tha 15ns must occur before lock detect is set.
1	5 consecutive cycles of hase delay less tha 15ns must occur before lock detect is set.

DLY	SYNC	Operation
0	0	Normal Operation
0	1	Output of Prescaler is Resynchronize with non-delayed versi on of RF Input.
1	0	Normal Operation
1	1	Output of Prescaler is Resynchronize with delayed version of RF Input.

N COUNTER LATCH

Table 4. N Counter Latch Map

Reserved		CP Gain	13-Bit B Counter													6-Bit A Counter						Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)



A6	A5	.....	A2	A1	A Counter Divide Ratio
0	0	.....	0	0	0
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	60
1	1	.....	0	1	61
1	1	.....	1	0	62
1	1	.....	1	1	63

B13	B12	B11	.....	B3	B2	B1	B Counter Divide Ratio
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	8188
1	1	1	.....	1	0	1	8189
1	1	1	.....	1	1	0	8190
1	1	1	.....	1	1	1	8191

F4 (Function Latch) Fastlock Enable	CP Gain	Operation
0	0	Charge Pump Current Setting 1 is permanently used
0	1	Charge Pump Current Setting 2 is permanently used
1	0	Charge Pump Current Setting 1 is used
1	1	Charge Pump Current is switched to Setting 2. The time spent in Setting 2 is dependent on which Fastlock Mode is used. See Function Latch Description

N = BP + A, P is prescaler value set in the Function Latch
B must be greater than or equal to A
For contiguous values of N, N_{MIN} is $(P^2 - P)$

These bits are not used by the device and are Don't Care Bits.

FUNCTION LATCH

Table 5. Function Latch Map

Prescaler Value		Power Down 2	Current Setting 2			Current Setting 1			Timer Counter Control				FastLock Mode	Fastlock Enable	CP 3-State	PD Polarity	MUXOUT Control			Power Down 1	Counter Reset	Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

F1	Counter Operation
0	Normal
1	R, A, B Counters Held in Reset

F2	PD Polarity
0	Negative
1	Positive

F3	Charge Pump Output
0	Normal
1	3-State

F4	F5	Fastlock Mode
0	X	Fastlock Disabled
1	0	Fastlock Mode 1
1	1	Fastlock Mode 2

TC4	TC3	TC2	TC1	Timeout (PFD Cycles)
0	0	0	0	3
0	0	0	1	7
0	0	1	0	11
0	0	1	1	15
0	1	0	0	19
0	1	0	1	23
0	1	1	0	27
0	1	1	1	31
1	0	0	0	35
1	0	0	1	39
1	0	1	0	43
1	0	1	1	47
1	1	0	0	51
1	1	0	1	55
1	1	1	0	59
1	1	1	1	63

M3	M2	M1	Output
0	0	0	3-State Output
0	0	1	Digital Lock Detect (Active High)
0	1	0	N Divider Output
0	1	1	DV_{DD}
1	0	0	R Divider Output
1	0	1	N-Channel Open-Drain Lock Detect
1	1	0	Serial Data Output
1	1	1	DGND

CPI6	CPI5	CP14	I_{CP} (mA)		
CPI3	CPI2	CPI1	2.7kΩ	4.7kΩ	10kΩ
0	0	0	1.088	0.625	0.294
0	0	1	2.176	1.25	0.588
0	1	0	3.264	1.875	0.882
0	1	1	4.352	2.5	1.176
1	0	0	5.44	3.125	1.47
1	0	1	6.528	3.75	1.764
1	1	0	7.616	4.375	2.058
1	1	1	8.704	5.0	2.352

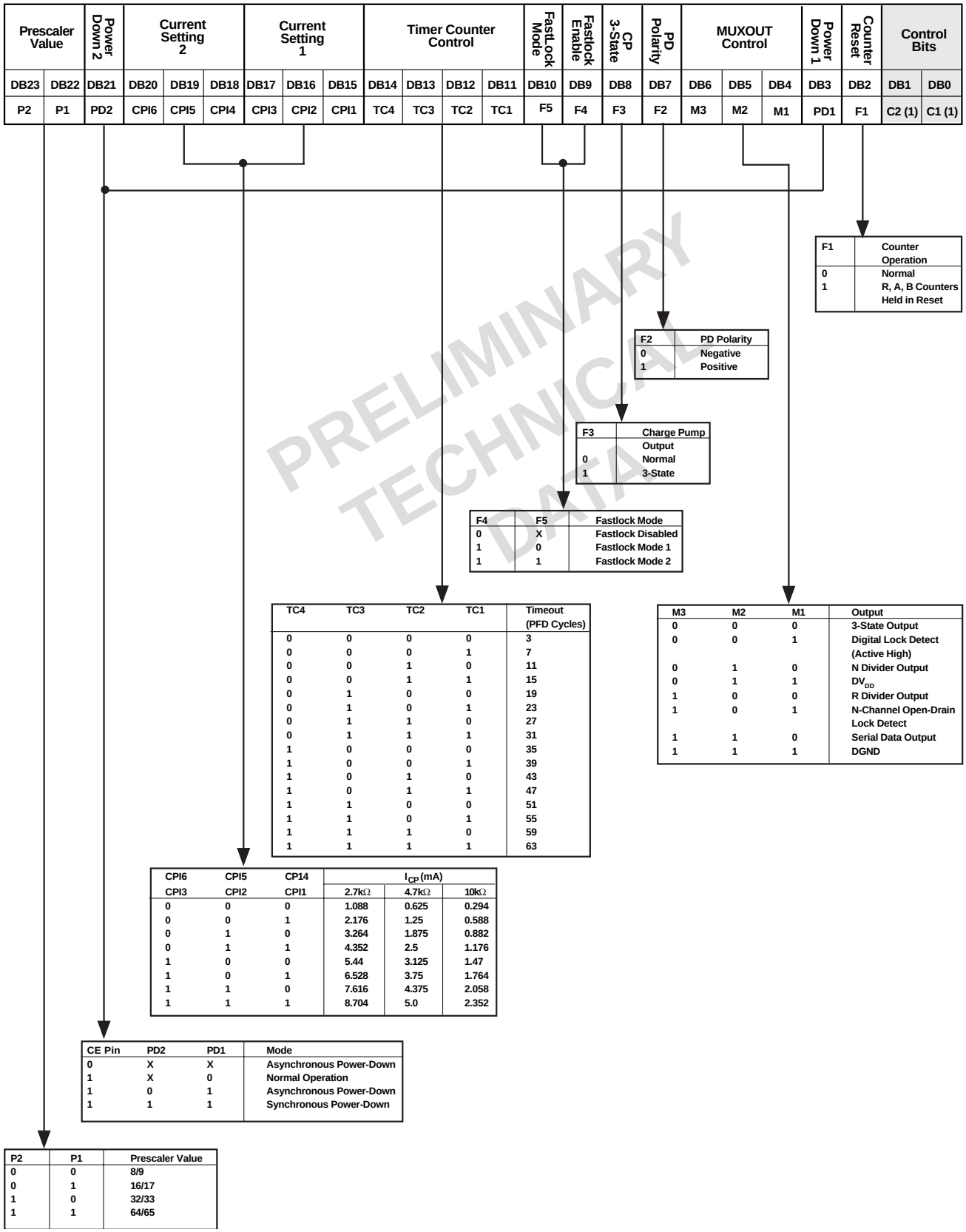
CE Pin	PD2	PD1	Mode
0	X	X	Asynchronous Power-Down
1	X	0	Normal Operation
1	0	1	Asynchronous Power-Down
1	1	1	Synchronous Power-Down

P2	P1	Prescaler Value
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

INITIALIZATION LATCH

Table 6. Initialization Latch Map

Prescaler Value		Power Down 2	Current Setting 2			Current Setting 1			Timer Counter Control				FastLock Mode	FastLock Enable	CP 3-State	PD Polarity	MUXOUT Control			Power Down 1	Counter Reset	Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)



F1	Counter Operation
0	Normal
1	R, A, B Counters Held in Reset

F2	PD Polarity
0	Negative
1	Positive

F3	Charge Pump Output
0	Normal
1	3-State

F4	F5	Fastlock Mode
0	X	Fastlock Disabled
1	0	Fastlock Mode 1
1	1	Fastlock Mode 2

TC4	TC3	TC2	TC1	Timeout (PFD Cycles)
0	0	0	0	3
0	0	0	1	7
0	0	1	0	11
0	0	1	1	15
0	1	0	0	19
0	1	0	1	23
0	1	1	0	27
0	1	1	1	31
1	0	0	0	35
1	0	0	1	39
1	0	1	0	43
1	0	1	1	47
1	1	0	0	51
1	1	0	1	55
1	1	1	0	59
1	1	1	1	63

M3	M2	M1	Output
0	0	0	3-State Output
0	0	1	Digital Lock Detect (Active High)
0	1	0	N Divider Output
0	1	1	DV_{DD}
1	0	0	R Divider Output
1	0	1	N-Channel Open-Drain Lock Detect
1	1	0	Serial Data Output
1	1	1	DGND

CPI6 CPI3	CPI5 CPI2	CP14 CPI1	I_{CP} (mA) 2.7kΩ	4.7kΩ	10kΩ
0	0	0	1.088	0.625	0.294
0	0	1	2.176	1.25	0.588
0	1	0	3.264	1.875	0.882
0	1	1	4.352	2.5	1.176
1	0	0	5.44	3.125	1.47
1	0	1	6.528	3.75	1.764
1	1	0	7.616	4.375	2.058
1	1	1	8.704	5.0	2.352

CE Pin	PD2	PD1	Mode
0	X	X	Asynchronous Power-Down
1	X	0	Normal Operation
1	0	1	Asynchronous Power-Down
1	1	1	Synchronous Power-Down

P2	P1	Prescaler Value
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

THE FUNCTION LATCH

With C2, C1 set to 1,0, the on-chip function latch will be programmed. Table 5 shows the input data format for programming the Function Latch.

Counter Reset

DB2 (F1) is the counter reset bit. When this is "1", the R counter and the A,B counters are reset. For normal operation this bit should be "0". *Upon powering up, the F1 bit needs to be disabled, the N counter resumes counting in "close" alignment with the R counter. (The maximum error is one prescaler cycle).*

Power Down

DB3 (PD1) and DB21 (PD2) on the ADF4110 Family, provide programmable power-down modes. They are enabled by the CE pin .

When the CE pin is low, the device is immediately disabled regardless of the states of PD2, PD1.

In the programmed asynchronous power-down, the device powers down immediately after latching a "1" into bit PD1, with the condition that PD2 has been loaded with a "0".

In the programmed synchronous power-down, the device power down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing a "1" into bit PD1 (on condition that a "1" has also been loaded to PD2), then the device will go into power-down after the first successive charge pump event.

When a power down is activated (either synchronous or asynchronous mode including CE-pin-activated power down), the following events occur:

All active DC current paths are removed.

The R, N and timeout counters are forced to their load state conditions.

The charge pump is forced into three-state mode.

The digital clock detect circuitry is reset.

The RF_{IN} input is debiased.

The oscillator input buffer circuitry is disabled.

The input register remains active and capable of loading and latching data.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, M1 on the ADF4110 Family. Table 5 shows the truth table.

Fastlock Enable Bit

DB9 of the Function Latch is the Fastlock Enable Bit. Only when this is "1" is Fastlock enabled.

Fastlock Mode Bit

DB10 of the Function Latch is the Fastlock Mode bit. When Fastlock is enabled, this bit determines which Fastlock Mode is used. If the Fastlock Mode bit is "0" then Fastlock Mode 1 is selected and if the Fastlock Mode bit is "1", then Fastlock Mode 2 is selected.

Fastlock Mode 1

The charge pump current is switched to the contents of Current Setting 2.
The device enters Fastlock by having a "1" written to the CP Gain bit in the N counter latch. The device exits Fastlock by having a "0" written to the CP Gain bit in the N counter latch.

Fastlock Mode 2

The charge pump current is switched to the contents of Current Setting 2.
The device enters Fastlock by having a "1" written to the CP Gain bit in the N counter latch. The device exits Fastlock under the control of the Timer Counter. After the timeout period determined by the value in TC4 - TC1, the CP Gain bit in the N counter latch is automatically reset to "0" and the device reverts to normal mode instead of Fastlock. See Table 5 for the timeout periods.

Timer Counter Control

The user has the option of programming two charge pump currents. The intent is that the Current Setting 1 is used when the RF output is stable and the system is in a static state. Current Setting 2 is meant to be used when the system is dynamic and in a state of change (i.e. when a new output frequency is programmed).

The normal sequence of events is as follows:

The user initially decides what the preferred charge pump currents are going to be. For example, they may choose 2.5mA as Current Setting 1 and 5mA as the Current Setting 2.

At the same time they must also decide how long they want the secondary current to stay active before reverting to the primary current. This is controlled by the Timer Counter Control Bits DB14 to DB11 (TC4 - TC1) in the Function Latch. The truth table is given in Table 5.

Now, when the user wishes to program a new output frequency, they can simply program the A,B counter latch with new values for A and B. At the same time they can set the CP Gain bit to a "1" ,which sets the charge pump with the value in CPI6 - CPI4 for a period of time determined by TC4 - TC1. When this time is up, the charge pump current reverts to the value set by CPI3 - CPI1. At the same time the CP Gain bit in the A, B Counter latch is reset to 0 and is now ready for the next time that the user wishes to change the frequency again.

Note that there is an enable feature on the Timer Counter. It is enabled when Fastlock Mode 2 is chosen by setting the Fastlock Mode bit (DB10) in the Function Latch to "1".

Charge Pump Currents

CPI3, CPI2, CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, CPI4 program Current Setting 2 for the charge pump. The truth table is given in Table 5.

Prescaler Value
P2 and P1 in the Function Latch set the prescaler values. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 125MHz. Thus, with an RF frequency of 2GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

The Initialization Latch
When C2, C1 = 1, 1 then the Initialization Latch is programmed. This is essentially the same as the Function Latch (programmed when C2, C1 = 1, 0).

However, when the Initialization Latch is programmed there is a additional internal reset pulse applied to the R and N counters. This pulse ensures that the N counter is at load point when the N counter data is latched and the device will begin counting in close phase alignment.

If the Latch is programmed for synchronous powerdown (CE pin is High; PD1 bit is High; PD2 bit is Low), the internal pulse also triggers this powerdown. The prescaler reference and the oscillator input buffer are unaffected by the internal reset pulse and so close phase alignment is maintained when counting resumes.

When the first N counter data is latched after initialisation, the internal reset pulse is again activated. However, successive N counter loads after this will not trigger the internal reset pulse.

Device Programming After Initial Power-Up.
After initially powering up the device, there are three ways to program the device.

Initialisation Latch Method.

Apply V_{DD}.
Program the Initialisation Latch ("11" in 2 lsb's of input word). Make sure that F1bit is programmed to "0".
Then do an R load ("00" in 2 lsb's).
Then do an N load ("01" in 2 lsb's).
When the Initialisation Latch is loaded, the following occurs:

1. The function latch contents are loaded.
2. An internal pulse resets the R, N and timeout counters to load state conditions and also tri-states the charge pump. Note that the prescaler bandgpap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
3. Latching the first N counter data after the initialisation word will activate the same internal reset pulse. Successive N loads will not trigger the internal reset pulse unless there is another initialisation.

The CE pin Method.
Apply V_{DD}.

Bring CE low to put the device into power-down. This is an asychronous power-down in that it happens immediately.
Program the Function Latch (10).
Program the R Counter Latch (00).
Program the N Counter Latch (01).
Bring CE high to take the device out of power-down. The R and N counter will now resume counting in close alignment. Note that after CE goes high, a duration of 1us may be required for the prescaler bandgap voltage and oscillator input buffer bias to reach steady state.
CE can be used to power the device up and down in order to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled as long as it has been programmed at least once after Vcc was initially applied.

The Counter Reset Method
Apply V_{DD}.

Do a Function Latch Load ("10" in 2 lsb's). As part of this, load "1" to the F1 bit. This enables the counter reset.
Do an R Counter Load ("00" in 2 lsb's).
Do an N Counter Load ("01" in 2 lsb's).
Do a Function Latch Load ("10" in 2 lsb's). As part of this, load "0" to the F1 bit. This disables the counter reset.
This sequence provides the same close alignment as the initialisation method. It offers direct control over the internal reset. Note that counter reset holds the counters at load point and tri-states the charge pump, but does not trigger synchronous power-down. The counter reset method requires an extra function latch load compared to the initialisation latch method.