14-Bit, 65 MSPS Monolithic A/D Converter

PRELIMINARY TECHNICAL DATA AD6644

FEATURES
65 MSPS Guaranteed Sample Rate
40 MSPS Version Available
Sampling jitter < 300 fs
100 dB Multi-tone SFDR
Single +5V Supply
1.4 W Power Dissipation
Differential Analog Inputs
Digital Outputs
Two's Complement Format
3.3V or 5V CMOS-Compatible
DataReady for Output Latching

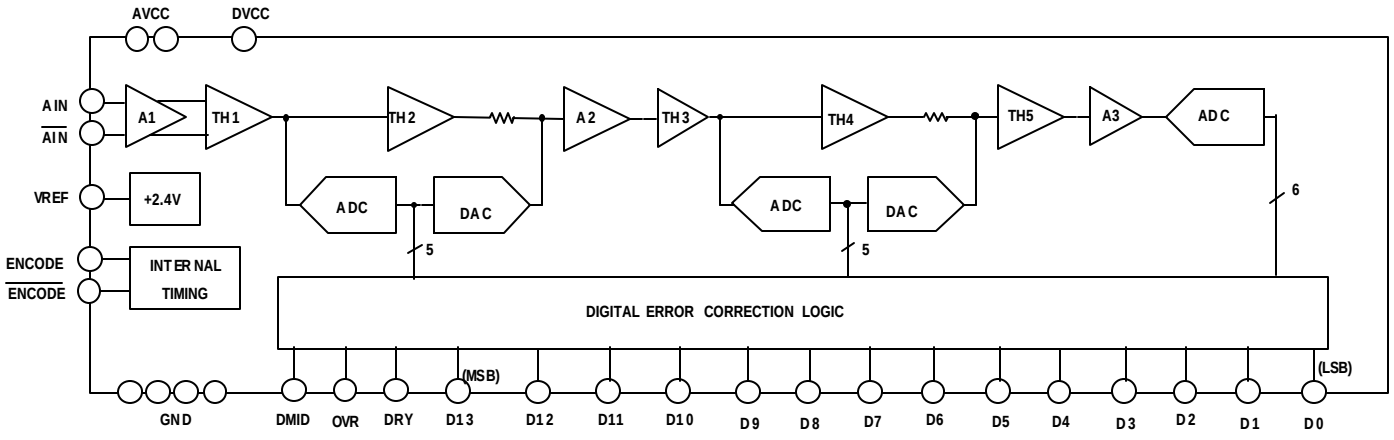
APPLICATIONS
Multi-Channel, Multi-Mode Receivers
AMPS, IS-136, CDMA, GSM, 3rd Gen.
Single Channel Digital Receivers
Antenna Array Processing
Communications Instrumentation
Radar, Infrared Imaging

PRODUCT DESCRIPTION
The AD6644 is a high speed, high performance, monolithic 14-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference are included on chip to provide a complete conversion solution. The AD6644 runs off of a single +5 V supply and provides CMOS-compatible digital outputs. It is the third generation in a wideband ADC family, preceded by the AD9042 (12 b. 41 MSPS) and the AD6640 (12 bit 65 MSPS, IF-sampling.)

Designed for multi-channel, multi-mode receivers, the AD6644 is part of ADI's new SoftCell™ transceiver chipset. The AD6644 maintains 100dB multi-tone, spurious-free dynamic range (SFDR) through the Nyquist band. This break-through performance eases the burden placed on multi-mode digital receivers (software radios) which are typically limited by the ADC. Noise performance is exceptional; typical signal-to-noise ratio is 74 dB.

The AD6644 is also useful in single channel digital receivers designed for use in wide channel-bandwidth systems (CDMA, W-CDMA). With oversampling, harmonics can be placed outside the analysis bandwidth. Oversampling also facilitates the use of decimation receivers (such as the AD6620) allowing the noise floor in the analysis bandwidth to be reduced. By replacing traditional analog filters with predictable digital components, modern receivers can be built using fewer "RF" components, resulting in decreased manufacturing costs, higher manufacturing yields, and improved reliability.

The AD6644 is built on Analog Devices high-speed complementary bipolar process (XFCB) and uses an innovative, multi-pass circuit architecture. Units are packaged in a 52-pin Quad Plastic Flatpack (LQFP) specified from -25°C to +85°C.



AD6644 Functional Block Diagram

AD6644 - PRELIMINARY SPECIFICATIONS

DC SPECIFICATIONS (AVCC = +5V, DVCC = +3.3V; TMIN = -25°C, TMAX = +85°C)

Parameter	Temp	Test Level	AD6644AST-40 Min	AD6644AST-40 Typ	AD6644AST-40 Max	AD6644AST-65 Min	AD6644AST-65 Typ	AD6644AST-65 Max	Units
RESOLUTION				14			14		Bits
ACCURACY									
No Missing Codes	Full	II		Guaranteed			Guaranteed		
Offset Error	Full	II		3			3		mV
Gain Error	Full	II		6			6		% FS
Differential Nonlinearity (DNL)	Full	II	-0.75	± 0.25	+0.75	-0.75	± 0.25	+0.75	LSB
Integral Nonlinearity (INL)	Full	V		± 0.50			± 0.50		LSB
TEMPERATURE DRIFT									
Offset Error	Full	V		TBD			TBD		ppm/°C
Gain Error	Full	V		TBD			TBD		ppm/°C
POWER SUPPLY REJECTION	Full	V		TBD			TBD		mV/V
ANALOG INPUTS (AIN, $\overline{AIN}$)									
Differential Input Voltage Range	Full			2.2			2.2		V_{PP}
Differential Input Resistance	Full	IV		1			1		kΩ
Differential Input Capacitance	+25°C	V		TBD			TBD		pF
POWER SUPPLY									
Supply Voltages									
AVCC[1]	Full	II	4.75	5.0	5.30	4.75	5.0	5.30	V
DVCC	Full	II	3.0	3.3	5.30	3.0	3.3	5.30	V
Supply Current									
I_{AVCC} (AVCC = 5.0V)	Full	II		260			260		mA
I_{DVCC} (DVCC = 3.3V)	Full	II		30			30		mA
POWER CONSUMPTION	Full	II		1.4			1.4		W

NOTES
[1] AVCC may be varied from +4.75 to +5.3V. However, rated AC (harmonics) performance is valid only over the range AVCC=+5.0 to +5.3V.

DIGITAL SPECIFICATIONS (AVCC = +5V, DVCC = +3.3V; TMIN = -25°C, TMAX = +85°C)

Parameter (Conditions)	Temp	Test Level	AD6644AST-40 Min	AD6644AST-40 Typ	AD6644AST-40 Max	AD6644AST-65 Min	AD6644AST-65 Typ	AD6644AST-65 Max	Units
ENCODE INPUTS (ENC, $\overline{ENC}$)									
Differential Input Voltage[1]	Full	IV	0.4			0.4			V_{PP}
Differential Input Resistance	+25°C	V		10			10		kΩ
Differential Input Capacitance	+25°C	V		2.5			2.5		pF
LOGIC OUTPUTS (D13 - D0, DRY)									
Logic Compatibility				CMOS			CMOS		
Logic "1" Voltage (DVCC = +3.3V)	Full	II	2.8	DVCC-0.2		2.8	DVCC-0.2		V
Logic "0" Voltage(DVCC = +3.3V)	Full	II		0.2	0.5		0.2	0.5	V
Logic "1" Voltage (DVCC = +5.0V)	Full	IV	4	DVCC-0.35		4	DVCC-0.35		V
Logic "0" Voltage(DVCC = +5.0V)	Full	IV		0.35	0.5		0.35	0.5	V
Output Coding				Twos Complement			Twos Complement		

NOTES
[1]All AC specifications tested by driving ENCODE and $\overline{ENCODE}$ differentially.

AD6644 - PRELIMINARY SPECIFICATIONS cont.

SWITCHING SPECIFICATIONS

(AVCC = +5V, DVCC = +3.3V; ENCODE & $\overline{\text{ENCODE}}$ = Maximum Conversion Rate MSPS; TMIN = -25°C, TMAX = +85°C)

Parameter (Conditions)	Temp	Test Level	AD6644AST-40 Min	AD6644AST-40 Typ	AD6644AST-40 Max	AD6644AST-65 Min	AD6644AST-65 Typ	AD6644AST-65 Max	Units
Maximum Conversion Rate	Full	II	40			65			MSPS
Minimum Conversion Rate	Full	IV			15			15	MSPS
Encode Pulse Width High (t_{ENCH})	Full	IV	10			6.5			ns
Encode Pulse Width Low (t_{ENCL})	Full	IV	10			6.5			ns

AC SPECIFICATIONS[1]

(AVCC = +5Vmin, DVCC = +3.3V; ENCODE & $\overline{\text{ENCODE}}$ = Maximum Conversion Rate; TMIN = -25°C, TMAX = +85°C)

Parameter (Conditions)	Temp	Test Level	AD6644AST-40 Min	AD6644AST-40 Typ	AD6644AST-40 Max	AD6644AST-65 Min	AD6644AST-65 Typ	AD6644AST-65 Max	Units
SNR									
Analog Input 2.2 MHz	+25°C	V		74.5			74.5		dB
@ -1dBFS 15.5 MHz	+25°C	V		74.0			74.0		dB
31.0 MHz	+25°C	V		73.5			73.5		dB
SINAD[2]									
Analog Input 2.2 MHz	+25°C	V		74.5			74.5		dB
@ -1dBFS 15.5 MHz	+25°C	V		74.0			74.0		dB
31.0 MHz	+25°C	V		73.0			73.0		dB
Worst Harmonic (2^{nd} or 3^{rd})[2]									
Analog Input 2.2 MHz	+25°C	V		90			90		dBc
@ -1dBFS 15.5 MHz	+25°C	V		90			90		dBc
31.0 MHz	+25°C	V		86			86		dBc
Worst Harmonic (4^{th} or higher)[2]									
Analog Input 2.2 MHz	+25°C	V		93			93		dBc
@ -1dBFS 15.5 MHz	+25°C	V		92			92		dBc
31.0 MHz	+25°C	V		92			92		dBc
Multi-tone SFDR[2,3]									
Analog Input @ 2.2 MHz	Full	V		100			100		dBFS
15.5 MHz	Full	V		100			100		dBFS
31.0 MHz	Full	V		100			100		dBFS
Two-tone IMD Rejection[2]									
F1, F2 @ -7 dBFS	Full	V		90			90		dBc
Analog Input Bandwidth	+25°C	V		250			250		MHz

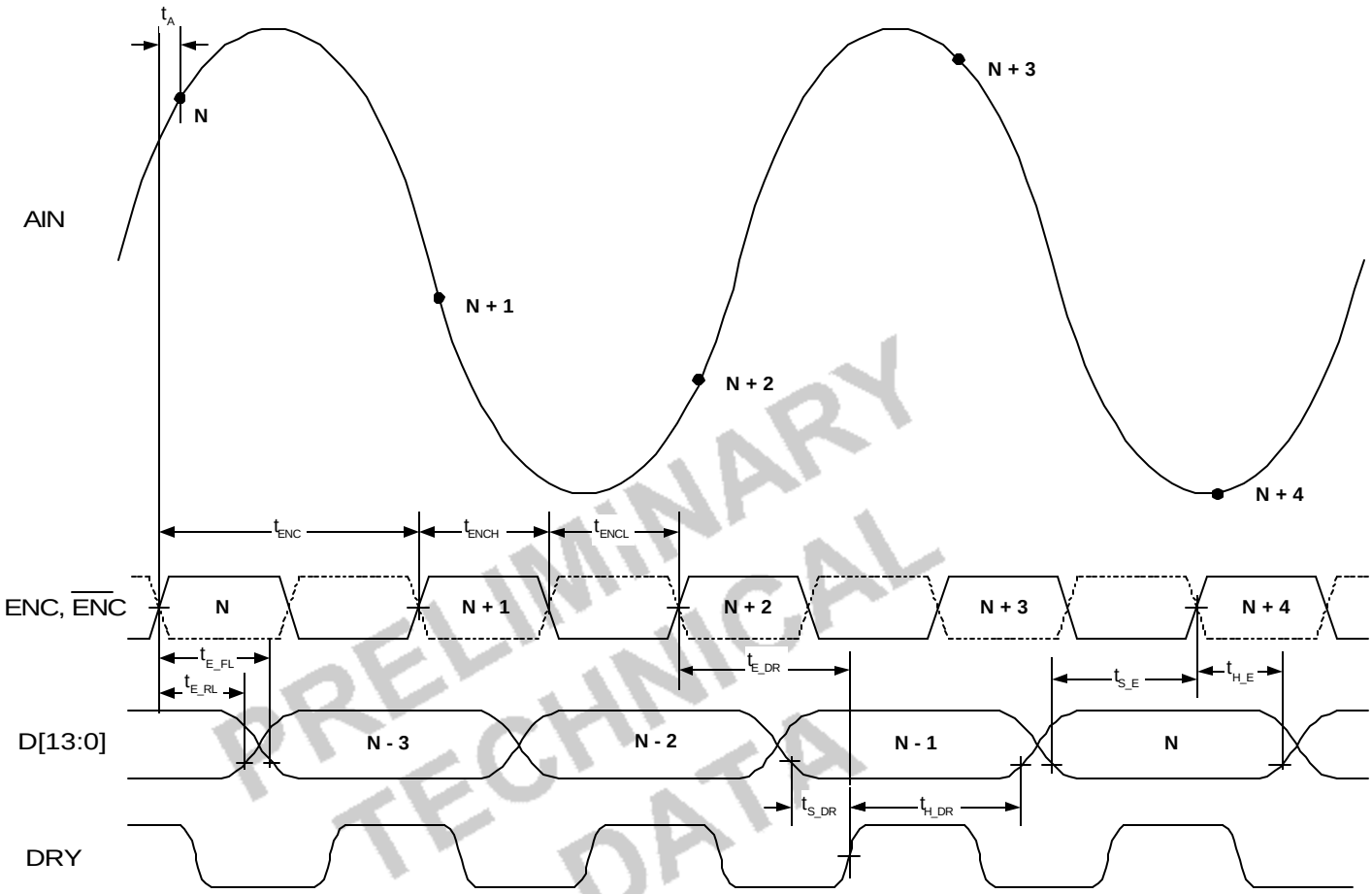
NOTES

[1] All AC specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially.

[2] AVCC = +5V to +5.3V for rated AC performance

[3] Analog Input signal power swept from -20 dBFS to -100 dBFS.

AD6644 - PRELIMINARY SPECIFICATIONS cont.



SWITCHING SPECIFICATIONS cont.

Parameter	Name	Temp	Test Level	AD6644AST-40/65 Min	Typ	Max	Units
ENCODE Input Parameters							
Encode Period	t_{ENC}				Input Condition		ns
Encode Pulse Width High	t_{ENCH}				Input Condition		ns
Encode Pulse Width Low	t_{ENCL}				Input Condition		ns
ENCODE/DataReady							
Encode Rising to DataReady Rising	t_{E_DR}	Full	IV		t_{ENCH} + 3		ns
@ 65MSPS (50% duty cycle)	t_{E_DR}	Full	IV		10.7		ns
ENCODE/DATA (D13:0)							
ENC to DATA Falling Low	t_{E_FL}	Full	IV		6		ns
ENC to DATA Rising Low	$t_{E\ RL}$	Full	IV		4		ns
ENCODE to DATA Delay (Hold Time)	t_{H_E}	Full	IV		4		ns
ENCODE to DATA Delay (Setup Time)	$t_{S\ E}$	Full	IV		$t_{ENC} - 6$		ns
Encode = 65 MSPS	$t_{S\ E}$	Full	IV		9.4		ns
DataReady(DRY)/DATA							
DataReady to DATA Delay (Hold Time)	t_{H_DR}	Full	IV		$t_{ENC} - t_{E\_DR} + t_{E\_RL}$		ns
Encode = 65 MSPS (50% duty cycle)	t_{H_DR}	Full	IV		8.7		ns
DataReady to DATA Delay (Setup Time)	$t_{S\ DR}$	Full	IV		$t_{E\_DR} - t_{E\_FL}$		ns
@ 65MSPS (50% duty cycle)	$t_{S\ DR}$	Full	IV		4.7		ns
Aperture Delay	t_A	25°C	V		TBD		ps
Aperture Uncertainty (jitter)	t_J	25°C	V		0.3		ps rms

AD6644 - PRELIMINARY SPECIFICATIONS cont.

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Min	Max	Units
ELECTRICAL			
AVCC , DVCC Voltage	0	7	V
ANALOG INPUT Voltage	0	AVCC	V
ANALOG INPUT Current		10	mA
Digital Input Voltage (ENCODE)	0	AVCC	V
ENC, $\overline{\text{ENC}}$ Differential Voltage		AVCC	V
Digital Output Current	-10	10	mA
ENVIRONMENTAL[2]			
Operating Temperature Range (Ambient)	-25	+85	^{o}C
Maximum Junction Temperature		+150	^{o}C
Lead Temperature (Soldering, 10 sec)		+300	^{o}C
Storage Temperature Range (Ambient)	-65	+150	^{o}C

NOTES

[1] Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2] Typical thermal impedance for "ST" package (52-pin LQFP): θ_{JA} = TBD ^{o}C/W

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at +25°C and guaranteed by design and characterization at temperature extremes.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

ORDERING GUIDE

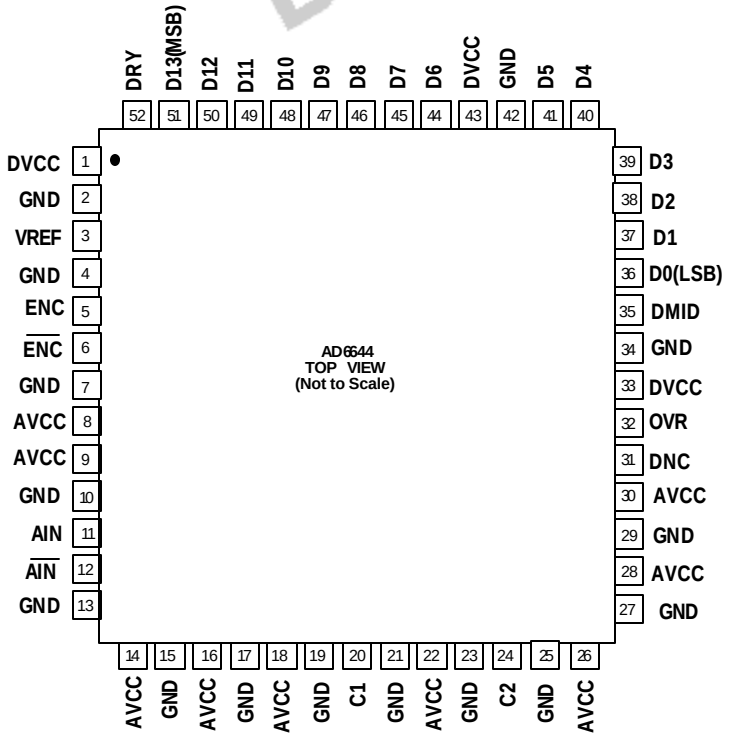
Model	Temperature Range	Package Description	Status
AD6644XST		52 pin LQFP	X-Grade
AD6644AST-40	-25^{o}C to +85^{o}C (Ambient)	52 pin LQFP	Pre-Release
AD6644AST-65	-25^{o}C to +85^{o}C (Ambient)	52 pin LQFP	Pre-Release
AD6644ST/PCB		Evaluation board with AD6644XST	Consult Factory

AD6644 - PRELIMINARY SPECIFICATIONS cont.

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Function
1, 33, 43	DVCC	+3.3V/+5V Power supply (digital) output stage only
2, 4, 7, 10, 13, 15, 17, 19 21, 23, 25, 27, 29, 34, 42	GND	Ground
3	VREF	+2.4V Reference
5	ENC	Encode Input, conversion initiated on rising edge
6	$\overline{\text{ENC}}$	Complement of ENC, differential input
8, 9, 14, 16, 18, 22, 26, 28, 30	AVCC	+5V Analog Power supply
11	AIN	Analog Input
12	$\overline{\text{AIN}}$	Complement of AIN, differential analog input
20	C1	Internal voltage reference, bypass to ground with 0.1uF and 0.01uF microwave chip capacitor.
24	C2	Internal voltage reference, bypass to ground with 0.1uF and 0.01uF microwave chip capacitor.
31	DNC	Do not connect this pin.
32	OVR	Over-range bit, high indicates analog input exceeds +/- FS
35	DMID	Output Data Voltage Midpoint; approximately equal to (DVCC)/2
36	D0	Digital Output Bit (Least Significant Bit); twos complement
37-41, 44-50	D1-D5, D6-D12	Digital Output Bits in twos complement
51	D13	Digital Output Bit (Most Significant Bit); twos complement
52	DRY	DataReady Output

PIN CONFIGURATION

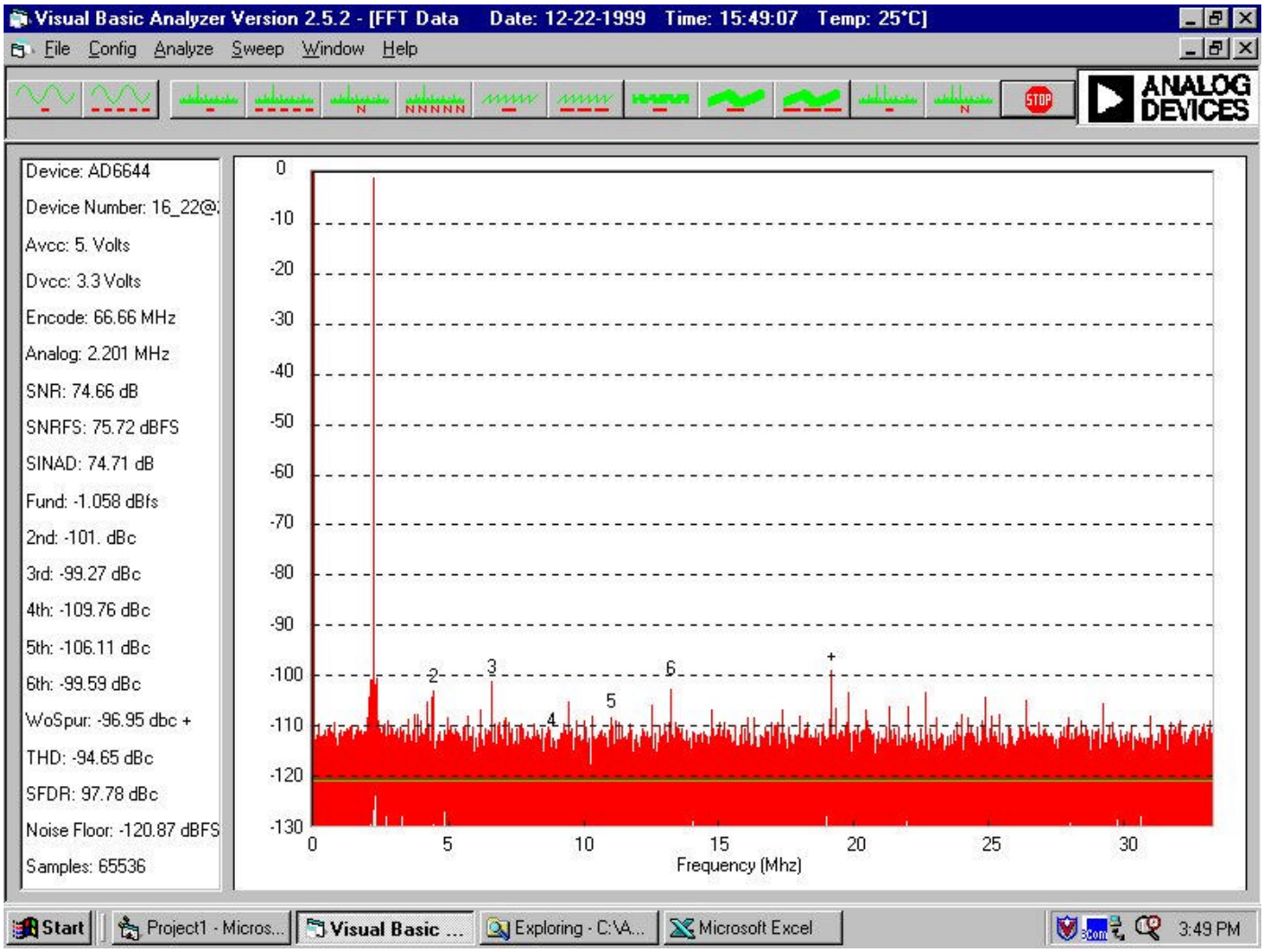


DNC = Do Not Connect

AD6644 - PRELIMINARY SPECIFICATIONS cont.

AD6644 PERFORMANCE DATA @ -1dBFS

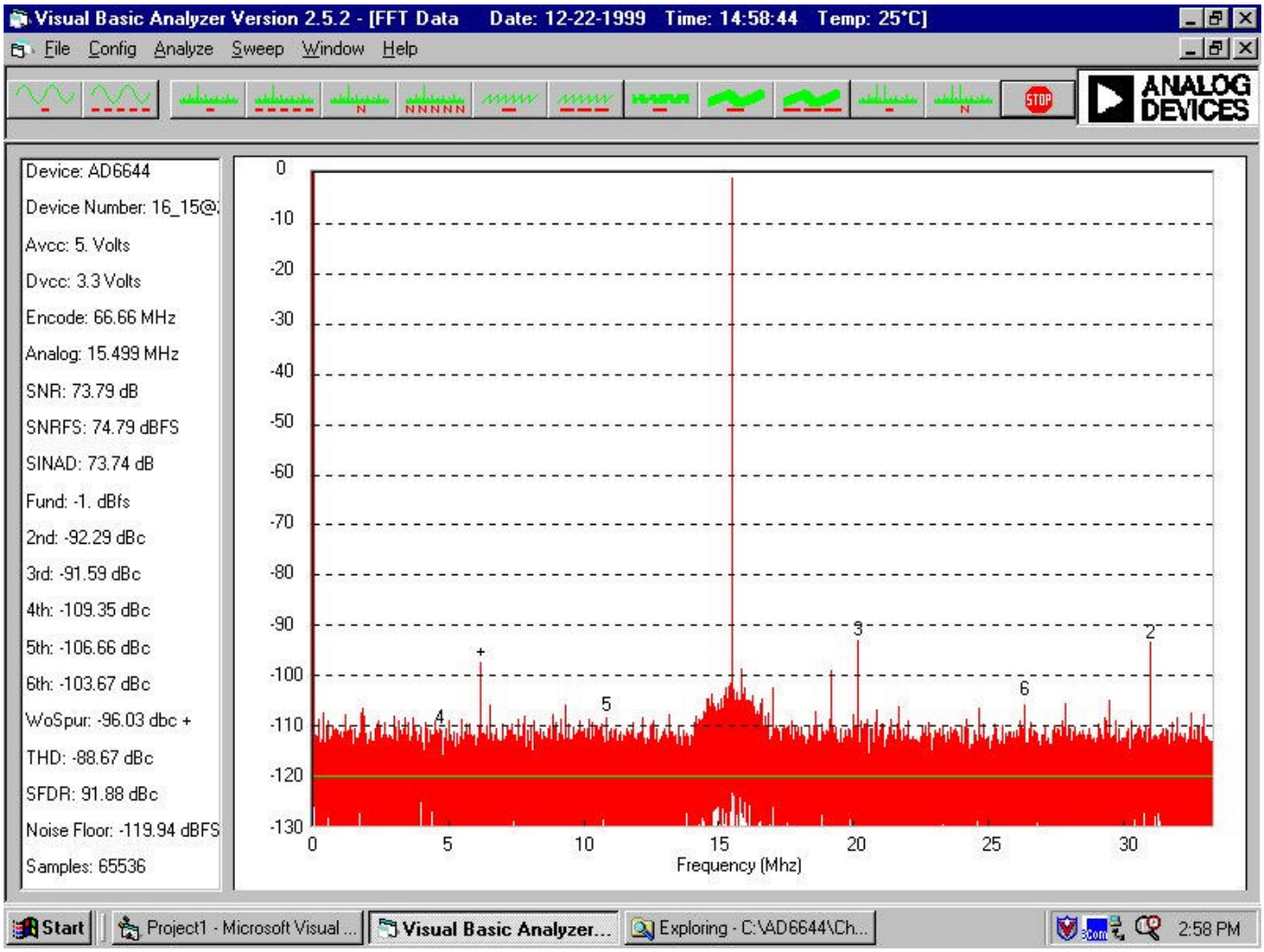
Encode = 66.6 MSPS, AIN = 2.2 MHz @ -1 dBFS
SNR = 74.6 dB, 2nd Harmonic @ -101 dBc, 3rd Harmonic @ -99 dBc
Worst Other Harmonic @ -97 dBc



AD6644 - PRELIMINARY SPECIFICATIONS cont.

AD6644 PERFORMANCE DATA @ -1dBFS

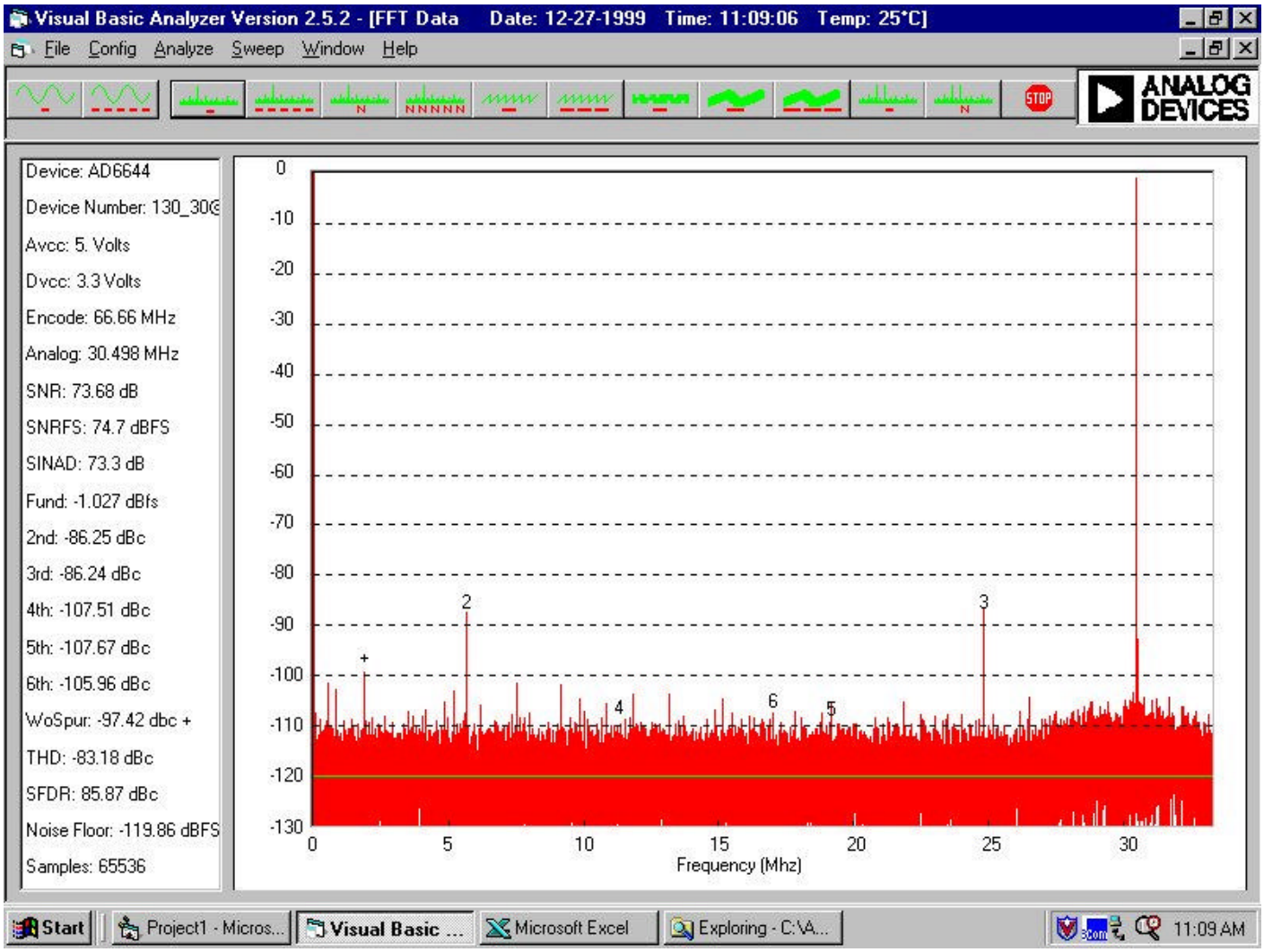
Encode = 66.6 MSPS, AIN = 15.5 MHz @ -1 dBFS
SNR = 74 dB, 2nd Harmonic @ -92 dBc, 3rd Harmonic @ -92 dBc
Worst Other Harmonic @ -96 dBc



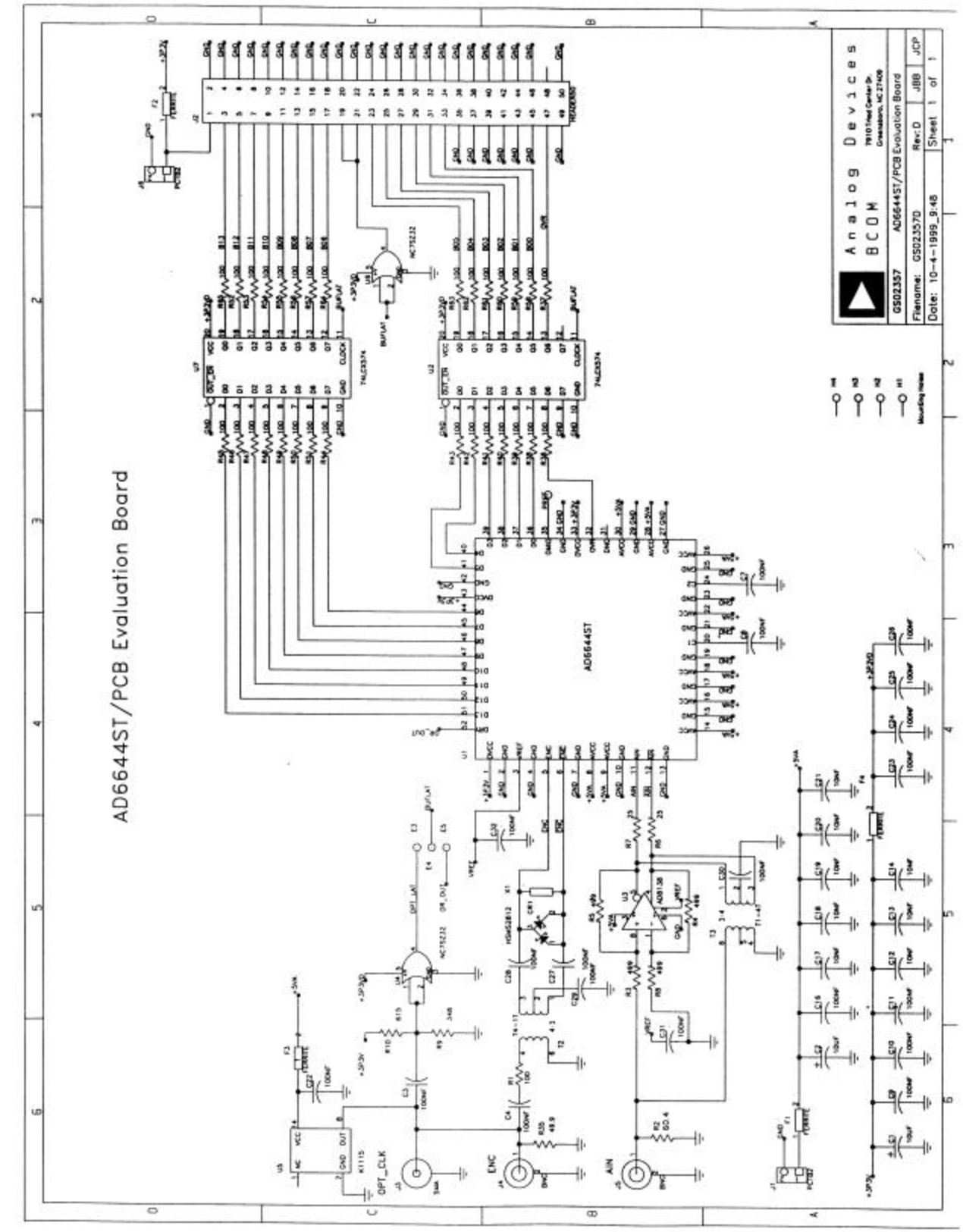
AD6644 - PRELIMINARY SPECIFICATIONS cont.

AD6644 PERFORMANCE DATA @ -1dBFS

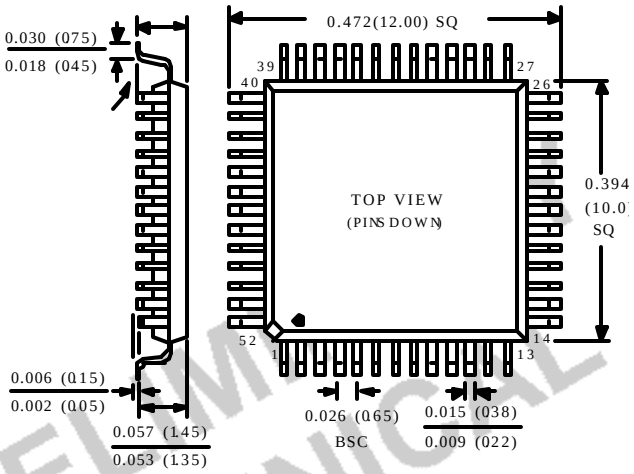
Encode = 66.6 MSPS, AIN = 30.5 MHz @ -1 dBFS
SNR = 73.7 dB, 2nd Harmonic @ -86 dBc, 3rd Harmonic @ -86 dBc
Worst Other Harmonic @ -97 dBc



AD6644 Evaluation Board Schematic



AD6644 PACKAGE



AD6644AST Package Outline