PRELIMINARY
PRODUCT SPECIFICATION

Z86C02/E02/L02

CMOS Z8® 8-BIT LOW-COST 512 BYTE-ROM MICROCONTROLLERS

FEATURES

Part Number	ROM (Bytes)	RAM* (Bytes)	Speed (MHz)	Auto Latch	Permanent WDT
Z86C02	512	61	8	Optional	Optional
Z86E02	512	61	8	Optional	Optional
Z86L02	512	61	8	Optional	Optional

* General-Purpose

- 18-Pin DIP and SOIC Packages
- 0°C to 70°C Standard Temperature
  –40°C to 105°C Extended Temperature
  (Z86C02/E02 only)
- 3.0V to 5.5V Operating Range (Z86C02)
  4.5V to 5.5V Operating Range (Z86E02)
  2.0V to 3.9V Operating Range (Z86L02)
- 14 Input / Output Lines
- Five Vectored, Prioritized Interupts from Five Different Sources
- Two On-Board Comparators
- Software Enabled Watch-Dog Timer
- Programmable Interrupt Polarity
- Two Standby Modes: STOP and HALT
- Low-Voltage Protection
- ROM Mask/OTP Options:
  – Low-Noise (Z86C02/E02 only)
  – ROM Protect
  – Auto Latch
  – Permanent Watch-Dog Timer (WDT)
  – RC Oscillator (Z86C02/L02 Only)
  – 32 KHz Operation (Z86C02/L02 Only)
- One Programmable 8-Bit Counter/Timer, With a 6-Bit Programmable Prescaler
- Power-On Reset (POR) Timer
- On-Chip Oscillator that Accepts RC, Crystal, Ceramic Resonator, LC, or External Clock Drive (C02/L02 only)
- On-Chip Oscillator that Accepts RC or External Clock Drive (Z86E02 SL1903 only)
- On-Chip Oscillator that Accepts Crystal,Ceramic Resonator, LC, or External Clock Drive (Z86E02 only)
- Clock-Free WDT Reset
- Low-Power Consumption (50mw)
- Fast Instruction Pointer
  (1.5µs @ 8 MHz)
- Fourteen Digital Inputs at CMOS Levels; Schmitt-Triggered

GENERAL DESCRIPTION

Zilog's Z86C02/E02/L02 Microcontrollers (MCUs) are members of the Z8® single-chip microcontroller family which offer easy software/hardware system expansion.

For applications demanding powerful I/O capabilities, the MCU's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

One on-chip counter/timers, with a large number of user selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications. Additionally, two on-board comparators process analog signals with a common reference voltage (Figure 1).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B/ /W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

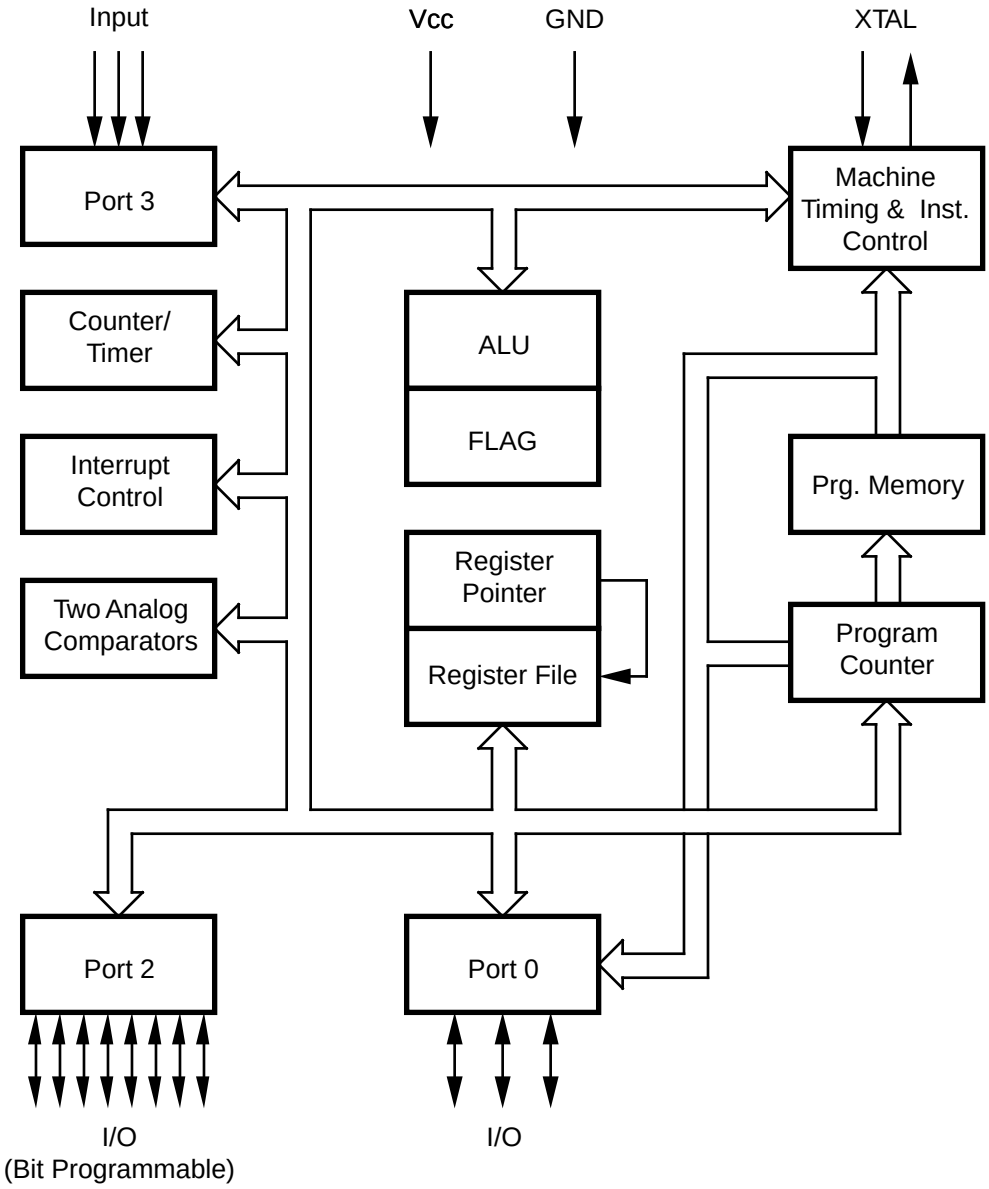


Figure 1. Z86C02/E02/L02
Functional Block Diagram

GENERAL DESCRIPTION (Continued)

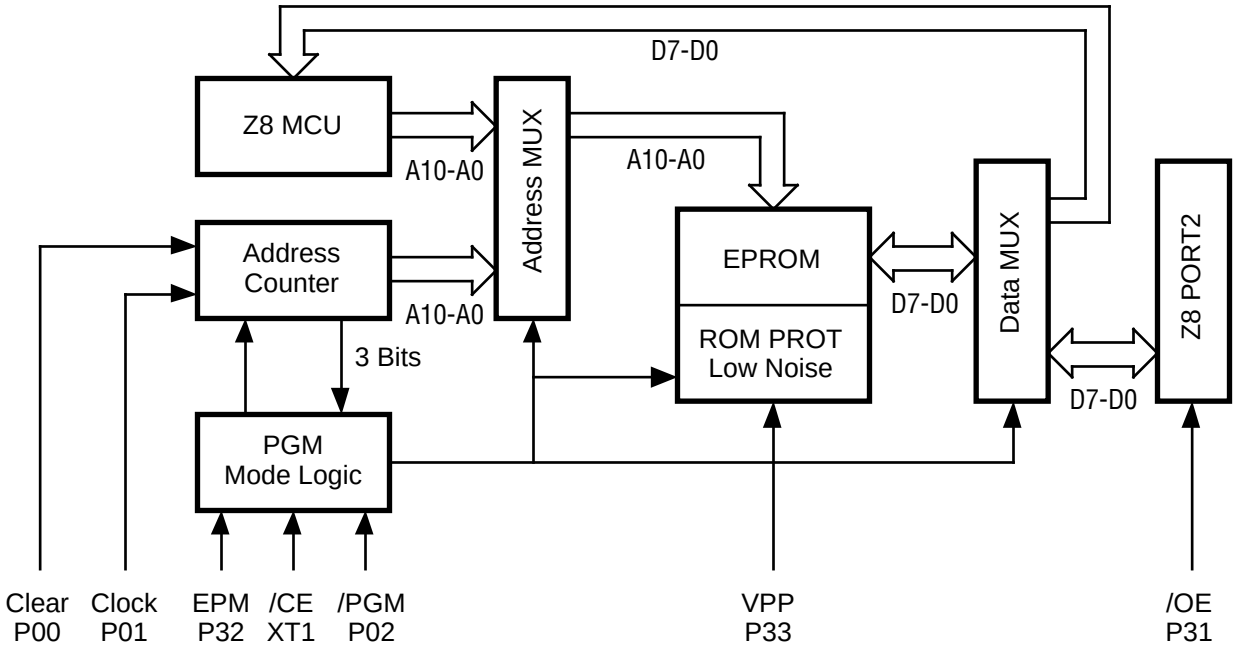


Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTIONS

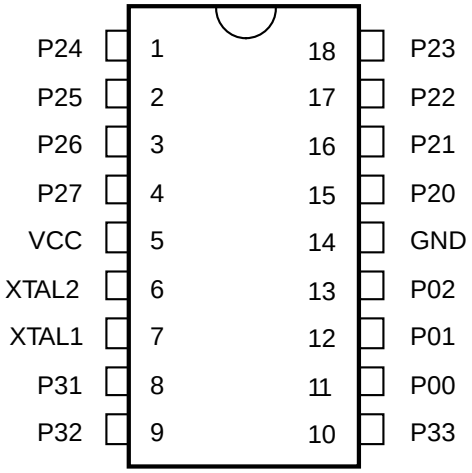


Figure 3. 18-Pin DIP Configuration

Table 1. 18-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{cc}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0, 1, 2	In/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0, 1, 2, 3	In/Output

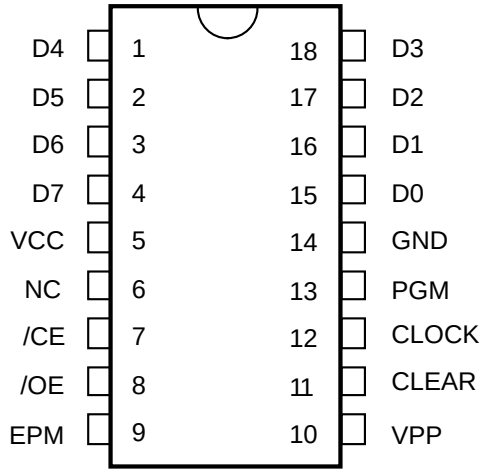


Figure 4. 18-Pin EPROM Mode Configuration

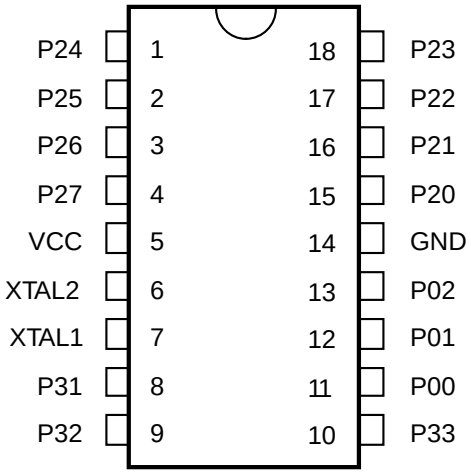


Figure 5. 18-Pin Standard Mode Configuration

Table 2. EPROM Mode Pin Identification

Pin #	Symbol	Function	Direction
1-4	D7-D4	Data 4, 5, 6, 7	In/Output
5	V_{cc}	Power Supply	
6	NC	No Connection	
7	/CE	Chip Enable	Input
8	/OE	Output Enable	Input
9	EPM	EPROM Program Mode	Input
10	V_{PP}	Program Voltage	Input
11	Clear	Clear Clock	Input
12	Clock	Address	Input
13	/PGM	Program Mode	Input
14	GND	Ground	
15-18	D3-D0	Data 0, 1, 2, 3	In/Output

PIN DESCRIPTION (Continued)

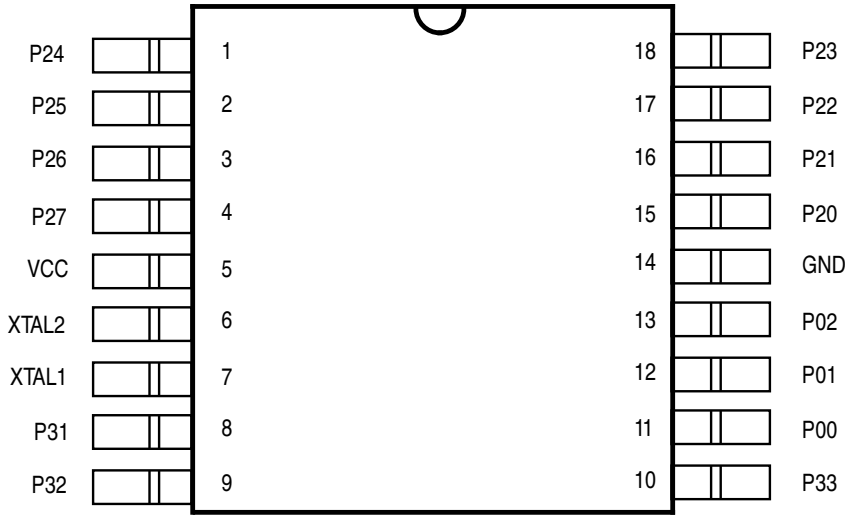


Figure 5. 18-Pin SOIC Configuration

Table 2. 18-Pin SOIC Pin Identification

Standard Mode Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4,5,6,7	In/Output
5	V_{cc}	Power Supply	
6	XTAL2	Crystal Osc. Clock	Output
7	XTAL1	Crystal Osc. Clock	Input
8	P31	Port 3, Pin 1, AN1	Input

Standard Mode Pin #	Symbol	Function	Direction
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0,1,2	In/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0,1,2,3	In/Output

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	–40	+105	C
Storage Temperature	–65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	–0.7	+12	V
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V
Voltage on Pin 7 with Respect to V_{SS} [Note 2] (Z86C02/L02)	–0.7	V_{DD}+1	V
Voltage on Pin 7,8,9,10 with Respect to V_{SS} [Note 2] (Z86E02)	–0.7	V_{DD}+1	V
Total Power Dissipation		462	mW
Maximum Allowed Current out of V_{SS}		300	mA
Maximum Allowed Current into V_{DD}		270	mA
Maximum Allowed Current into an Input Pin [Note 3]	–600	+600	µA
Maximum Allowed Current into an Open-Drain Pin [Note 4]	–600	+600	µA
Maximum Allowed Output Current Sinked by Any I/O Pin		20	mA
Maximum Allowed Output Current Sourced by Any I/O Pin		20	mA
Maximum Allowed Output Current Sinked by Port 2, Port 0		80	mA
Maximum Allowed Output Current Sourced by Port 2, Port 0		80	mA

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

Notes:
[1] This applies to all pins except where otherwise noted. Maximum current into pin must be ±600µA.
[2] There is no input protection diode from pin to V_{DD}.
[3] This excludes Pin 6 and Pin 7.
[4] Device pin is not at an output Low state.

Total Power dissipation = V_{DD} x [I_{DD} – (sum of I_{OH})] + sum of [(V_{DD} – V_{OH}) x I_{OH}] + sum of (V_{0L} x I_{0L})

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 6).

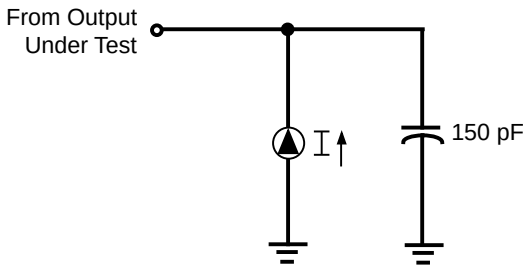


Figure 6. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	15 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC ELECTRICAL CHARACTERISTICS

Z86C02

Sym	Parameter	V_{CC}[4]	T_A = 40°C to +105°C / T_A = 0°C to +70°C Min	Max	Typical @25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	$0.8V_{CC}$	V_{CC}+0.3	1.7	V	Driven by External Clock Generator	
		5.5V	$0.8V_{CC}$	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS}–0.3	$0.2V_{CC}$	0.8	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	$0.7V_{CC}$	V_{CC}+0.3	1.8	V		[1]
		5.5V	$0.7V_{CC}$	V_{CC}+0.3	2.8	V		[1]
V_{IL}	Input Low Voltage	3.0V	V_{SS}–0.3	$0.2V_{CC}$	0.8	V		[1]
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.5	V		[1]
V_{OH}	Output High Voltage	3.0V	V_{CC}–0.4		3.0	V	I_{OH} = –2.0 mA	[5]
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	[5]
		3.0V	V_{CC}–0.4		3.0	V	Low Noise @ I_{OH} = –0.5 mA	
		5.5V	V_{CC}–0.4		4.8	V	Low Noise @ I_{OH} = –0.5 mA	
V_{OL1}	Output Low Voltage	3.0V		0.8	0.2	V	I_{OL} = +4.0 mA	[5]
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	[5]
		3.0V		0.8	0.2	V	Low Noise @ I_{OL} = 1.0 mA	
		5.5V		0.4	0.1	V	Low Noise @ I_{OL} = 1.0 mA	
V_{OL2}	Output Low Voltage	3.0V		1.0	0.8	V	I_{OL} = +12 mA	[5]
		5.5V		0.8	0.3	V	I_{OL} = +12 mA	[5]
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25	10	mV		
		5.5V		25	10	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset					V		
			2.2	2.8	2.6	V		[9]
			2.0	3.0	2.6	V		[10]
I_{IL}	Input Leakage (Input Bias Current of Comparator)	3.0V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range		0	V_{CC}–1.0		V		[9]
			0	V_{CC}–1.5		V		[10]

DC ELECTRICAL CHARACTERISTICS (Continued)
Z86C02

Sym	Parameter	V_{CC}[4]	$T_A = -40°C$ to $+105°C$ / $T_A = 0°C$ to $+70°C$ Min	Max	Typical @25°C	Units	Conditions	Notes
I_{CC}	Supply Current	3.0V		3.5	1.5	mA	@2MHz	[5,6,7]
		5.5V		7.0	3.8	mA	@2MHz	[5,6,7]
		3.0V		8.0	3.0	mA	@8MHz	[5,6,7]
		5.5V		11.0	4.4	mA	@8MHz	[5,6,7]
I_{CC1}	Standby Current (Halt Mode)	3.0V		2.5	0.7	mA	@2MHz	[5,6,7]
		5.5V		4.0	2.5	mA	@2MHz	[5,6,7]
		3.0V		4.0	1.0	mA	@8MHz	[5,6,7]
		5.5V		5.0	3.0	mA	@8MHz	[5,6,7]
I_{CC}	Supply Current (Low Noise Mode)	3.0V		3.5	1.5	mA	@1MHz	[5,6,7]
		5.5V		7.0	3.8	mA	@1MHz	[5,6,7]
		3.0V		5.8	2.5	mA	@2MHz	[5,6,7]
		5.5V		9.0	4.0	mA	@2MHz	[5,6,7]
		3.0V		8.0	3.0	mA	@4MHz	[5,6,7]
		5.5V		11.0	4.4	mA	@4MHz	[5,6,7]

Z86C02

Sym	Parameter	V_{CC} [4]	T_A = -40°C to +105°C / T_A = 0°C to +70°C Min	Max	Typical @25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Low Noise Halt Mode)	3.0V		2.5	0.7	mA	@1MHz	[6,7,8]
		5.5V		4.0	2.5	mA	@1MHz	[6,7,8]
		3.0V		3.0	0.9	mA	@2MHz	[6,7,8]
		5.5V		4.5	2.8	mA	@2MHz	[6,7,8]
		3.0V		4.0	1.0	mA	@4MHz	[6,7,8]
		5.5V		5.0	3.0	mA	@4MHz	[6,7,8]
I_{CC2}	Standby Current (Stop Mode)	3.0V		10	1.0	µA		[6,7,8,9]
		3.0V		20	1.0	µA		[6,7,8,10]
		5.5V		10	1.0	µA		[6,7,8,9]
		5.5V		20	1.0	µA		[6,7,8,10]
I_{ALL}	Auto Latch Low Current	3.0V		12	3.0	µA	$0V<V_{IN}<V_{CC}$	
		5.5V		32	16	µA	$0V<V_{IN}<V_{CC}$	
I_{ALH}	Auto Latch High Current	3.0V		–8	-1.5	µA	$0V<V_{IN}<V_{CC}$	
		5.5V		–16	-8.0	µA	$0V<V_{IN}<V_{CC}$	

Notes:

[1] Port 0, 2, and 3 only.
[2] V_{SS} = 0V = GND.
[3] The device operates down to V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
[4] V_{CC} = 3.0V to 5.5V, typical values measured at V_{CC} = 3.3V and V_{CC} = 5.0V.
[5] Standard Mode (not Low EMI mode).
[6] Inputs at V_{CC} or V_{SS}, outputs unloaded.
[7] Halt mode and low EMI mode.
[8] WDT not running.
[9] TA=0˚C to 70˚C.
[10] TA=–40˚C to 105˚C.

DC ELECTRICAL CHARACTERISTICS (Continued)

Z86L02

Sym	Parameter	V_{CC}[4]	T_A = 0°C to +70°C Min	Max	Typical @25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	2.0V	$0.9V_{CC}$	V_{CC}+0.3		V	Driven by External Clock Generator	
		3.9V	$0.9V_{CC}$	V_{CC}+0.3		V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0V	V_{SS}–0.3	$0.1V_{CC}$		V	Driven by External Clock Generator	
		3.9V	V_{SS}–0.3	$0.1V_{CC}$		V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0V	$0.9V_{CC}$	V_{CC}+0.3		V		[1]
		3.9V	$0.9V_{CC}$	V_{CC}+0.3		V		[1]
V_{IL}	Input Low Voltage	2.0V	V_{SS}–0.3	$0.1V_{CC}$		V		[1]
		3.9V	V_{SS}–0.3	$0.1V_{CC}$		V		[1]
V_{OH}	Output High Voltage	2.0V	V_{CC}–0.4		3.0	V	I_{OH} = –500µA	[5]
		3.9V	V_{CC}–0.4		3.0	V	I_{OH} = –500µA	[5]
V_{OL1}	Output Low Voltage	2.0V		0.8	0.2	V	I_{OL} = +1.0 mA	[5]
		3.9V		0.4	0.1	V	I_{OL} = +1.0 mA	[5]
V_{OL2}	Output Low Voltage	2.0V		1.0	0.8	V	I_{OL} = +3.0 mA	[5]
		3.9V		0.8	0.3	V	I_{OL} = +3.0 mA	[5]
V_{OFFSET}	Comparator Input Offset Voltage	2.0V		25	10	mV		
		3.9V		25	10	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		1.4	2.15		V		
I_{IL}	Input Leakage (Input Bias Current of Comparator)	2.0V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		3.9V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	2.0V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		3.9V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range		0	V_{CC}–1.0		V		

DC ELECTRICAL CHARACTERISTICS (Continued)

Z86L02

Sym	Parameter	V_{CC}[4]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current	2.0V		3.3		mA	@2MHz	[5,6]
		3.9V		6.8		mA	@2MHz	[5,6]
		2.0V		6.0		mA	@8MHz	[5,6]
		3.9V		9.0		mA	@8MHz	[5,6]
I_{CC1}	Standby Current (Halt Mode)	2.0V		2.3		mA	@2MHz	[5,6,7]
		3.9V		3.8		mA	@2MHz	[5,6,7]
		2.0V		3.8		mA	@8MHz	[5,6,7]
		3.9V		4.8		mA	@8MHz	[5,6,7]

DC ELECTRICAL CHARACTERISTICS (Continued)
Z86L02

Sym	Parameter	V_{CC}[4]	T_A = 0°C to +70°C Min	Max	Typical @25°C	Units	Conditions	Notes
I_{CC2}	Standby Current (Stop Mode)	2.0V		10	1.0	µA		[6,7]
		3.9V		10	1.0	µA		[6,7]
I_{ALL}	Auto Latch Low Current	2.0V		12	3.0	µA	$0V<V_{IN}<V_{CC}$	
		3.9V		32	16	µA	$0V<V_{IN}<V_{CC}$	
I_{ALH}	Auto Latch High Current	2.0V		–8	-1.5	µA	$0V<V_{IN}<V_{CC}$	
		3.9V		–16	-8.0	µA	$0V<V_{IN}<V_{CC}$	

Notes:
[1] Port 0, 2, and 3 only.
[2] V_{SS} = 0V = GND.
[3] The device operates down to V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
[4] V_{CC} = 2.0V to 3.9V, typical values measured at V_{CC} = 3.3 V.
[5] Standard Mode (not Low EMI mode).
[6] Inputs at V_{CC} or V_{SS}, outputs are unloaded.
[7] WDT is not running.

DC ELECTRICAL CHARACTERISTICS (Continued)

Z86E02

Sym	Parameter	V_{CC}[4]	T_A = –40°C to +105°C T_A = 0°C to +70°C Min	Max	Typical @25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	$0.8V_{CC}$	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
		5.5V	$0.8V_{CC}$	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}–0.3	$0.2V_{CC}$	1.7	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	$0.7V_{CC}$	V_{CC}+0.3	2.8	V		
		5.5V	$0.7V_{CC}$	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	4.5V	V_{SS}–0.3	$0.2V_{CC}$	1.5	V		
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.5	V		
V_{OH}	Output High Voltage	4.5V	V_{CC}–0.4		4.8	V	I_{OH}=–2.0mA	[5]
		5.5V	V_{CC}–0.4		4.8	V	I_{OH}=–2.0mA	[5]
		4.5V	V_{CC}–0.4		4.8	V	Low Noise@I_{OH}=–0.5mA	
		5.5V	V_{CC}–0.4		4.8	V	Low Noise@I_{OH}=–0.5mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL}=+4.0 mA	[5]
		5.5V		0.4	0.1	V	I_{OL}=+4.0 mA	[5]
		4.5V		0.4	0.1	V	Low Noise@I_{OL}=1.0 mA	
		5.5V		0.4	0.1	V	Low Noise@I_{OL}=1.0 mA	
V_{OL2}	Output Low Voltage	4.5V		1.0	0.8	V	I_{OL}=+12mA	[5]
		5.5V		1.0	0.8	V	I_{OL}=+12mA	[5]
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25	10	mV		
		5.5V		25	10	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		2.6	3.3	3.0	V		[9]
			2.2	3.6	3.0	V		[10]
I_{IL}	Input Leakage (Input Bias Current of Comparator)	4.5V	–1.0	1.0		µA	V_{IN}=OV,V_{CC}	
		5.5V	–1.0	1.0		µA	V_{IN}=OV,V_{CC}	
I_{OL}	Output Leakage	4.5V	–1.0	1.0		µA	V_{IN}=OV,V_{CC}	
		5.5V	–1.0	1.0		µA	V_{IN}=OV,V_{CC}	
V_{VCR}	Comparator Input Common Mode Voltage Range		0	V_{CC}–1.0		V		[9]
			0	V_{CC}–1.5		V		[10]

DC ELECTRICAL CHARACTERISTICS (Continued)
Z86E02

Sym	Parameter	V_{CC}[4]	T_A = –40°C to +105°C / T_A = 0°C to +70°C Min	Max	Typical @25°C	Units	Conditions	Notes
I_{CC}	Supply Current	4.5V		9.0	3.8	mA	@2MHz	[5,6]
		5.5V		9.0	3.8	mA	@2MHz	[5,6]
		4.5V		15.0	4.4	mA	@8MHz	[5,6]
		5.5V		15.0	4.4	mA	@8MHz	[5,6]
I_{CC1}	Standby Current (HALT mode)	4.5V		4.0	2.5	mA	@2MHz	[5,6]
		5.5V		4.0	2.5	mA	@2MHz	[5,6]
		4.5V		5.0	3.0	mA	@8MHz	[5,6]
		5.5V		5.0	3.0	mA	@8MHz	[5,6]
I_{CC}	Supply Current (Low Noise Mode)	4.5V		9.0	3.8	mA	@1MHz	[6]
		5.5V		9.0	3.8	mA	@1MHz	[6]
		4.5V		11.0	4.0	mA	@2MHz	[6]
		5.5V		11.0	4.0	mA	@2MHz	[6]
		4.5V		15.0	4.4	mA	@4MHz	[6]
		5.5V		15.0	4.4	mA	@4MHz	[6]

DC ELECTRICAL CHARACTERISTICS (Continued)

Z86E02

Sym	Parameter	V_{CC} [4]	T_A = –40°C to +105°C / T_A = 0°C to +70°C Min	Max	Typical @25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Low Noise Halt Mode)	4.5V		4.0	2.5	mA	@1MHz	[6,7,8]
		5.5V		4.0	2.5	mA	@1MHz	[6,7,8]
		4.5V		4.5	2.7	mA	@2MHz	[6,7,8]
		5.5V		4.5	2.7	mA	@2MHz	[6,7,8]
		4.5V		5.0	3.0	mA	@4MHz	[6,7,8]
		5.5V		5.0	3.0	mA	@4MHz	[6,7,8]
I_{CC2}	Standby Current (Stop Mode)	4.5V		10	1.0	µA		[6,7,9]
		4.5V		20	1.0	µA		[6,7,10]
		5.5V		10	1.0	µA		[6,7,9]
		5.5V		20	1.0	µA		[6,7,10]
I_{ALL}	Auto Latch Low Current	4.5V		32	16	µA	$0V<V_{IN}<V_{CC}$	
		5.5V		32	16	µA	$0V<V_{IN}<V_{CC}$	
$_{ALH}$	Auto Latch High Current	4.5V		–16	-8.0	µA	$0V<V_{IN}<V_{CC}$	
		5.5V		–16	-8.0	µA	$0V<V_{IN}<V_{CC}$	

Notes:

[1] Port 0, 2, and 3 only.
[2] V_{SS} = 0V = GND.
[3] The device operates down to V_{LV} of the specified frequency for V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
[4] V_{CC} = 4.5V to 5.5V, typical values measured at V_{CC} = 5.0V.
[5] Standard Mode (not Low EMI mode).
[6] Inputs at V_{CC} or V_{SS}, outputs are unloaded.
[7] WDT not running.
[8] Halt mode and low EMI mode.
[9] TA=0˚C to 70˚C.
[10] TA=–40˚C to 105˚C.

AC ELECTRICAL CHARACTERISTICS

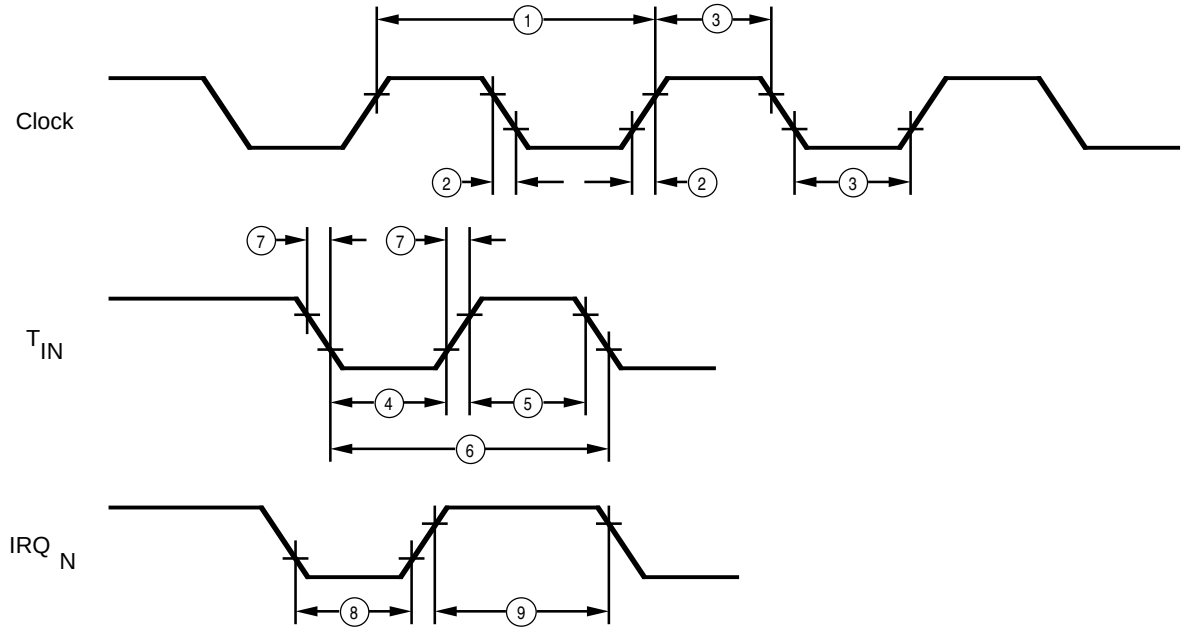


Figure 7. AC Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

				T_A = –40°C to +105°C T_A = 0°C to +70°C 8MHz			
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	2.0V	125	DC	ns	[1]
			5.5V	125	DC	ns	[1]
2	TrC,TfC	Clock Input Rise	2.0V		25	ns	[1]
		and Fall Times	5.5V		25	ns	[1]
3	TwC	Input Clock Width	2.0V	62			[1]
			5.5V	62		ns	[1]
4	TwTinL	Timer Input Low Width	2.0V	70		ns	[1]
			5.5V	70		ns	[1]
5	TwTinH	Timer Input High Width	2.0V	5TpC			[1]
			5.5V	5TpC			[1]
6	TpTin	Timer Input Period	2.0V	8TpC			[1]
			5.5V	8TpC			[1]
7	TrTin,	Timer Input Rise	2.0V		100	ns	[1]
	TfTin	and Fall Timer	5.5V		100	ns	[1]
8	TwIL	Int. Request Input	2.0V	70		ns	[1,2,3]
		Low Time	5.5V	70		ns	[1,2,3]
9	TwIH	Int. Request Input	3.0V	5TpC			[1,2,3]
		High Time	5.5V	5TpC			[1,2,3]
10	Twdt	Watch-Dog Timer	2.0V	25		ms	
		Delay Time Before	3.0V	10		ms	
		Time-Out	5.5V	5		ms	
11	Tpor	Power-On	2.0V	70	250	ms	
		Reset Time	3.0V	50	150	ms	
			5.5V	10	70	ms	

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

[2] Interrupt request through Port 3 (P33-P31).

[3] IRQ 0,1,2 only.

AC ELECTRICAL CHARACTERISTICS

Low Noise Mode (Z86C02/E02 Only)

				$T_A = -40°C$ to $+105°C$ $T_A = 0°C$ to $+70°C$ 1MHz		4MHz			
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TPC	Input Clock Period	3.0V	1000	DC	250	DC	ns	[1]
			5.5V	1000	DC	250	DC	ns	[1]
2	TiC	Clock Input Rise	3.0V		25		25	ns	[1]
	TfC	and Fall Times	5.5V		25		25	ns	[1]
3	TwC	Input Clock Width	3.0V	500		125		ns	[1]
			5.5V	500		125			[1]
4.	TwTinL	Timer Input Low Width	3.0V	70		70		ns	[1]
			5.5V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.0V	2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC			[1]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			[1]
			5.5V	4TpC		4TpC			[1]
7	TrTin,	Timer Input Rise	3.0V		100		100	ns	[1]
	TfTin	and Fall Timer	5.5V		100		100	ns	[1]
8	TwIL	Int. Request Input	3.0V	70		70		ns	[1,2,3]
		Low Time	5.5V	70		70		ns	[1,2,3]
9	TwIH	Int. Request Input	3.0	2.5TpC		2.5TpC			[1,2,3]
		High Time	5.5V	2.5TpC		2.5TpC			[1,2,3]
10	Tpor	Power-On Reset Time	3.0V	50	150	50	150	ms	
			5.5V	10	70	10	70	ms	
11	Twdt	Watch-Dog Timer Delay	3.0V	10		10		ms	
			5.5V	5		5		ms	

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.Power-On Reset Time

[2] Interrupt request through Port 3 (P33-P31).

[3] IRQ 0,1,2 only.

LOW NOISE VERSION

Low EMI Emission

The Z8® can be programmed to operate in a Low EMI emission mode by means of a mask ROM bit option (Z86C02) or OTP bit option (Z86E02). Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI mode is mask-programmable to be selected by the customer at the time the ROM Code is submitted (for Z86C02 only).

PRECAUTION:

1. Stack pointer register (sph) at FFHex and general purpose register at FEHex are set to 00Hex after reset.

PIN FUNCTIONS

OTP Programming Mode

D7-D0 *Data Bus.* Data can be read from, or written to the EPROM through this data bus.

V_{CC} *Power Supply.* It is 5V during EPROM Read Mode and 6V during the other modes (Program, Program Verify, etc.).

/CE *Chip Enable* (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

/OE *Output Enable* (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input. This pin must toggle for each data output read.

EPM *EPROM Program Mode.* This pin controls the different EPROM Program Modes by applying different voltages.

V_{PP} *Program Voltage.* This pin supplies the program voltage.

Clear *Clear* (active High). This pin resets the internal address counter at the High Level.

Clock *Address Clock.* This pin is a clock input. The internal address counter increases by one with one clock cycle.

/PGM *Program Mode* (active Low). A Low level at this pin programs the data to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if ***excessive noise*** surges above V_{cc} occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by ***excessive noise*** surges on the V_{pp}, /CE, /EPM, /OE pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{CC}
- Adding a capacitor to the affected pin.

STANDARD MODE

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, RC, or an external single-phase clock (8 MHz max) to the on-chip clock oscillator and buffer.

Port 0, P02-P00. Port 0 is a 3-bit bi-directional, Schmitt-triggered CMOS compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs (Figure 9).

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. On Power-up and Reset, the Auto Latch will set the ports to an undetermined state of 0 or 1. Default condition is Auto Latches enabled.

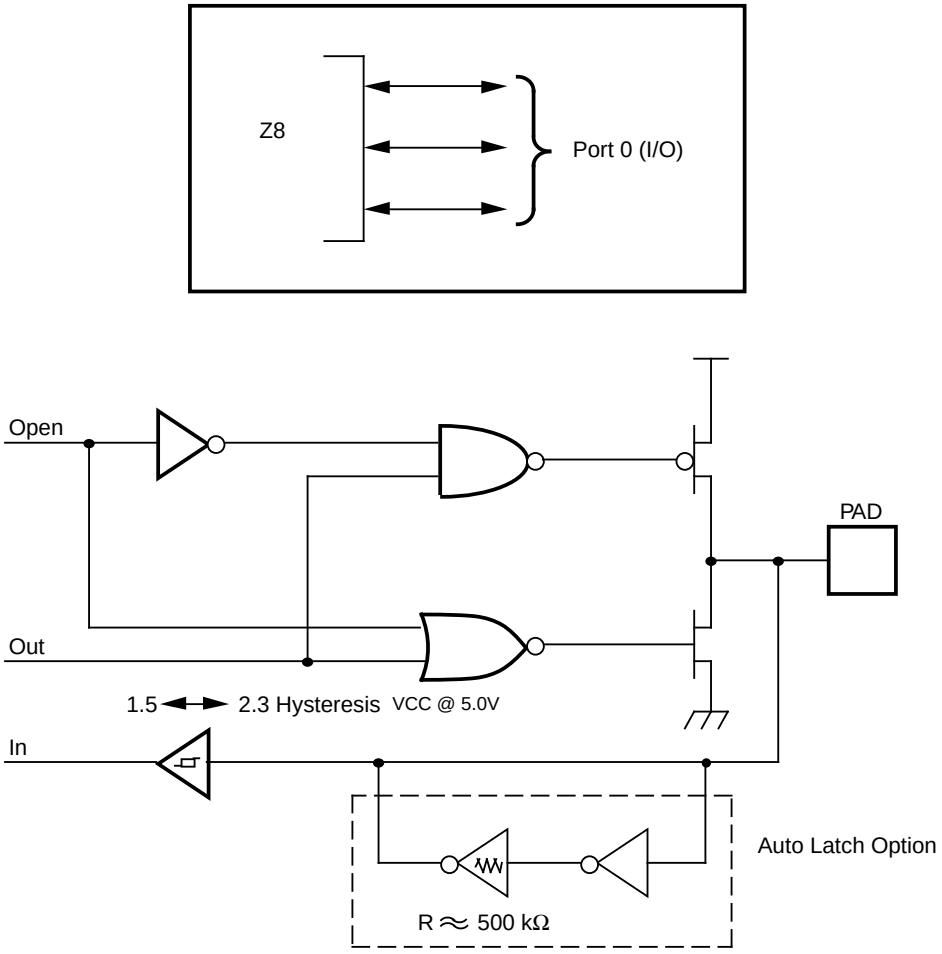


Figure 9. Port 0 Configuration

Port 2, P27-P20. Port 2 is an 8-bit, bit programmable, bi-directional, Schmitt-triggered CMOS compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 10).

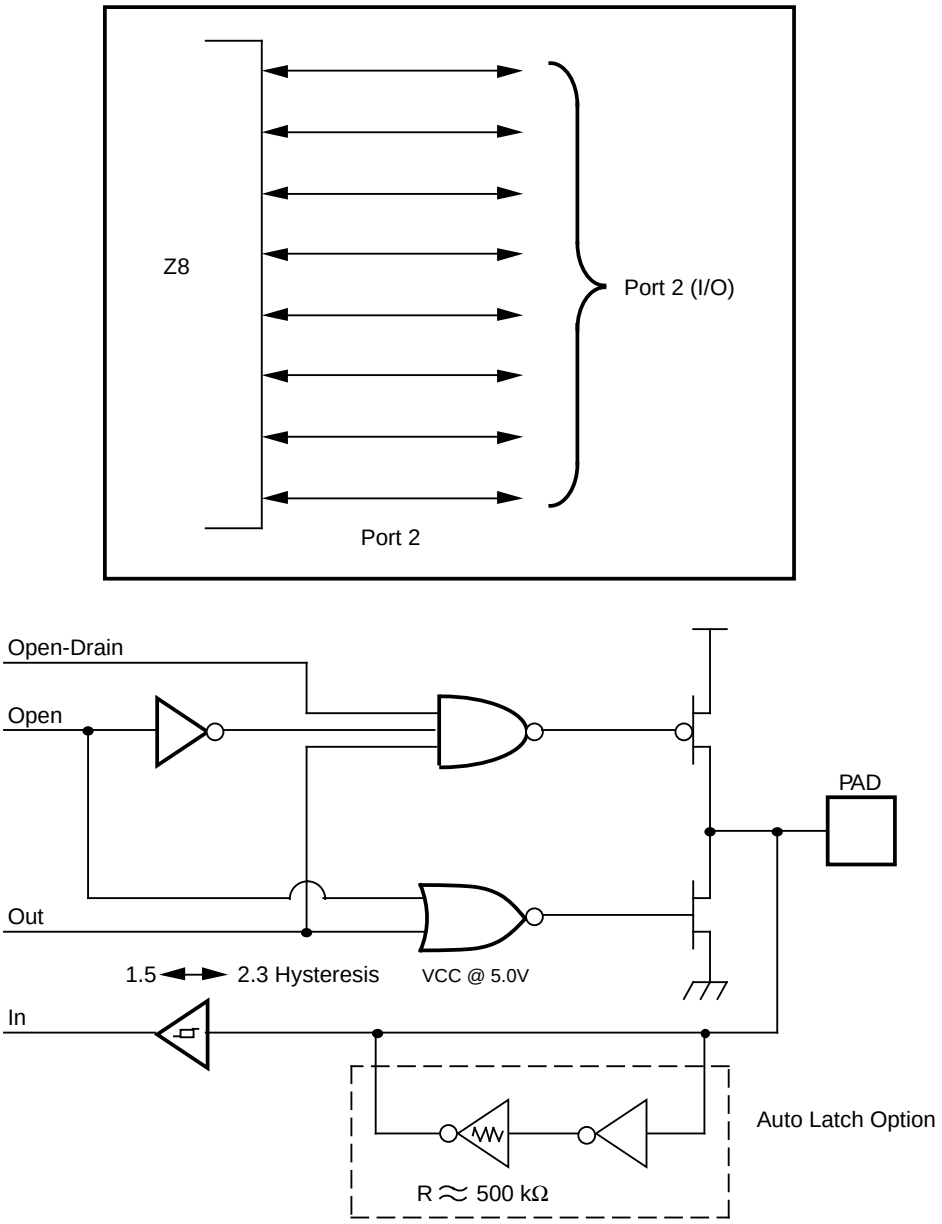


Figure 10. Port 2 Configuration

Standard Mode (Continued)

Port 3, P33-P31. Port 3 is a 3-bit, CMOS compatible port with three fixed input (P33-P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs or analog inputs. These three input lines are also used as the interrupt sources IRQ0-IRQ3 and as the timer input signal T_{IN} (Figure 11).

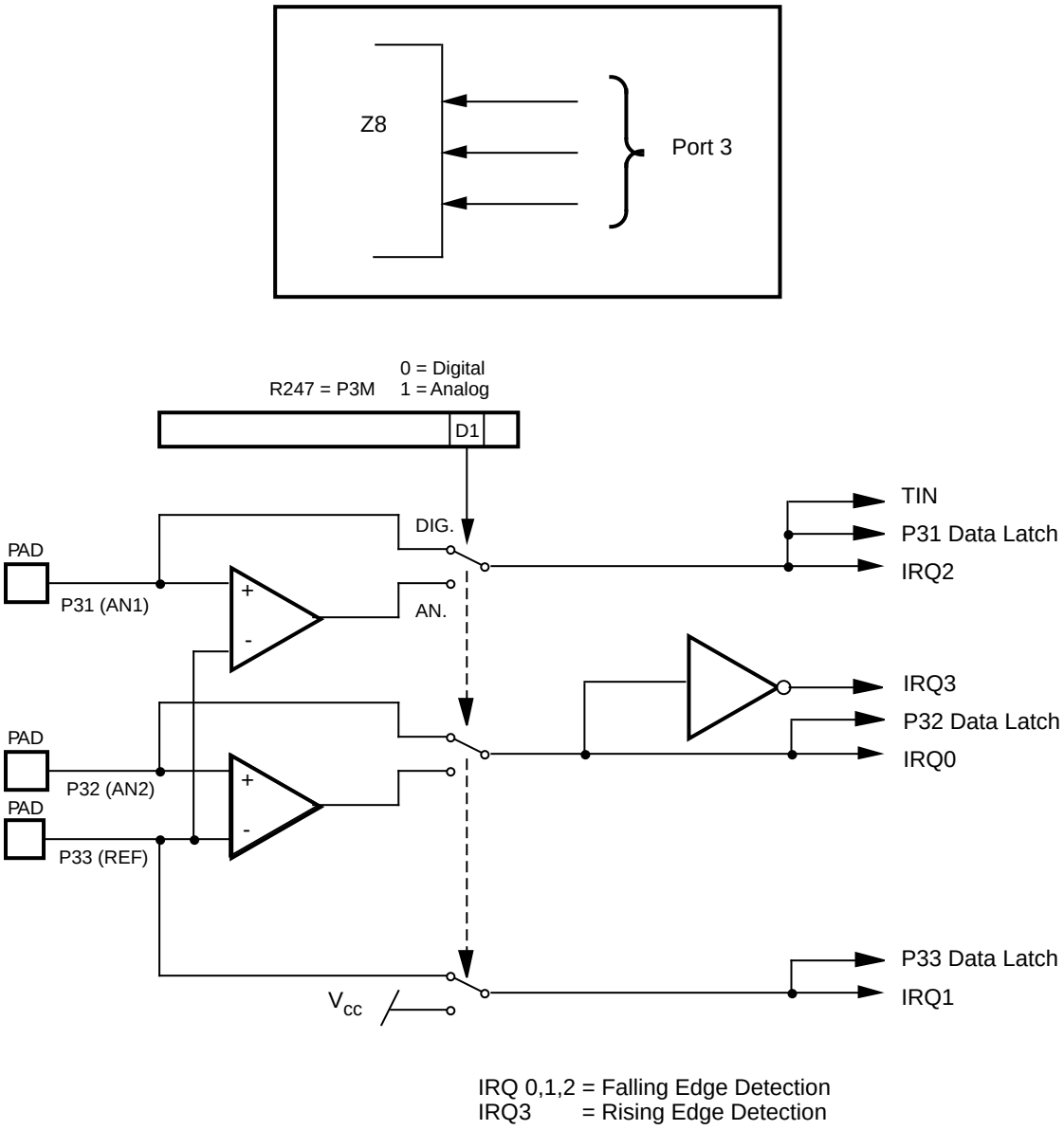


Figure 11. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to input of Port 3, P31 and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In analog mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP mode. The common voltage range is 0-4 V when the V_{CC} is 5.0 V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z86C02/E02/L02 devices to enhance the standard Z8® core architecture to provide the user with increased design flexibility.

RESET. This function is accomplished by means of a Power-On Reset or a Watch-Dog Timer Reset. Upon power-up, the Power-On Reset circuit waits for T_{POR} ms, plus 18 clock cycles, then starts program execution at address 000C (Hex) (Figure 12). The control registers' reset value is shown in Table 3.

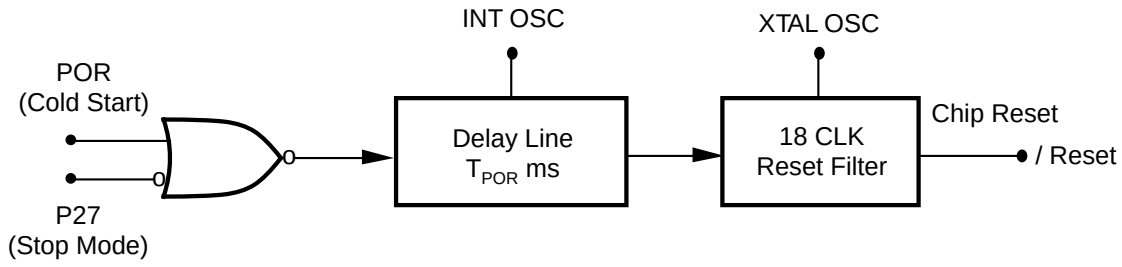


Figure 12. Internal Reset Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power bad to power good status
- Stop-Mode Recovery
- WDT time-out
- WDH time-out (in Halt Mode)
- WDT time-out (in Stop Mode)

Watch-Dog Timer Reset. The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator. If the permanent WDT option is selected then the WDT is enabled after reset and operates in run mode, halt mode, stop mode and can not be disabled. If the permenent WDT option is not selected then the WDT, when enabled by the user's software, does not operate in stop mode but it can operate in halt mode by using a WDH instruction

FUNCTIONAL DESCRIPTION (Continued)

Table 3. Control Registers

		Reset Condition								
Addr.	**Reg.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Comments**
FF	SPL	0	0	0	0	0	0	0	0	
FE	GPR	0	0	0	0	0	0	0	0	
FD	RP	0	0	0	0	0	0	0	0	
FC	FLAGS	U	U	U	U	U	U	U	U	
FB	IMR	0	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9	IPR	U	U	U	U	U	U	U	U	
F8	P01M	U	U	U	0	U	U	0	1	
F7*	P3M	U	U	U	U	U	U	0	0	P2 Open Drain
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F3	PRE1	U	U	U	U	U	U	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F1	TMR	0	0	0	0	0	0	0	0	

Note:

* Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 4 and the user must avoid bus contention on the port pins or it may affect device reliability.

Program Memory. The Z8 addresses up to 512 bytes of internal program memory (Figure 13). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-511 are on-chip one-time programmable ROM.

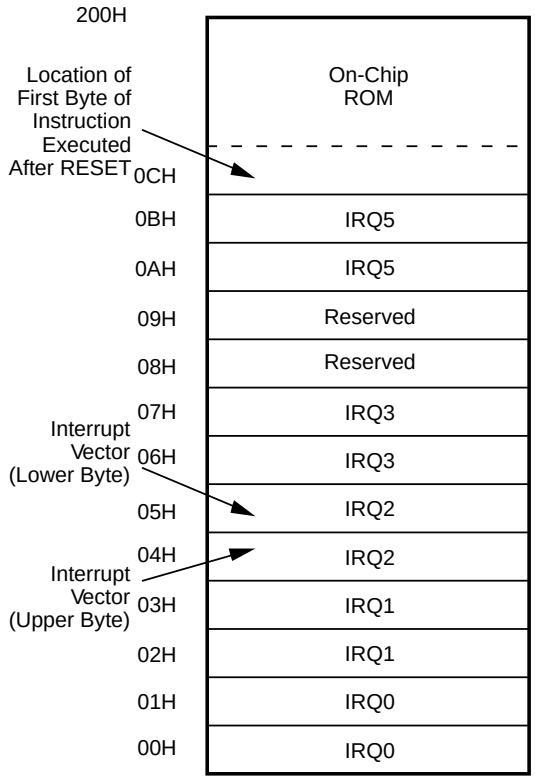


Figure 13. Program Memory Map

Register File. The Register File consists of three I/O port registers, 61 general-purpose registers, and 12 control and status registers R0-R3, R4-R127 and R241-R255, respectively (Figure 14). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8. The instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 15) addresses the starting location of the active working-register group.

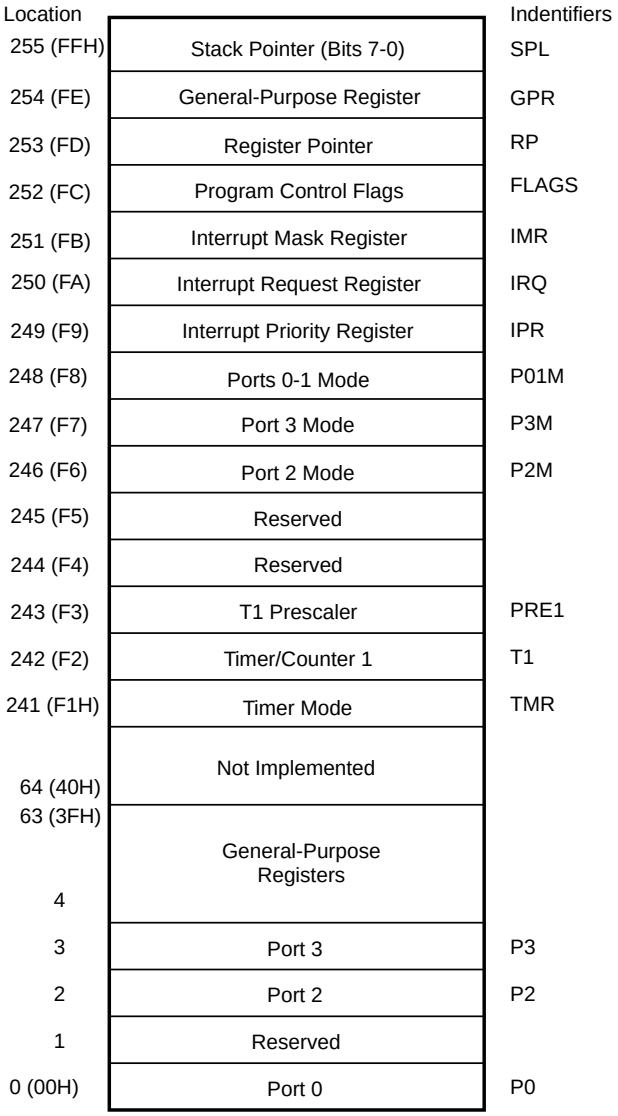


Figure 14. Register File

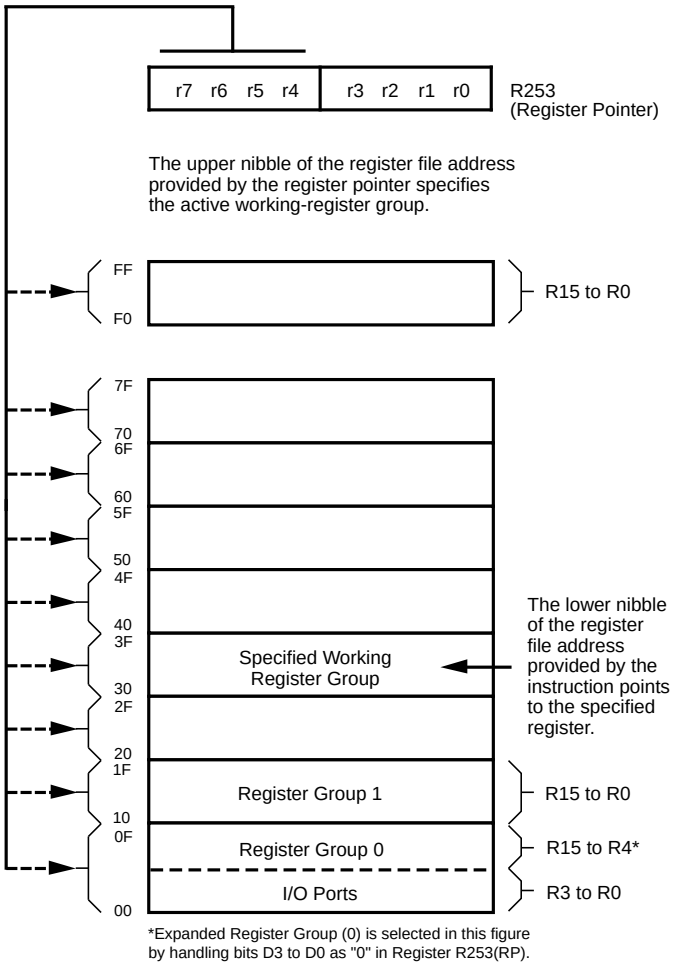


Figure 15. Register Pointer

FUNCTIONAL DESCRIPTION (Continued)

Stack Pointer. The Z8 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 60 general-purpose registers. It is set to 00Hex after any reset.

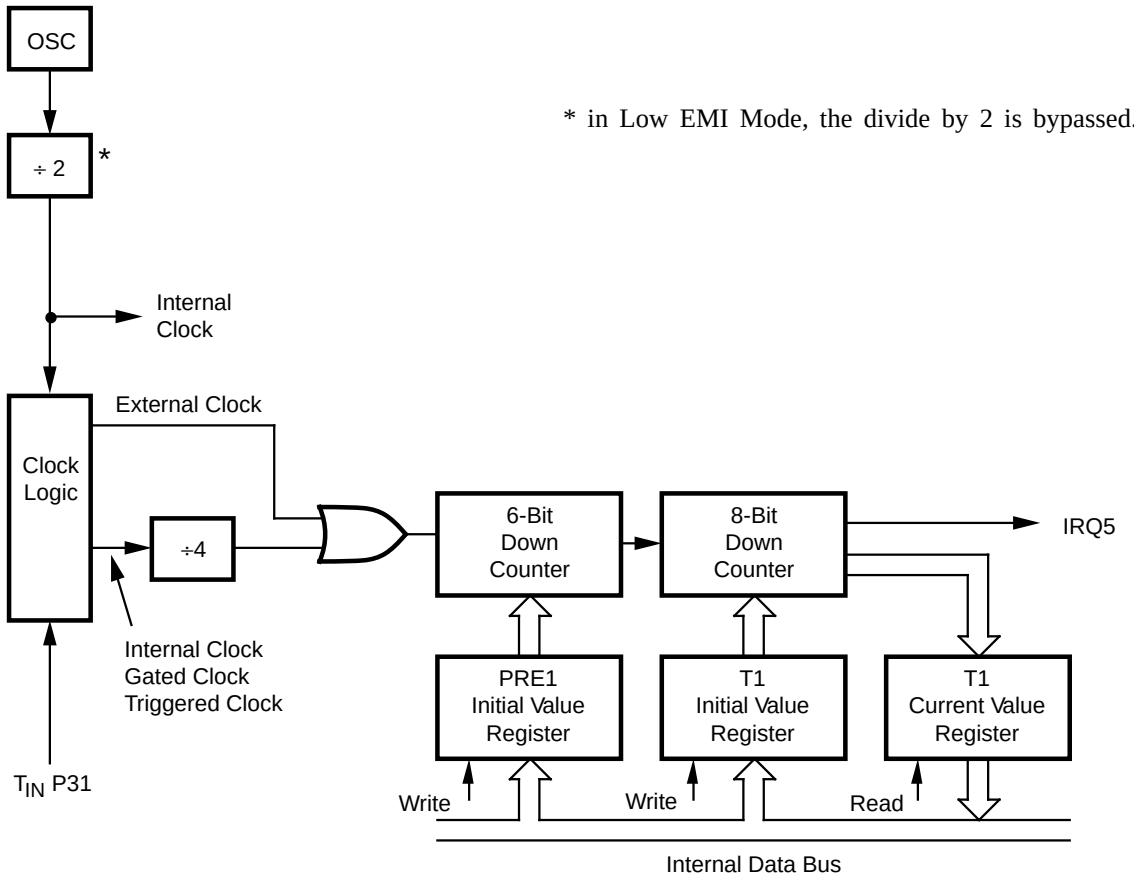
General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register. But is set to 00Hex after any reset.

Counter/Timer. There is an 8-bit programmable counter/timers (T1), each driven by its 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources. (Figure 16).

The 6-bit prescaler divide the input frequency of the clock source by any integer number from 1 to 64. The prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counter, but not the prescaler, is read at any time without disturbing it's value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.



* in Low EMI Mode, the divide by 2 is bypassed.

Figure 16. Counter/Timers Block Diagram

Interrupts. The Z8 has five interrupts from four different sources. These interrupts are maskable and prioritized (Figure 17). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and one counter/timer. The Interrupt Mask Register globally or individually enables or disables the five interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Note: User must select any Z86E08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not directly supported on the Z86CCP00ZEM emulator. Please refer to Emulator User's Manual for workaround.

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F)Edge
IRQ1	REF(P33)	2,3	External (F)Edge
IRQ2	AN1(P31)	4,5	External (F)Edge
IRQ3	AN2(P32)	6,7	External (R)Edge
IRQ4	Reserved	8,9	Reserved
IRQ5	T1	10,11	Internal

Notes:
F = Falling edge triggered
R = Rising edge triggered

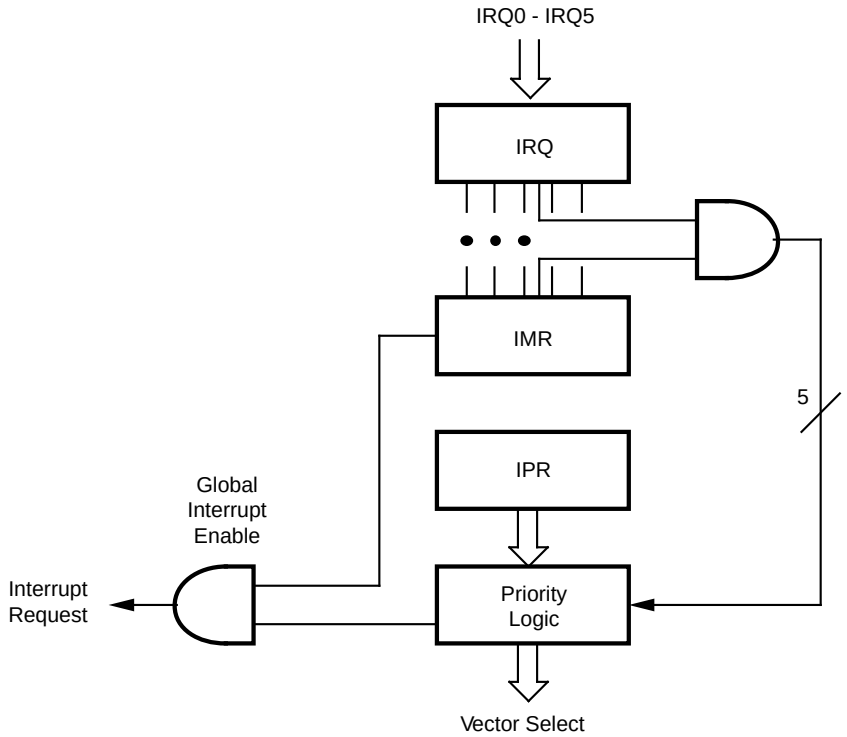


Figure 17. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT cut, 8 MHz max, with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal or ceramic resonator should be connected across XTAL1 and XTAL2 using the vendors crystal or ceramic resonator recommended capacitors from each pin directly to device ground pin 14 (Figure 18). Note that the crystal capacitor loads should be connected to V_{SS}, Pin 14 to reduce Ground noise injection.

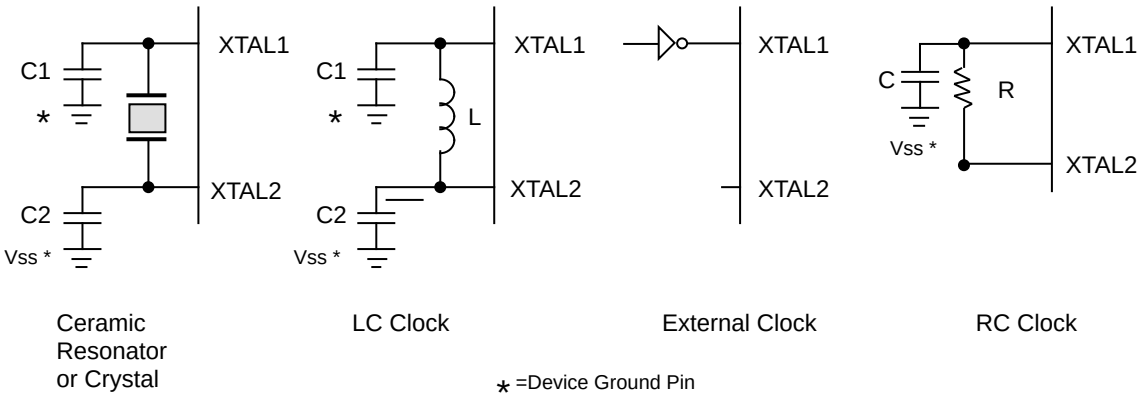


Figure 18. Oscillator Configuration

HALT Mode. This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timer and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA. The STOP mode is released by a RESET through a Stop-Mode Recovery (pin P27). A Low input condition on P27 releases the STOP mode. Program execution begins at location 000C(Hex). However, when P27 is used to release the STOP mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP mode, use the following instruction:

```
LD      P2M,#1XXXXXXXB
NOP
STOP
```

X = Dependent on user's application.

Note: Stop-Mode Recovery pin P27 is not edge triggered

In order to enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate SLEEP instruction, i.e.:

```
FF    NOP   ;  clear the pipeline
6F    STOP  ;  enter STOP mode
or
FF    NOP   ;  clear the pipeline
7F    HALT  ;  enter HALT mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 Twdt period; otherwise, the controller resets itself, The WDT instruction affects the flags accordingly; Z=1, S=0, V=0.

WDT = 5F (Hex)

Opcode WDT (5FH). The first time opcode 5FH is executed, the WDT is enabled and subsequent execution clears the WDT counter. This must be done at least every T_{WDT}; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of T_{POR}, plus 18 XTAL clock cycles.The WDT does not run in stop mode, unless the permanent WDT enable option is selected. The WDT does not run in halt mode unless WDH instruction is executed or permanent WDT enable option is selected.

Opcode WDH (4FH). When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT running during HALT mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Note: Opcode WDH and permanently enabled WDT is not directly supported by the Z86CCP00ZEM. Please refer to Emulator User's Manual for workaround.

Auto Reset Voltage (V_{LV}). The Z8 has an auto-reset built-in. The auto-reset circuit resets the Z8 when it detects the V_{CC} below V_{LV}. Figure 19 shows the Auto Reset Voltage versus temperature.

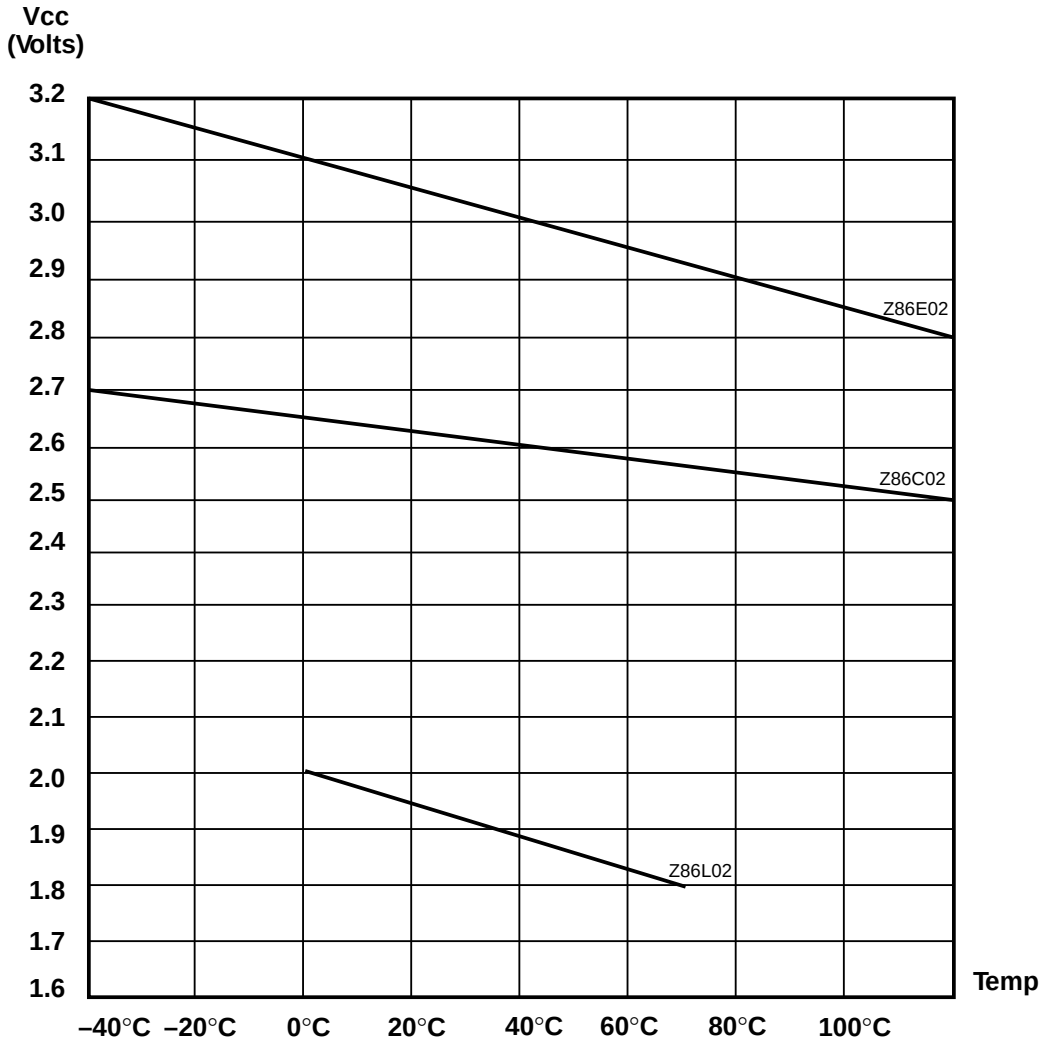


Figure 19. Typical Auto Reset Voltage (V_{LV}) vs Temperature

FUNCTIONAL DESCRIPTION (Continued)

Options

The Z86C02/E02/L02 offers ROMprotect, Low Noise, Auto Latch Disable, RC Oscillator, and Permanent WDT enable features as options.

Low Noise. The Z8 can operate in a low EMI emission mode by selecting low noise option. Use of this feature results in:

- All drivers slew rates reduced to 10 ns (typical).
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

ROM Protect. ROM Protect fully protects the Z8 ROM code from being read externally. When ROM Protect is selected, the instructions LDC and LDCI **are supported** dose not support the instructions of LDE and LDEI).

Auto Latch Disable. Auto Latch Disable option when Selected will globally disable all Auto Latches.

RC. RC Oscillator option when selected will allow using a resistor (R) and a capacitor (C) as a clock source.

WDT Enable. WDT Enable option bit when selected will have the WDT permanently enabled in all modes and can not be stopped in Halt or Stop Mode.

EPROM Mode Description. In addition to V_{DD} and GND (V_{SS}), the Z8 changes all its pin functions in the EPROM mode. XTAL2 has no function, XTAL1 functions as /CE, P31 functions as /OE, P32 functions as EPM, P33 functions as V_{PP}, and P02 functions as /PGM.

Please note that when using the device in a noisy environment, it is suggested that the voltages on the EPM and CE pins be clamped to V_{CC} through a diode to V_{CC} to prevent accidentally entering the OTP mode. The V_{PP} requires both a diode and a 100 pF capacitor.

User Modes. Table 5 shows the programming voltage of each mode of Z86E02.

Table 5. EPROM Programming Table

Programming Modes	V_{PP}	EPM	/CE	/OE	/PGM	ADDR	DATA	V_{CC}*
EPROM READ	NU	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.0V
PROGRAM	V_H	V_{IH}	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.4V
PROGRAM VERIFY	V_H	V_{IH}	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.4V
ROM PROTECT	V_H	V_H	V_H	V_{IH}	V_{IL}	NU	NU	5.0-6.4V
LOW NOISE SELECT	V_H	V_{IH}	V_H	V_{IH}	V_{IL}	NU	NU	5.0-6.4V
AUTO LATCH DISABLE	V_H	V_{IL}	V_H	V_{IL}	V_{IL}	NU	NU	5.0-6.4V
WDT ENABLE	V_H	V_{IL}	V_H	V_{IH}	V_{IL}	NU	NU	5.0-6.4V

Notes:
V_H = 13.0V ±0.25 V_{DC}.
V_{IH} = As per specific Z8 DC specification.
V_{IL} = As per specific Z8 DC specification.
X = Not used, but must be set to V_H, V_{IH}, or V_{IL} level.
NU = Not used, but must be set to either V_{IH} or V_{IL} level.
I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum.
* V_{CC} has a tolerance of ±0.25V.

Internal Address Counter. The address of Z86E02 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 20 shows the setup time of the serial address input.

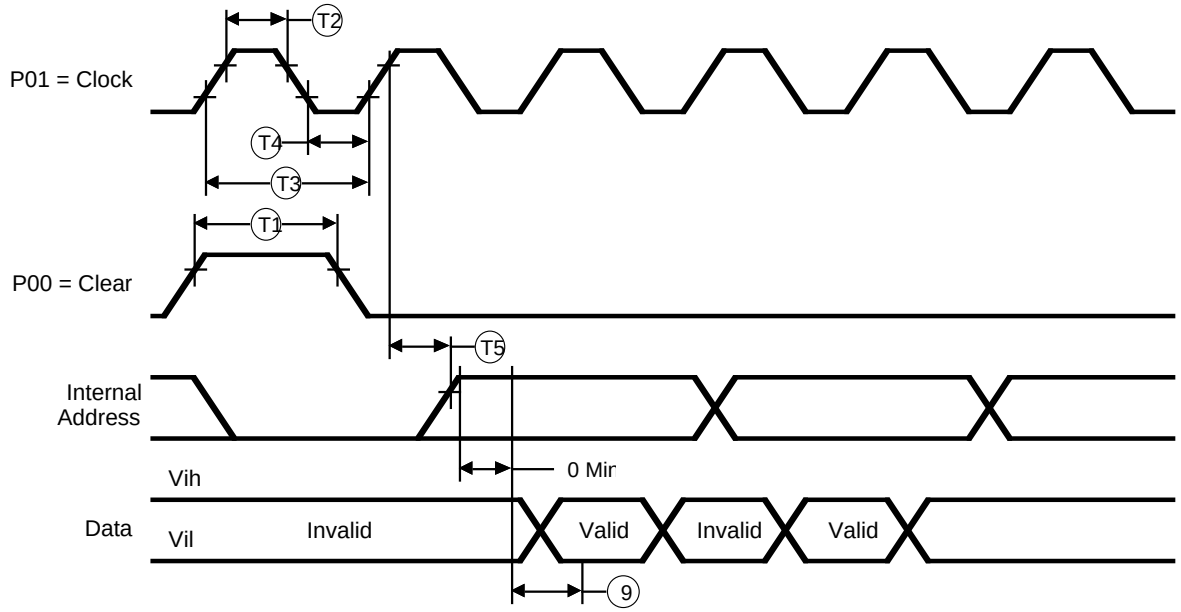
Programming Waveform. Figures 21, 22 and 23 show the programming waveforms of each mode. Table 6 shows the timing of programming waveforms.

Programming Algorithm. Figure 25 shows the flow chart of the Z86E02 programming algorithm.

Table 6. Z86E02Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time	188	4000	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85	3.2	ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	150		ms
16	/OE Low Width	250		ns

FUNCTIONAL DESCRIPTION (Continued)



Legend:	
T1 Reset Clock Width	30 ns Min
T2 Input Clock High	30 ns Min
T3 Input Clock Period	70 ns Min
T4 Input Clock Low	30 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max

Figure 20. Z86E02 Address Counter Waveform

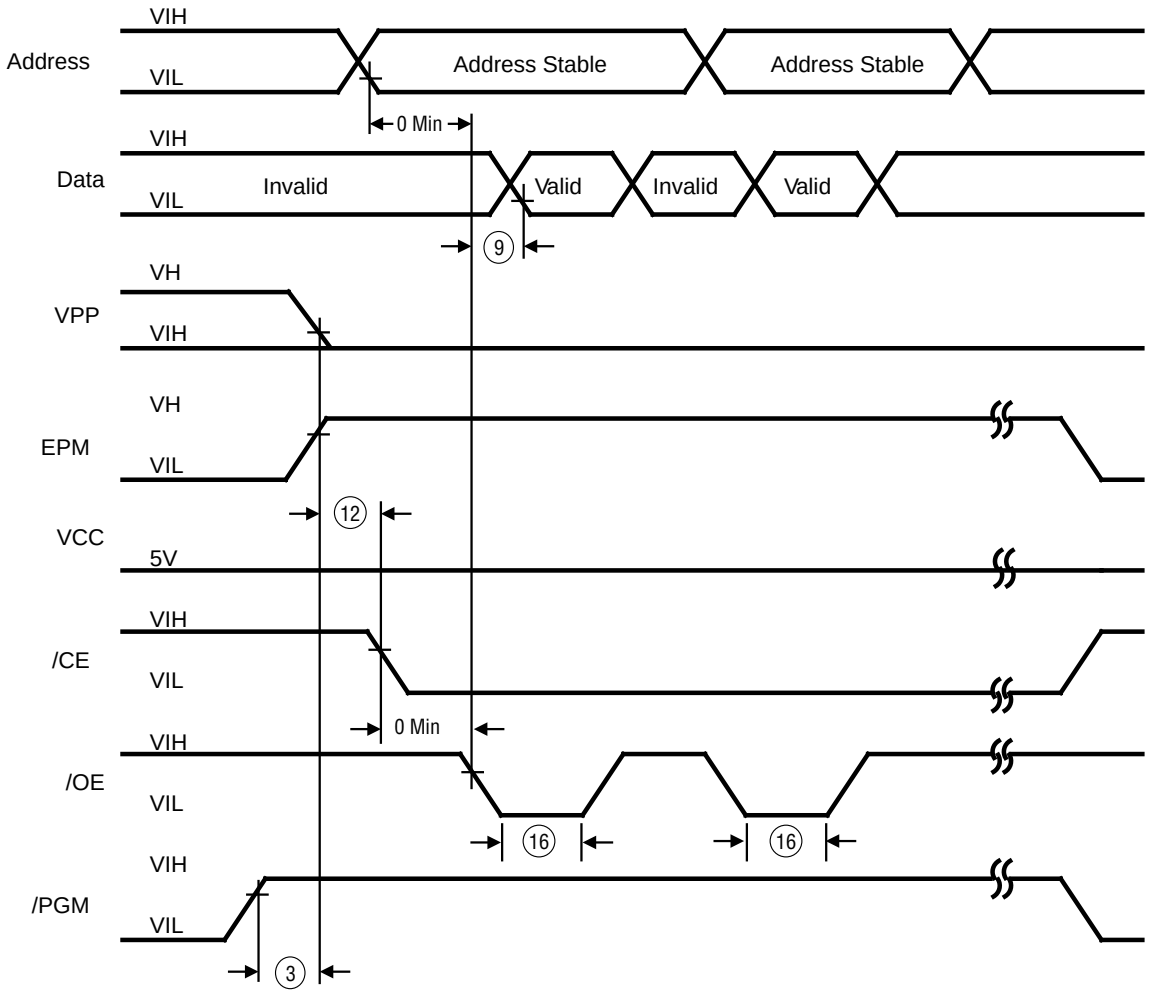


Figure 21. Z86E02 Programming Waveform (EPROM Read)

FUNCTIONAL DESCRIPTION (Continued)

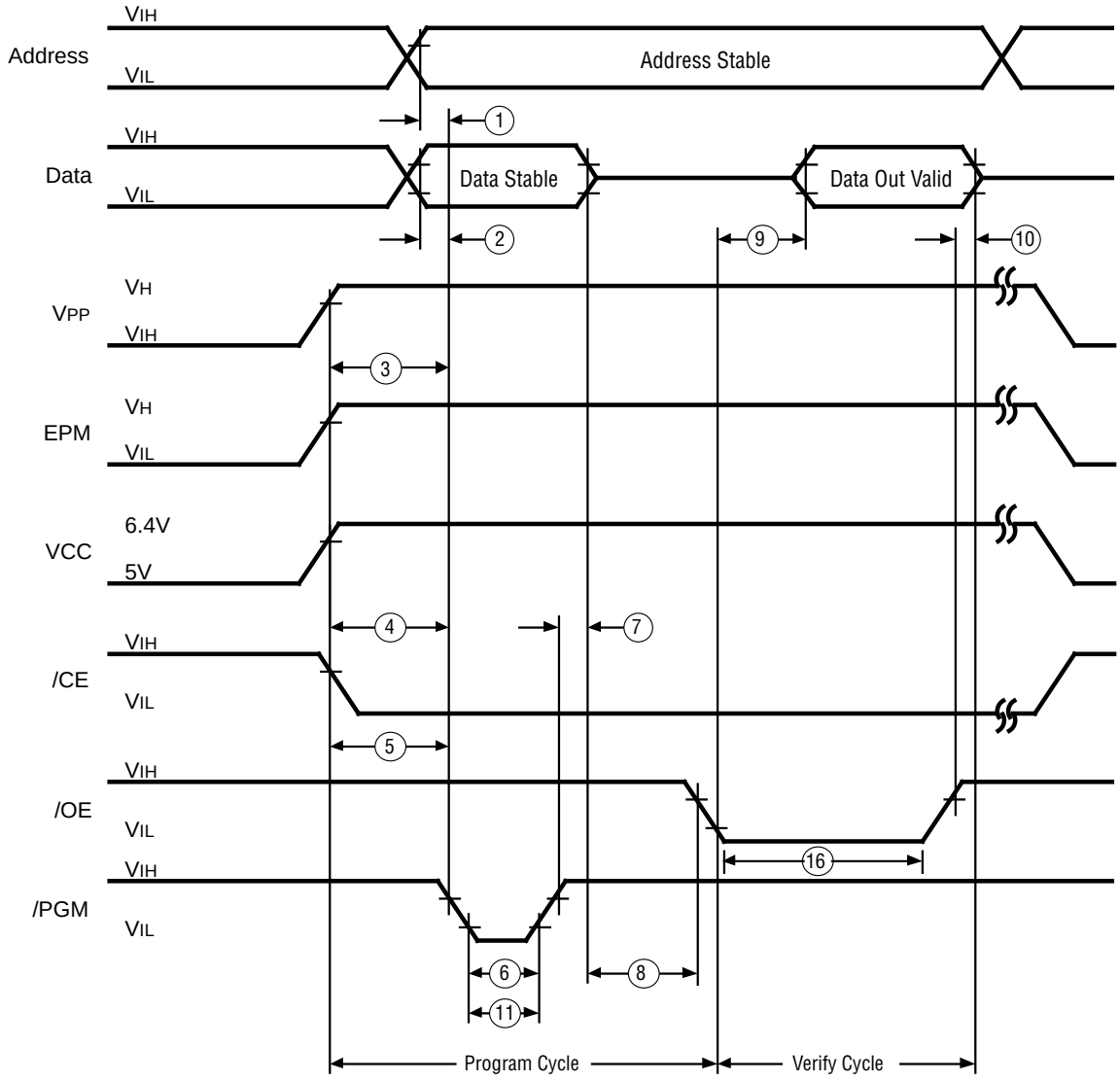


Figure 22. Z86E02 Programming Waveform (Program and Verify)

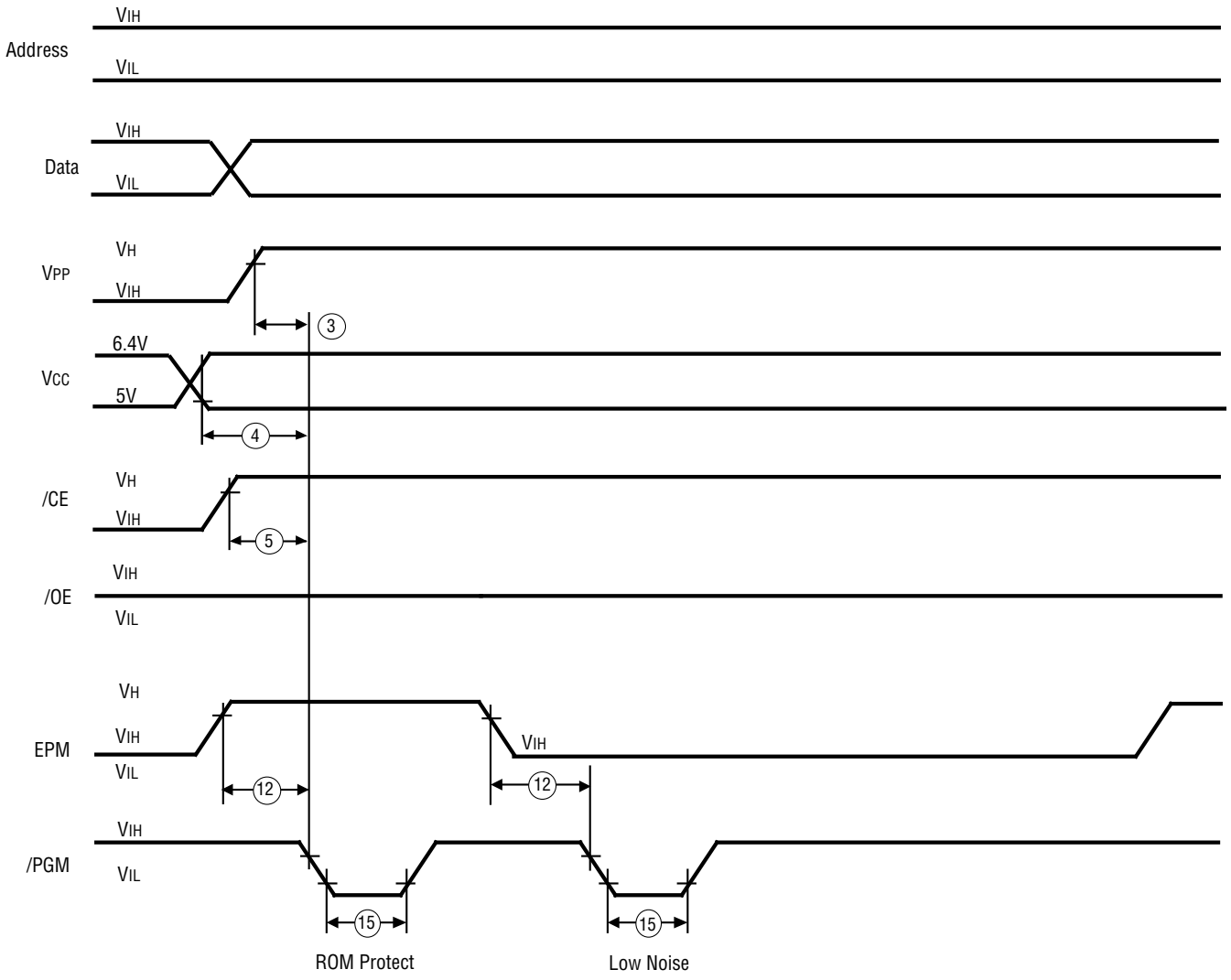


Figure 23. Z86E02 Programming Options Waveform (ROM Protect and Low Noise Program)

FUNCTIONAL DESCRIPTION (Continued)

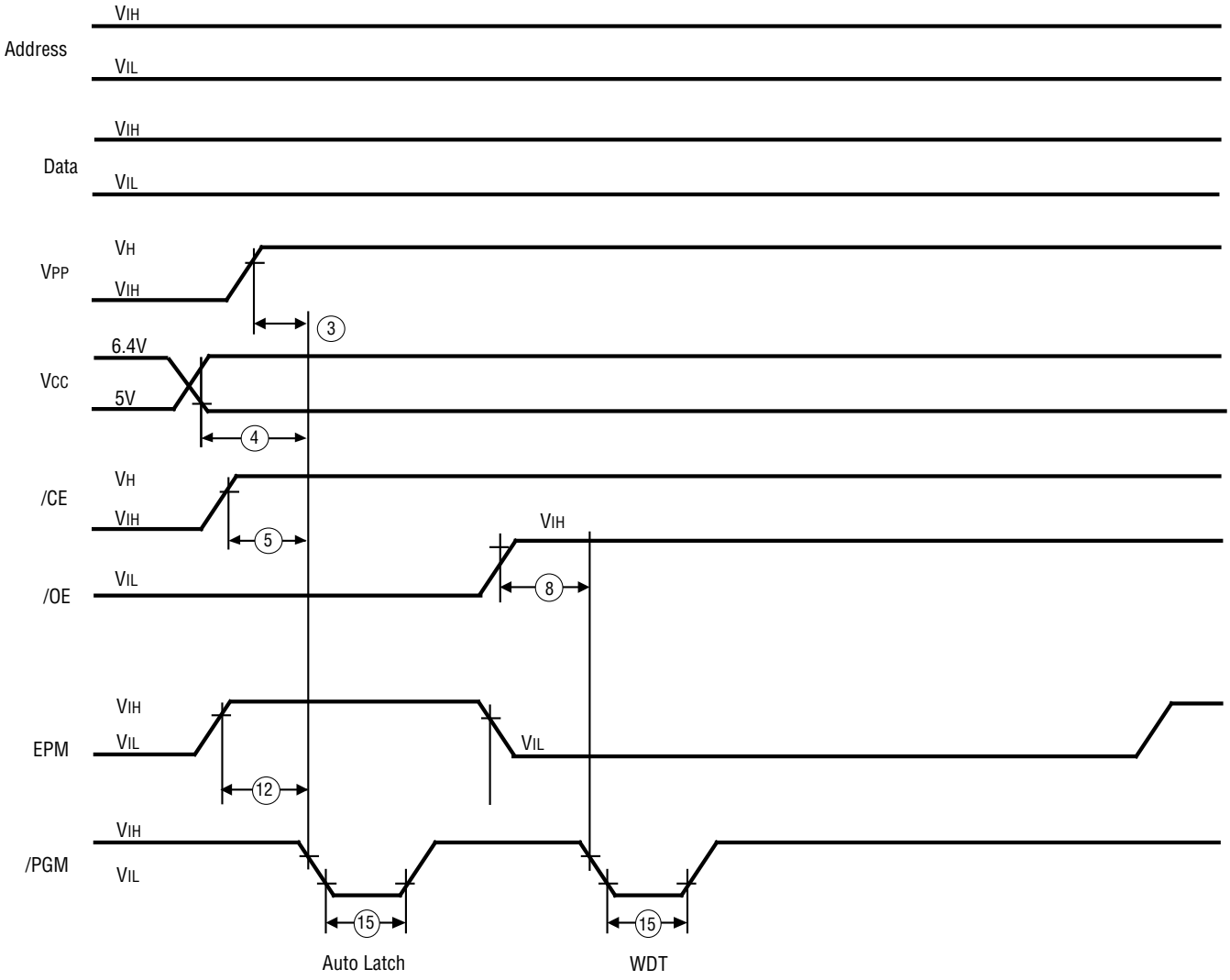


Figure 24. Z86E02 Programming Options Waveform (Auto Latch Disable and Permanent WDT Enable)

FUNCTIONAL DESCRIPTION (Continued)

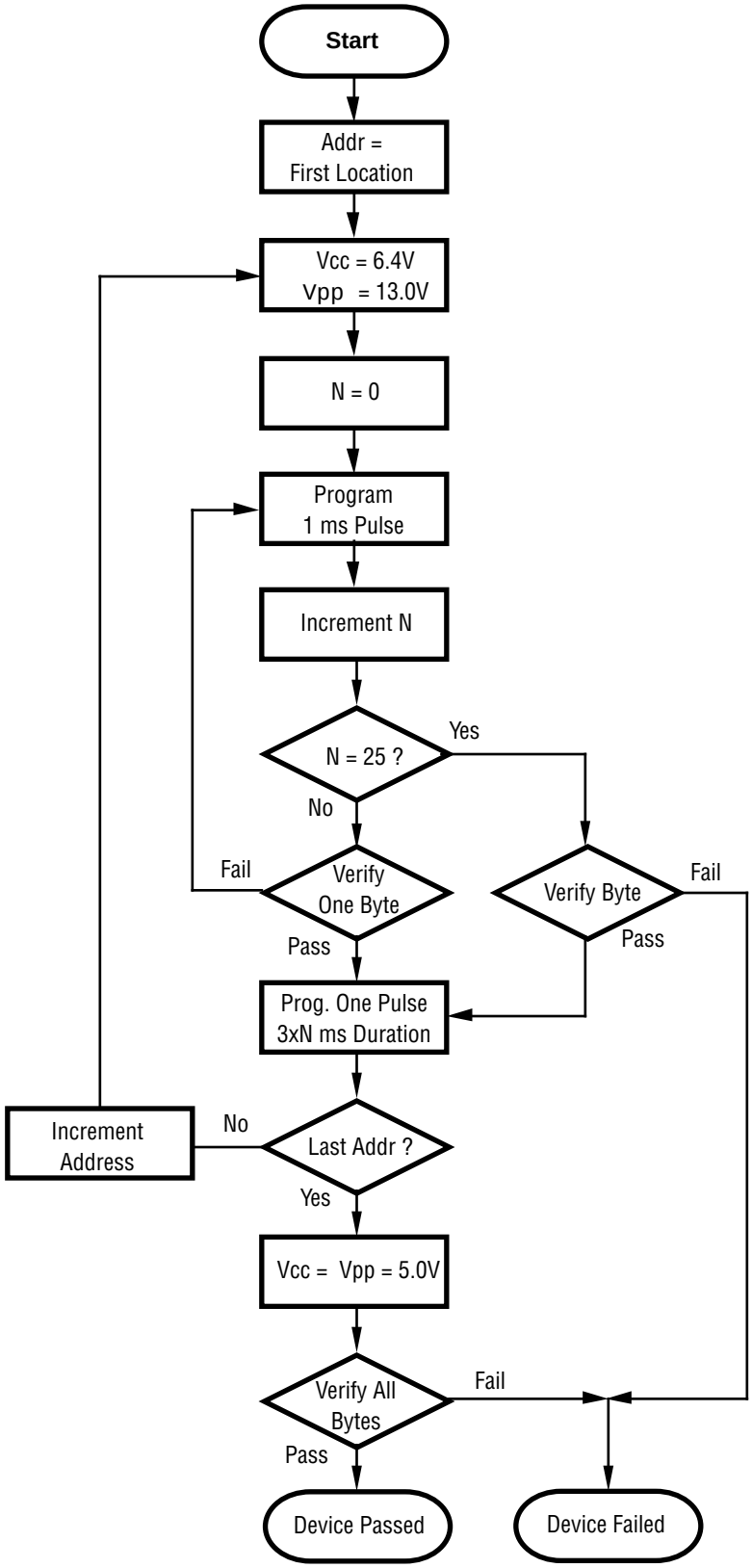


Figure 25. Z86E02 Programming Algorithm

Z8 CONTROL REGISTERS

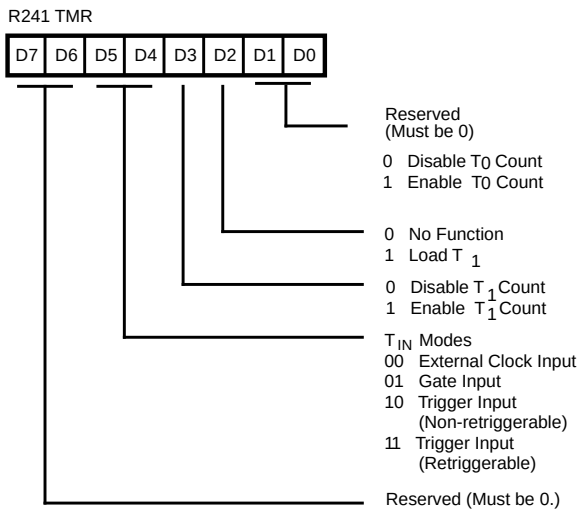


Figure 26. Timer Mode Register ($F1_H$: Read/Write)

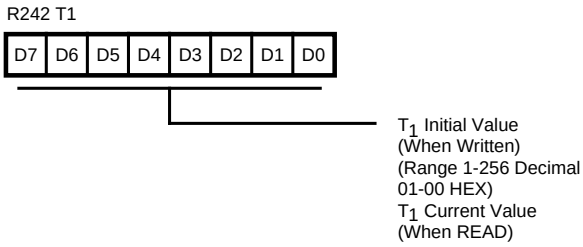


Figure 27. Counter Timer 1 Register ($F2_H$: Read/Write)

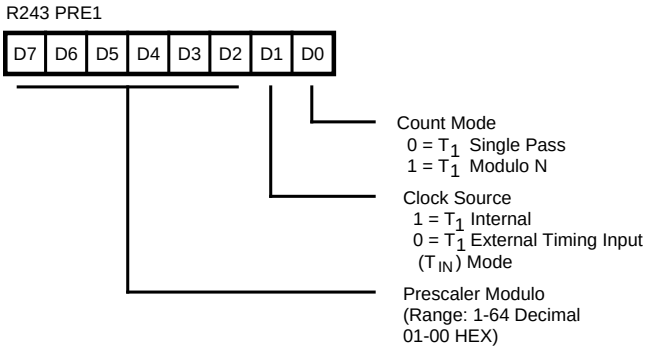


Figure 28. Prescaler 1 Register ($F3_H$: Write Only)

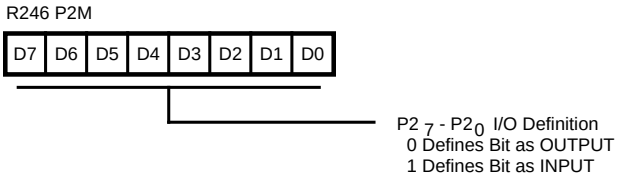


Figure 29. Port 2 Mode Register ($F6_H$: Write Only)

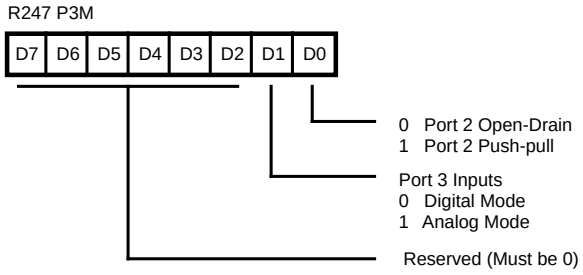


Figure 30. Port 3 Mode Register ($F7_H$: Write Only)

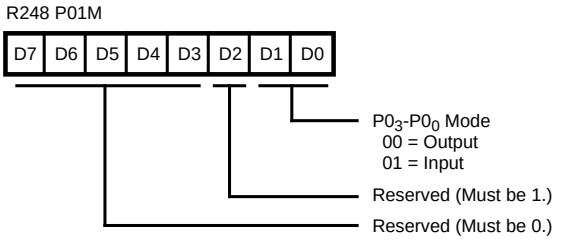


Figure 31. Port 0 and 1 Mode Register ($F8_H$: Write Only)

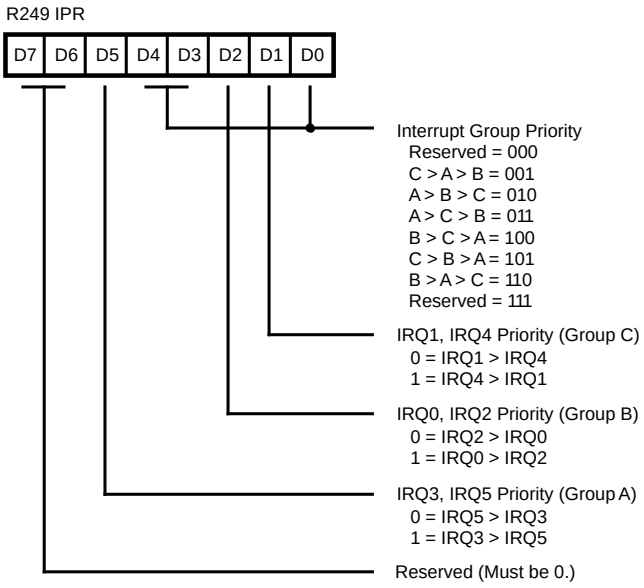


Figure 32. Interrupt Priority Register ($F9_H$: Write Only)

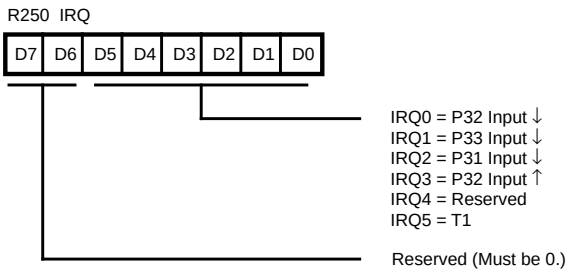


Figure 33. Interrupt Request Register (FA_H: Read/Write)

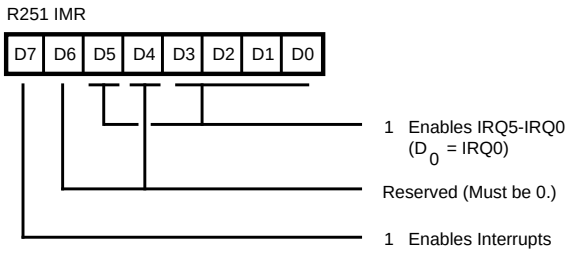


Figure 34. Interrupt Mask Register (FB_H: Read/Write)

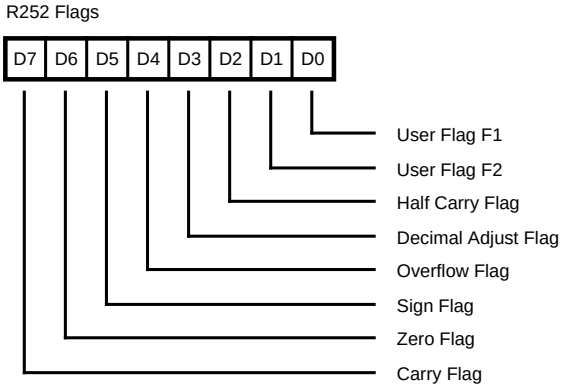


Figure 35. Flag Register (FC_H: Read/Write)

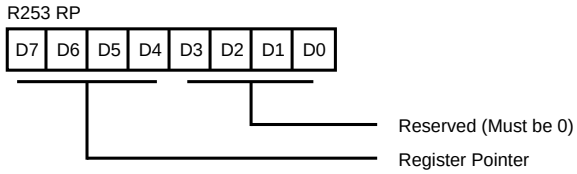


Figure 36. Register Pointer (FD_H: Read/Write)

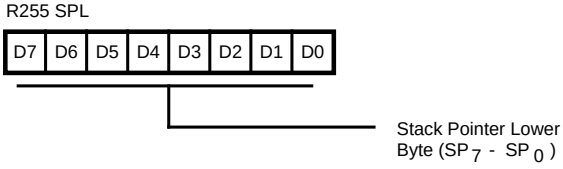


Figure 37. Stack Pointer (FF_H: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Ir	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack pointer
PC	Program counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags.

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

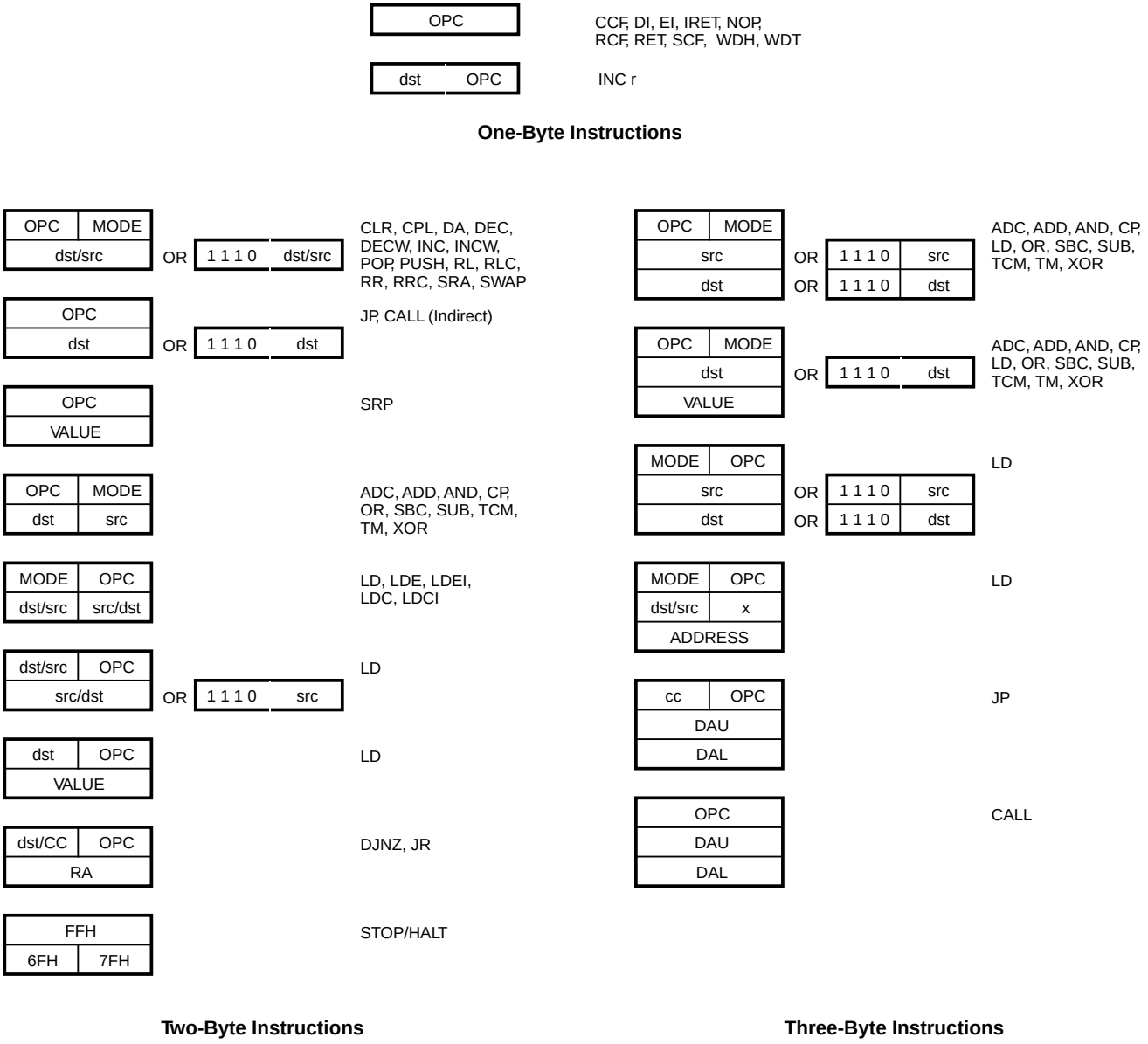
Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
X	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000	—	Always true	—
0111	C	Carry	C=1
1111	NC	No Carry	C=0
0110	Z	Zero	Z=1
1110	NZ	Not zero	Z=0
1101	PL	Plus	S=0
0101	MI	Minus	S=1
0100	OV	Overflow	V=1
1100	NOV	No overflow	V=0
0110	EQ	Equal	Z=1
1110	NE	Not equal	Z=0
1001	GE	Greater than or equal	(S XOR V)=0
0001	LT	Less than	(S XOR V)=1
1010	GT	Greater than	[Z OR (S XOR V)]=0
0010	LE	Less than or equal	[Z OR (S XOR V)]=1
1111	UGE	Unsigned greater than or equal	C=0
0111	ULT	Unsigned less than	C=1
1011	UGT	Unsigned greater than	(C = 0 AND Z=0)=1
0011	ULE	Unsigned less than or equal	(C OR Z)=1
0000	F	Never true (Always False)	—

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "←". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst(7)

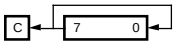
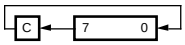
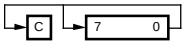
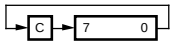
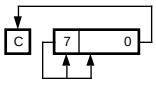
refers to bit 7 of the destination operand.

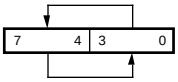
INSTRUCTION SUMMARY

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
ADC dst, src dst←dst+src+C	†	1[ ]	* * * * 0 *
ADD dst, src dst←dst+src	†	0[ ]	* * * * 0 *
AND dst, src dst←dstANDsrc	†	5[ ]	- * * 0 - -
CALL dst SP←SP–2 @SP←PC, PC←dst	DA IRR	D6 D4	- - - - - -
CCF C←NOTC		EF	* - - - - -
CLR dst dst←0	R IR	B0 B1	- - - - - -
COM dst dst←NOTdst	R IR	60 61	- * * 0 - -
CP dst, src dst–src	†	A[ ]	* * * * - -
DA dst dst←DAdst	R IR	40 41	* * * X - -
DEC dst dst←dst–1	R IR	00 01	- * * * - -
DECW dst dst←dst–1	RR IR	80 81	- * * * - -
DI IMR(7)←0		8F	- - - - - -
DJNZ r, dst r←r–1 if r≠0 PC←PC+dst Range: +127,–128	RA	rA r = 0 - F	- - - - - -
EI IMR(7)←1		9F	- - - - - -
HALT		7F	- - - - - -

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
INC dst dst←dst+1	r R IR	rE r = 0–F 20 21	- * * * - -
INCW dst dst←dst+1	RR IR	A0 A1	- * * * - -
IRET FLAGS←@SP; SP←SP+1 PC←@SP; SP←SP+2; IMR(7)←1		BF	* * * * * *
JP cc, dst if cc is true, PC←dst	DA IRR	cD c = 0–F 30	- - - - - -
JR cc, dst if cc is true, PC←PC+dst Range: +127,–128	RA	cB c = 0–F	- - - - - -
LD dst, src dst←src	r Im r R R r r X X r r Ir Ir r R R R IR R IM IR IM IR R	rC r8 r9 r = 0–F C7 D7 E3 F3 E4 E5 E6 E7 F5	- - - - - -
LDC dst, src dst←src	r Irr	C2	- - - - - -
LDCI dst, src dst←src r←r+1; rr←rr+1	Ir Irr	C3	- - - - - -

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
NOP		FF	- - - - - -
OR dst, src dst←dst OR src	†	4[ ]	- * * 0 - -
POP dst dst←@SP; SP←SP+1	R IR	50 51	- - - - - -
PUSH src SP←SP–1; @SP←src	R IR	70 71	- - - - - -
RCF C←0		CF	0 - - - - -
RET PC←@SP; SP←SP+2		AF	- - - - - -
RL dst 	R IR	90 91	* * * * - -
RLC dst 	R IR	10 11	* * * * - -
RR dst 	R IR	E0 E1	* * * * - -
RRC dst 	R IR	C0 C1	* * * * - -
SBC dst, src dst←dst–src–C	†	3[ ]	* * * * 1 *
SCF C←1		DF	1 - - - - -
SRA dst 	R IR	D0 D1	* * * 0 - -
SRP dst RP←src	Im	31	- - - - - -

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
STOP		6F	1 - - - - -
SUB dst, src dst←dst—src	†	2[ ]	* * * * 1 *
SWAP dst 	R IR	F0 F1	X * * X - -
TCM dst, src (NOT dst) AND src	†	6[ ]	- * * 0 - -
TM dst, src dst AND src	†	7[ ]	- * * 0 - -
WDH		4F	- - - - - -
WDT		5F	- X X X - -
XOR dst, src dst←dst XOR src	†	B[ ]	- * * 0 - -

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

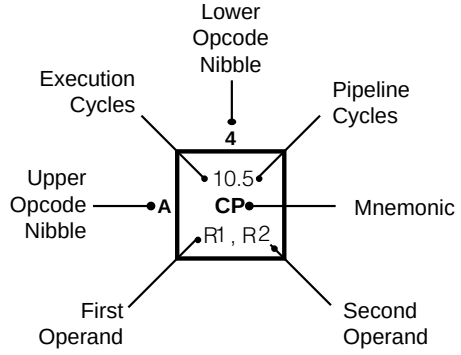
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								4.0 **WDH**
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1														6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1														6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1			20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2	3									2			3	1	



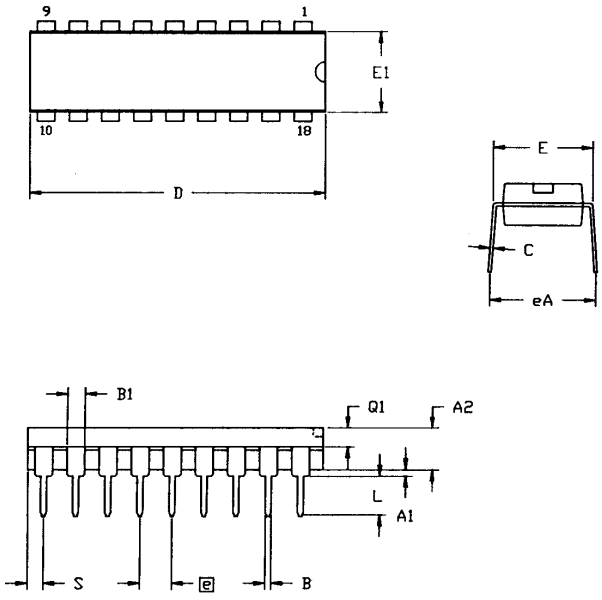
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: Blank areas are reserved.

*2-byte instruction appears as a 3-byte instruction

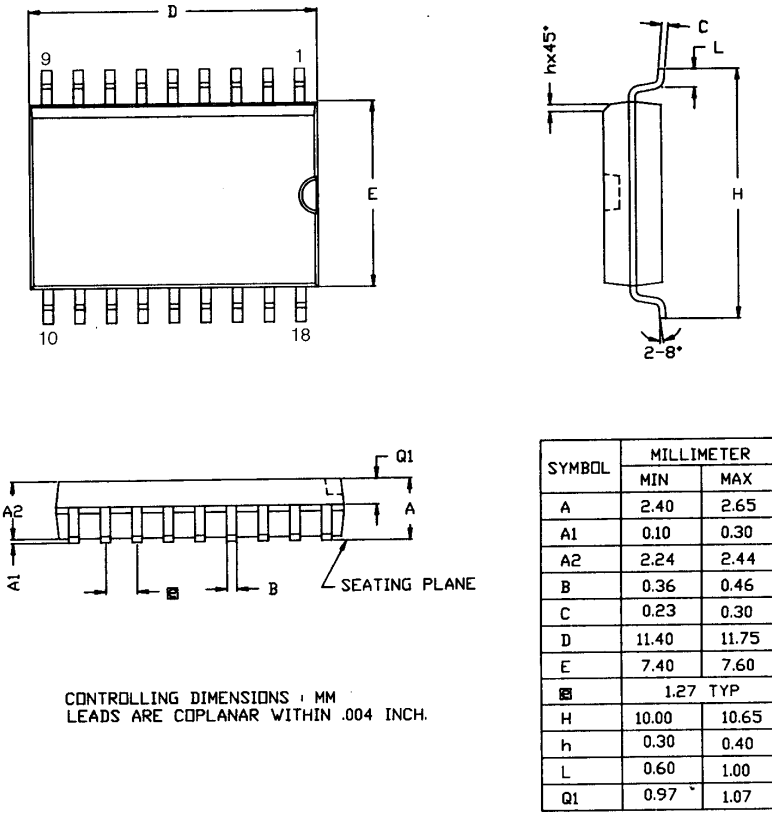
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram



CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

18-Pin SOIC Package Diagram

ORDERING INFORMATION

Standard Temperature

18-Pin DIP	18-Pin SOIC
Z86E0208PSC	Z86E0208SSC
Z86L0208PSC	Z86L0208SSC
Z86C0208PSC	Z86C0208SSC
Z86E0208PSC1903	Z86E0208SSC1903

Extended Temperature

18-Pin DIP	18-Pin SOIC
Z86E0208PEC	Z86E0208SEC
Z86L0208PEC	Z86L0208SEC
Z86C0208PEC	Z86C0208SEC
Z86E0208PEC1903	Z86E0208SEC1903

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

CODES

Preferred Package
P = Plastic DIP

Longer Lead Time
S = SOIC

Preferred Temperature
S = 0°C to +70°C
E = –40°C to +105°C

Speeds
08 = 8 MHz

Environmental
C = Plastic Standard

Example:

Z 86E02 08 P S C is a Z86E02, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow