PRELIMINARY
CUSTOMER PROCUREMENT SPECIFICATION

Z86C04/C08 & C05/C07

CMOS Z8® 8-BIT LOW-COST 1K/2K-ROM MICROCONTROLLERS

FEATURES

Part Number	ROM (Kbytes)	RAM* (Bytes)	Speed (MHz)	Auto Latch	Permanent WDT
Z86C04	1	125	8	Optional	Optional
Z86C08	2	125	12	Optional	Optional
Z86C05	1	125	8	None	Enabled
Z86C07	2	125	12	None	Enabled

* General-Purpose

- 18-Pin DIP and SOIC Packages
- 3.0V to 5.5V Operating Range
- 14 Input / Output Lines
- Six Vectored, Prioritized Interupts from Six Different Sources
- Two On-Board Comparators
- ROM Mask Options:
  - Low Noise
  - ROM Protect
  - Auto Latch
  - Permanent Watch-Dog Timer (WDT)
  - RC Oscillator
  - 32 KHz Operation
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- Power-On Reset (POR) Timer
- On-Chip Oscillator that Accepts RC, Crystal, Ceramic Resonance, LC, or External Clock Drive
- Clock-Free WDT Reset
- Low-Power Consumption (50mw)
- Fast Instruction Pointer (1.5µs @ 8 MHz, 1.0 µs @ 12 MHz)
- Fourteen Digital Inputs at CMOS Levels; Schmitt-Triggered
- Software Enabled Watch-Dog Timer
- Programmable Interrupt Polarity
- Two Standby Modes: STOP and HALT
- Low-Voltage Protection

GENERAL DESCRIPTION

Zilog's Z86C04/C08 and Z86C05/C07 Microcontrollers (MCU) are members of the Z8® single-chip microcontroller family which offer easy software/hardware system expansion.

For applications demanding powerful I/O capabilities, the Z86C04/C08 and Z86C05/C07's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of user selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications. Additionally, two on-board comparators process analog signals with a common reference voltage (Figure 1).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B/ /W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

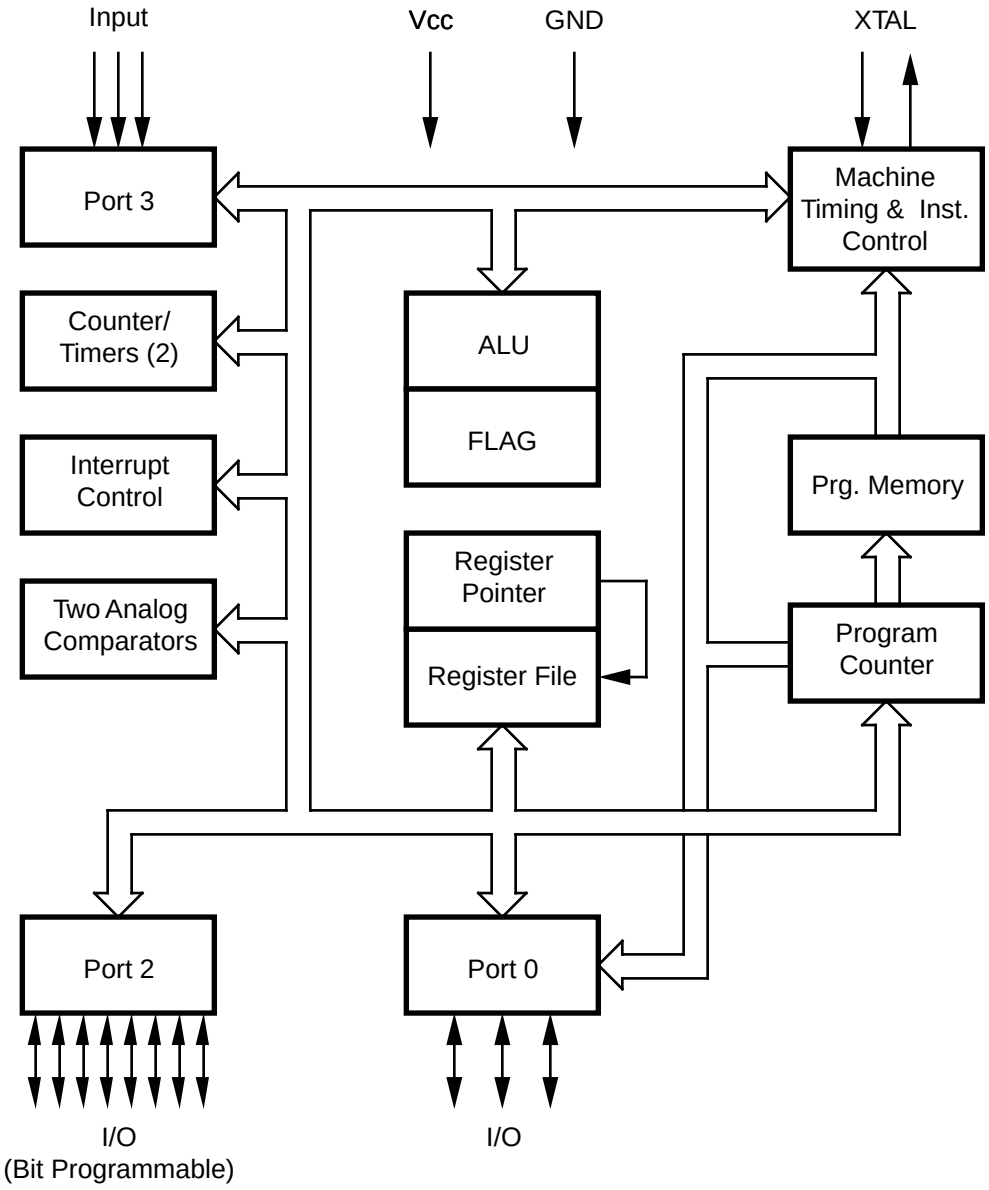

Figure 1. Z86C04/C08 and Z86C05/C07 Functional Block Diagram

PIN DESCRIPTIONS

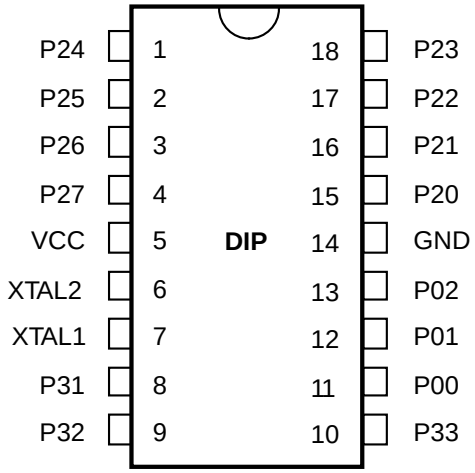

Figure 2. 18-Pin DIP Configuration

Table 1. 18-Pin DIP and SOIC Pin Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{cc}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0, 1, 2	In/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0, 1, 2, 3	In/Output

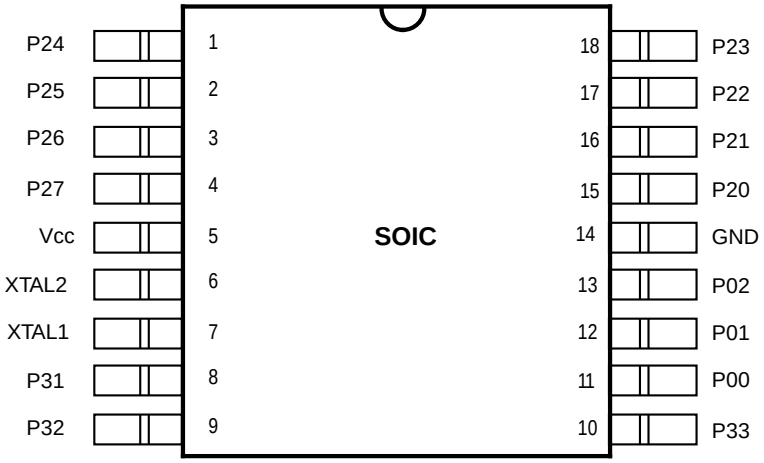

Figure 3. 18-Pin SOIC Pin Configuration

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	–40	+105	C
Storage Temperature	–65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	–0.6	+12	V
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V
Voltage on Pin 7 with Respect to V_{SS} [Note 2]	–0.6	V_{DD}+1	V
Total Power Dissipation		462	mW
Maximum Current out of V_{SS}		84	mA
Maximum Current into V_{DD}		84	mA
Maximum Current into an Input Pin [Note 3]	–600	+600	µA
Maximum Current into an Open-Drain Pin [Note 4]	–600	+600	µA
Maximum Output Current Sinked by Any I/O Pin		12	mA
Maximum Output Current Sourced by Any I/O Pin		12	mA
Total Maximum Output Current Sinked by Port 2		70	mA
Total Maximum Output Current Sourced by Port 2		70	mA

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

Notes:
[1] This applies to all pins except where otherwise noted. Maximum current into pin must be ±600µA.
[2] There is no input protection diode from pin to V_{DD}.
[3] This excludes Pin 6 and Pin 7.
[4] Device pin is not at an output Low state.

Total Power dissipation = V_{DD} x [I_{DD} – (sum of I_{OH})] + sum of [(V_{DD} – V_{OH}) x I_{OH}] + sum of (V_{0L} x I_{0L})

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 4).

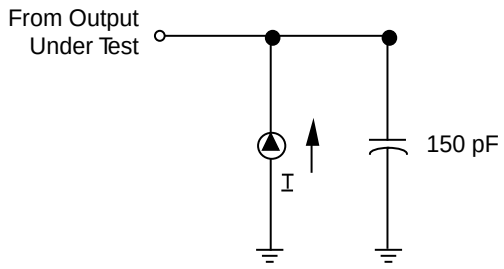

Figure 4. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	15 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC}[4]	T_A=0°C to +70°C Min	Max	T_A=–40°C to +105°C Min	Max	Typical @25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.8V_{CC}	V_{CC}+0.3	0.8V_{CC}	V_{CC}+0.3	1.7	V	Driven by External Clock Generator	
		5.5V	0.8V_{CC}	V_{CC}+0.3	0.8V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS}–0.3	0.2V_{CC}	V_{SS}–0.3	0.2V_{CC}	0.8	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2V_{CC}	V_{SS}–0.3	0.2V_{CC}	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7V_{CC}	V_{CC}+0.3	0.7V_{CC}	V_{CC}+0.3	1.8	V		[1]
		5.5V	0.7V_{CC}	V_{CC}+0.3	0.7V_{CC}	V_{CC}+0.3	2.8	V		[1]
V_{IL}	Input Low Voltage	3.0V	V_{SS}–0.3	0.2V_{CC}	V_{SS}–0.3	0.2V_{CC}	0.8	V		[1]
		5.5V	V_{SS}–0.3	0.2V_{CC}	V_{SS}–0.3	0.2V_{CC}	1.5	V		[1]
V_{OH}	Output High Voltage	3.0V	V_{CC}–0.4		V_{CC}–0.4		3.0	V	I_{OH}=–2.0mA	[5]
		5.5V	V_{CC}–0.4		V_{CC}–0.4		4.8	V	I_{OH}=–2.0mA	[5]
		3.0V	V_{CC}–0.4		V_{CC}–0.4		3.0	V	Low Noise@I_{OH}=–0.5mA	
		5.5V	V_{CC}–0.4		V_{CC}–0.4		4.8	V	Low Noise@I_{OH}=–0.5mA	
V_{OL1}	Output Low Voltage	3.0V		0.8		0.8	0.2	V	I_{OL}=+4.0mA	[5]
		5.5V		0.4		0.4	0.1	V	I_{OL}=+4.0mA	[5]
		3.0V		0.4		0.4	0.2	V	Low Noise@I_{OL}=1.0mA	
		5.5V		0.4		0.4	0.1	V	Low Noise@I_{OL}=1.0mA	
V_{OL2}	Output Low Voltage	3.0V		1.0		1.0	0.8	V	I_{OL}=+12mA	[5]
		5.5V		0.8		0.8	0.3	V	I_{OL}=+12mA	[5]
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		
		5.5V		25		25	10	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		2.2	2.8			2.6	V	Int. CLK Freq@6MHz Max.	
					2.0	3.0	2.6		Int. CLK Freq@4MHz Max.	
I_{IL}	Input Leakage (Input Bias Current of Comparator)	3.0V	–1.0	1.0	–1.0	1.0		µA	V_{IN}=0V,V_{CC}	
		5.5V	–1.0	1.0	–1.0	1.0		µA	V_{IN}=0V,V_{CC}	
I_{OL}	Output Leakage	3.0V	–1.0	1.0	–1.0	1.0		µA	V_{IN}=0V,V_{CC}	
		5.5V	–1.0	1.0	–1.0	1.0		µA	V_{IN}=0V,V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range		0	V_{CC}–1.0	0	V_{CC}–1.5		V		

Sym	Parameter	V_{CC}[4]	T_A=0°C to +70°C Min	Max	T_A=–40°C to +105°C Min	Max	Typical @25°C	Units	Conditions	Notes
I_{CC}	Supply Current	3.2V					8.0	µA	All output and I/O Pins Floating @32kHz	[7]
		3.0V		3.5		3.5	1.5	mA	All Output and I/O Pins Floating @2MHz	[5]
		5.5V		7.0		7.0	3.8	mA	All Output and I/O Pins Floating @2MHz	[5]
		3.0V		8.0		8.0	3.0	mA	All Output and I/O Pins Floating @8MHz	[5]
		5.5V		11.0		11.0	4.4	mA	All Output and I/O Pins Floating @8MHz	[5]
		3.0V		10		10	3.6	mA	All Output and I/O Pins Floating @12MHz	[5,6]
		5.5V		15		15	9.0	mA	All Output and I/O Pins Floating @12MHz	[5,6]
I_{CC1}	Standby Current	3.0V		2.5		2.5	0.7	mA	HALT mode V_{IN}=0V, V_{CC} @2MHz	[5]
		5.5V		4.0		4.0	2.5	mA	HALT mode V_{IN}=0V, V_{CC} @2MHz	[5]
		3.0V		4.0		4.0	1.0	mA	HALT mode V_{IN}=OV, V_{CC} @8MHz	[5]
		5.5V		5.0		5.0	3.0	mA	HALT mode V_{IN}=OV, V_{CC} @8MHz	[5]
		3.0V		4.5		4.5	1.5	mA	HALT mode V_{IN}=OV, V_{CC} @12MHz	[5,6]
		5.5V		7.0		7.0	4.0	mA	HALT mode V_{IN}=OV, V_{CC} @12MHz	[5,6]
I_{CC}	Supply Current (Low Noise Mode)	3.0V		3.5		3.5	1.5	mA	All Output and I/O Pins Floating @1MHz	
		5.5V		7.0		7.0	3.8	mA	All Output and I/O Pins Floating @1MHz	
		3.0V		5.8		5.8	2.5	mA	All Output and I/O Pins Floating @2MHz	
		5.5V		9.0		9.0	4.0	mA	All Output and I/O Pins Floating @2MHz	
		3.0V		8.0		8.0	3.0	mA	All Output and I/O Pins Floating @4MHz	
		5.5V		11.0		11.0	4.4	mA	All Output and I/O Pins Floating @4MHz	

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical @25°C	Units	Conditions
I_{CC1}	Standby Current (Low Noise Mode)	3.0V		2.5		2.5	0.7	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz
		5.5V		4.0		4.0	2.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz
		3.0V		3.0		3.0	0.9	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz
		5.5V		4.5		4.5	2.8	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz
		3.0V		4.0		4.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 4 MHz
		5.5V		5.0		5.0	3.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 4 MHz
I_{CC2}	Standby Current	3.0V		10		20	1.0	µA	STOP mode V_{IN} = 0V, V_{CC} WDT is not Running
		5.5V		10		20	1.0	µA	STOP mode V_{IN} = 0V, V_{CC} WDT is not Running
I_{ALL}	Auto Latch Low Current	3.0V		12		8.0	3.0	µA	0V < V_{IN} < V_{CC}
		5.5V		32		30	16	µA	0V < V_{IN} < V_{CC}
I_{ALH}	Auto Latch High Current	3.0V	–8		-5.0		-1.5	µA	0V < V_{IN} < V_{CC}
		5.5V	–16		-20		-8.0	µA	0V < V_{IN} < V_{CC}

Notes:

[1] Port 0, 2, and 3 only.

[2] V_{SS} = 0V = GND.

[3] The device operates down to V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient tempera ture. The V_{LV} increases as the temperature decreases.

[4] V_{CC} = 3.0V to 5.5V, typical values measured at V_{CC} = 3.3V and V_{CC} = 5.0V.

[5] Standard Mode (not Low EMI mode).

[6] Z86C07/C08 only.

[7] CL1 = 100 pF, CL2 = 220 pF, RF = 30 kOhm

AC ELECTRICAL CHARACTERISTICS

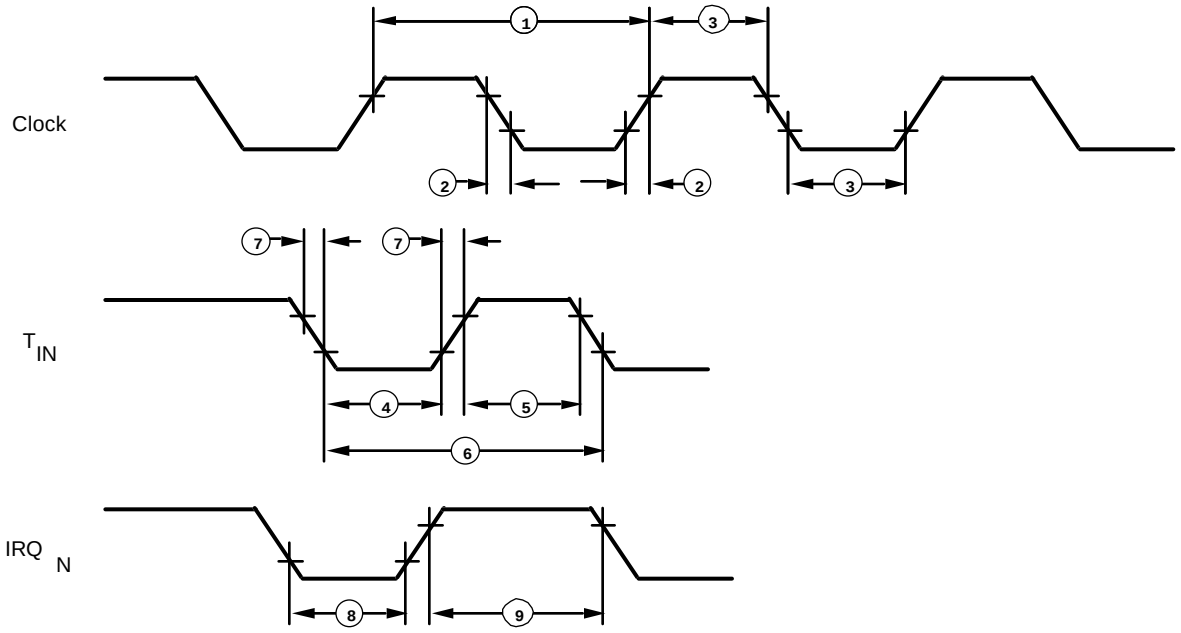

Figure 5. AC Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

				T_A=0°C to +70°C				T_A=–40°C to +105°C					
				8 MHz (C04/05)		12 MHz (C07/08)		8 MHz (C04/05)		12 MHz (C07/08)			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	125	DC	83	DC	125	DC	83	DC	ns	[1]
			5.5V	125	DC	83	DC	125	DC	83	DC	ns	[1]
2	TrC,TfC	Clock Input Rise	3.0V		25		15		25		15	ns	[1]
		and Fall Times	5.5V		25		15		25		15	ns	
3	TwC	Input Clock Width	3.0V	62		41			62		41		[1]
			5.5V	62		41			62		41	ns	[1]
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	[1]
			5.5V	70		70		70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			[1]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1]
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			[1]
			5.5V	8TpC		8TpC		8TpC		8TpC			[1]
7	TrTin,	Timer Input Rise	3.0V		100		100		100		100	ns	[1]
	TtTin	and Fall Timer	5.5V		100		100		100		100	ns	[1]
8	TwIL	Int. Request Input	3.0V	100		100		100		100		ns	[1,2]
		Low Time	5.5V	70		70		70		70		ns	[1,2]
9	TwIH	Int. Request Input	3.0V	5TpC		5TpC		5TpC		5TpC			[1]
		High Time	5.5V	5TpC		5TpC		5TpC		5TpC			[1,2]
10	Twdt	Watch-Dog Timer	3.0V		25		25		25		25	ms	[1]
		Delay Time	5.5V		12		12		10		10	ms	[1]
11	Tpor		3.0V	24		24		24		24		ms	[1]
			5.5V	12		12		12		12		ms	[1]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

[2] Interrupt request through Port 3 (P33-P31).

AC ELECTRICAL CHARACTERISTICS

Low Noise Mode

				T_A=0°C to +70°C				T_A=–40°C to +105°C					
				1MHz		4MHz		1MHz		4MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TPC	Input Clock Period	3.0V	1000	DC	250	DC	1000	DC	250	DC	ns	[1]
			5.5V	1000	DC	250	DC	1000	DC	250	DC	ns	[1]
2	TrC	Clock Input Rise	3.0V		25		25		25		25	ns	[1]
	TfC	and Fall Times	5.5V		25		25		25		25	ns	[1]
3	TwC	Input Clock Width	3.0V	500		125		500		125		ns	[1]
			5.5V	500		125		500		125		ns	[1]
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	[1]
			5.5V	70		70		70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC		4TpC		4TpC			[1]
			5.5V	4TpC		4TpC		4TpC		4TpC			[1]
7	TrTin,	Timer Input Rise	3.0V		100		100		100		100	ns	[1]
	TtTin	and Fall Timer	5.5V		100		100		100		100	ns	[1]
8	TwIL	Int. Request Input	3.0V	100		100		100		100		ns	[1,2]
		Low Time	5.5V	70		70		70		70		ns	[1,2]
9	TwIH	Int. Request Input	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
		High Time	5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1,2]
10	Twdt	Watch-Dog Timer	3.0V		25		25		25		25	ms	[1]
		Delay Time	5.5V		12		12		10		10	ms	[1]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

[2] Interrupt request through Port 3 (P33-P31).

LOW NOISE VERSION

Low EMI Emission

The Z8® can be programmed to operate in a Low EMI emission mode by means of a mask ROM bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

EMI Characteristics

The Z8 operating in the Low EMI mode generates EMI as measured in the following chart:

The measurements, shown in Figure 6, were made while operating the Z8 in three states: (1) idle condition; (2) static output; (3) switched output.

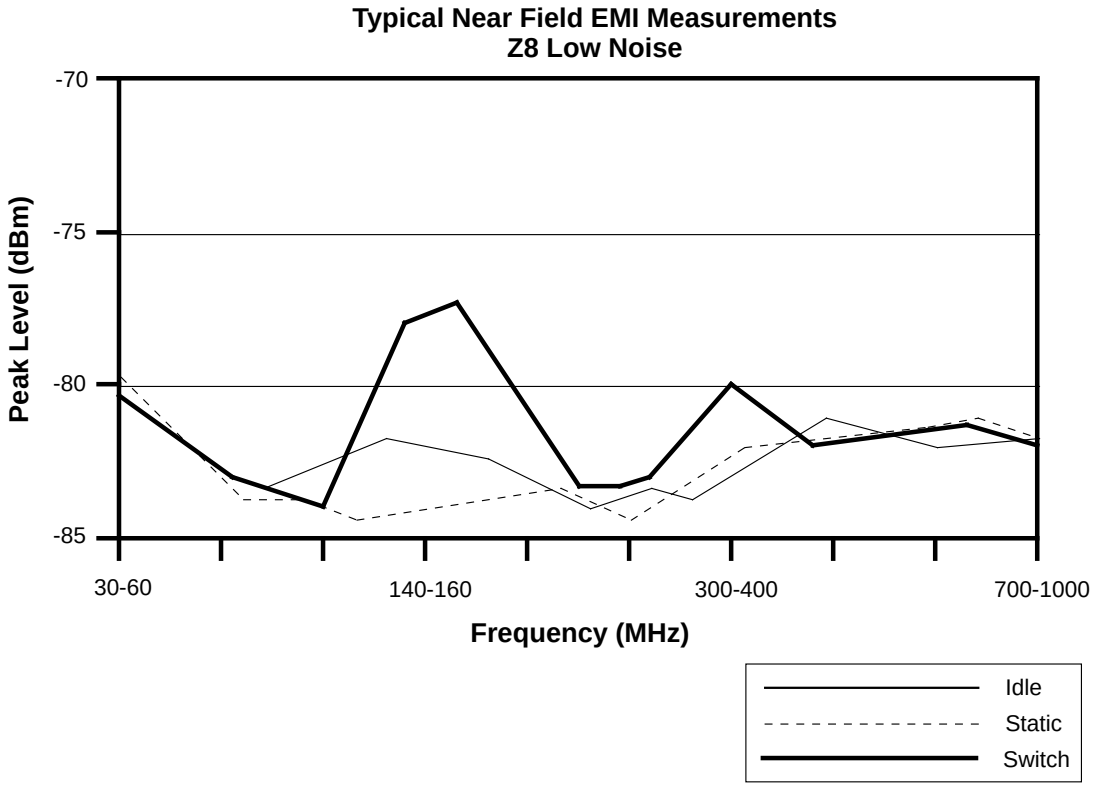

Figure 6. Typical Low Noise Measurements

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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