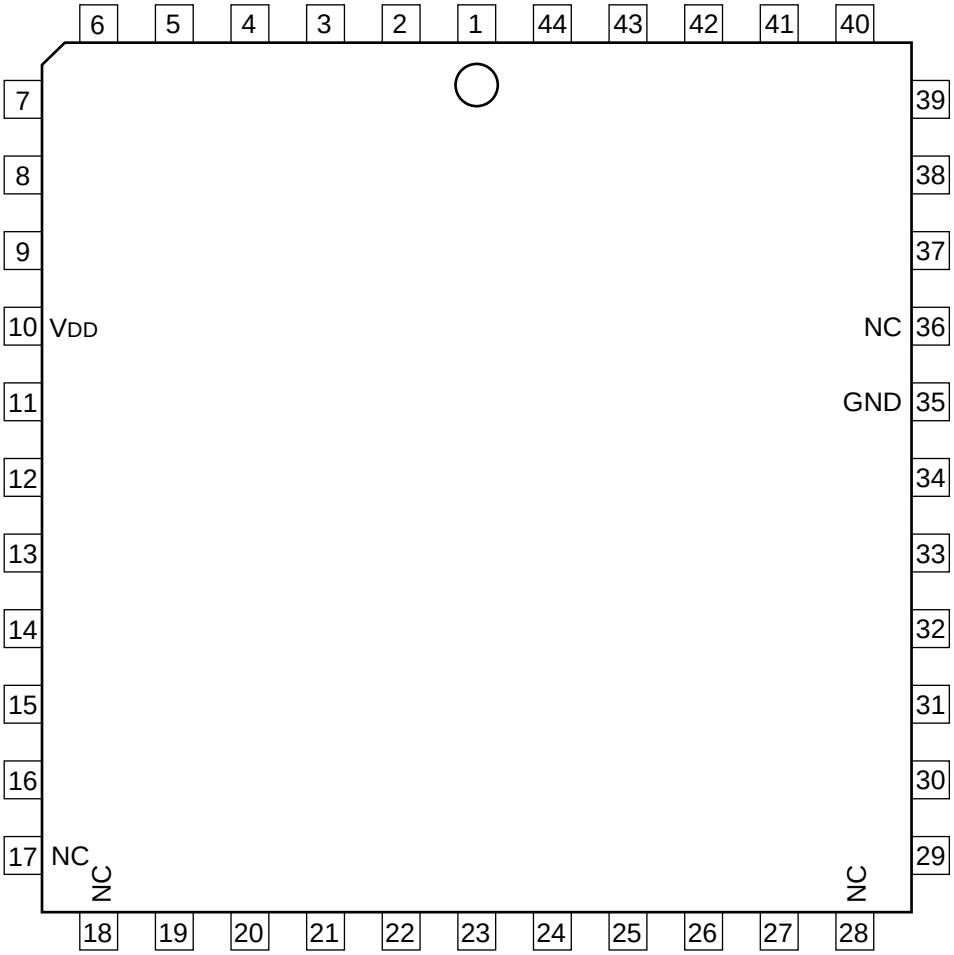
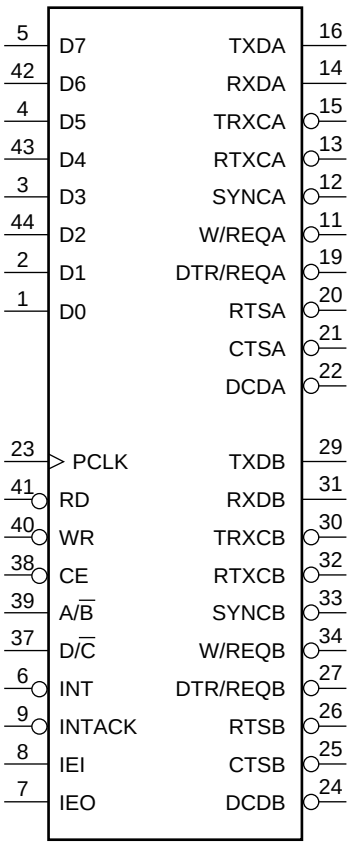
C-MOS SERIAL COMMUNICATION CONTROLLER

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I/O	D0	12	I/O	$\overline{\text{SYNCA}}$	23	I	PCLK	34	O	$\overline{\text{W}}/\overline{\text{REQB}}$
2	I/O	D1	13	I	$\overline{\text{RTXCA}}$	24	I	$\overline{\text{DCDB}}$	35	—	GND
3	I/O	D3	14	I	RXDA	25	I	$\overline{\text{CTSB}}$	36	—	NC
4	I/O	D5	15	I/O	$\overline{\text{TRXCA}}$	26	O	$\overline{\text{RTSB}}$	37	I	D/$\overline{\text{C}}$
5	I/O	D7	16	O	TXDA	27	O	$\overline{\text{DTR}}/\overline{\text{REQB}}$	38	I	$\overline{\text{CE}}$
6	O	$\overline{\text{INT}}$	17	—	NC	28	—	NC	39	I	A/$\overline{\text{B}}$
7	O	IEO	18	—	NC	29	O	TXDB	40	I	$\overline{\text{WR}}$
8	I	IEI	19	O	$\overline{\text{DTR}}/\overline{\text{REQA}}$	30	I/O	$\overline{\text{TRXCB}}$	41	I	$\overline{\text{RD}}$
9	I	$\overline{\text{INTACK}}$	20	O	$\overline{\text{RTSA}}$	31	I	RXDB	42	I/O	D6
10	—	VDD	21	I	$\overline{\text{CTSA}}$	32	I	$\overline{\text{RTXCB}}$	43	I/O	D4
11	O	$\overline{\text{W}}/\overline{\text{REQA}}$	22	I	$\overline{\text{DCDA}}$	33	I/O	$\overline{\text{SYNCB}}$	44	I/O	D2



INPUT

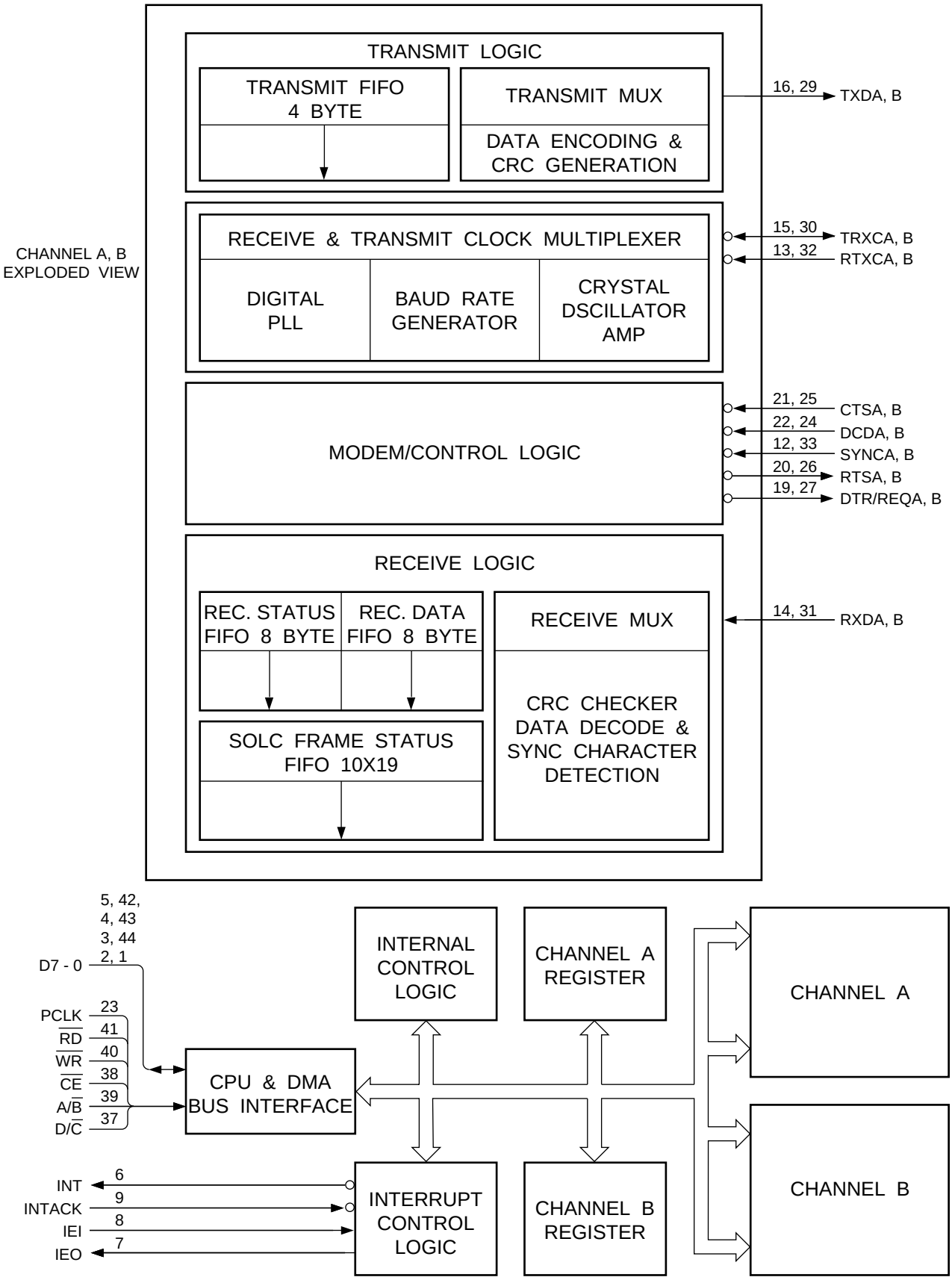
A/$\overline{B}$	;	CHANNEL A/CHANNEL B
$\overline{CE}$	;	CHIP ENABLE
$\overline{CTSA}$, $\overline{B}$	;	CLEAR TO SEND
D/$\overline{C}$	;	DATA/CONTROL SELECT
$\overline{DCDA}$, $\overline{B}$	;	DATA CARRIER DETECT
IEI	;	INTERRUPT ENABLE
$\overline{INTACK}$	;	INTERRUPT ACKNOWLEDGE
PCLK	;	CLOCK
$\overline{RD}$	;	READ
$\overline{RTXCA}$, $\overline{B}$	;	RECEIVE/TRANSMIT CLOCKS
RXDA, B	;	RECEIVE DATA
$\overline{WR}$	;	WRITE

OUTPUT

$\overline{DTR/REQA}$, $\overline{B}$	;	DATA TERMINAL READY/REQUEST
IEO	;	INTERRUPT ENABLE
$\overline{INT}$	;	INTERRUPT
$\overline{RTSA}$, $\overline{B}$	;	REQUEST TO SEND
TXDA, B	;	TRANSMIT DATA
$\overline{W/REQA}$, $\overline{B}$	;	WAIT/REQUEST

INPUT/OUTPUT

D7 - 0	;	DATA BUS
$\overline{SYNCA}$, $\overline{B}$	;	SYNCHRONIZATION
$\overline{TRXCA}$, $\overline{B}$	;	TRANSMIT/RECEIVE CLOCKS


CHANNEL A, B
EXPLODED VIEW
TRANSMIT LOGIC
TRANSMIT FIFO
4 BYTE
TRANSMIT MUX
DATA ENCODING &
CRC GENERATION
16, 29
TXDA, B
RECEIVE & TRANSMIT CLOCK MULTIPLEXER
DIGITAL
PLL
BAUD RATE
GENERATOR
CRYSTAL
DSCILLATOR
AMP
15, 30
TRXCA, B
13, 32
RTXCA, B
MODEM/CONTROL LOGIC
21, 25
CTSA, B
22, 24
DCDA, B
12, 33
SYNCA, B
20, 26
RTSA, B
19, 27
DTR/REQA, B
RECEIVE LOGIC
REC. STATUS
FIFO 8 BYTE
REC. DATA
FIFO 8 BYTE
RECEIVE MUX
14, 31
RXDA, B
SOLC FRAME STATUS
FIFO 10X19
CRC CHECKER
DATA DECODE &
SYNC CHARACTER
DETECTION
5, 42,
4, 43
3, 44
2, 1
D7 - 0
PCLK
23
RD
41
WR
40
CE
38
A/B
39
D/C
37
CPU & DMA
BUS INTERFACE
INTERNAL
CONTROL
LOGIC
CHANNEL A
REGISTER
CHANNEL A
CHANNEL B
CHANNEL B
REGISTER
INTERRUPT
CONTROL
LOGIC
INT
6
INTACK
9
IEI
8
IEO
7