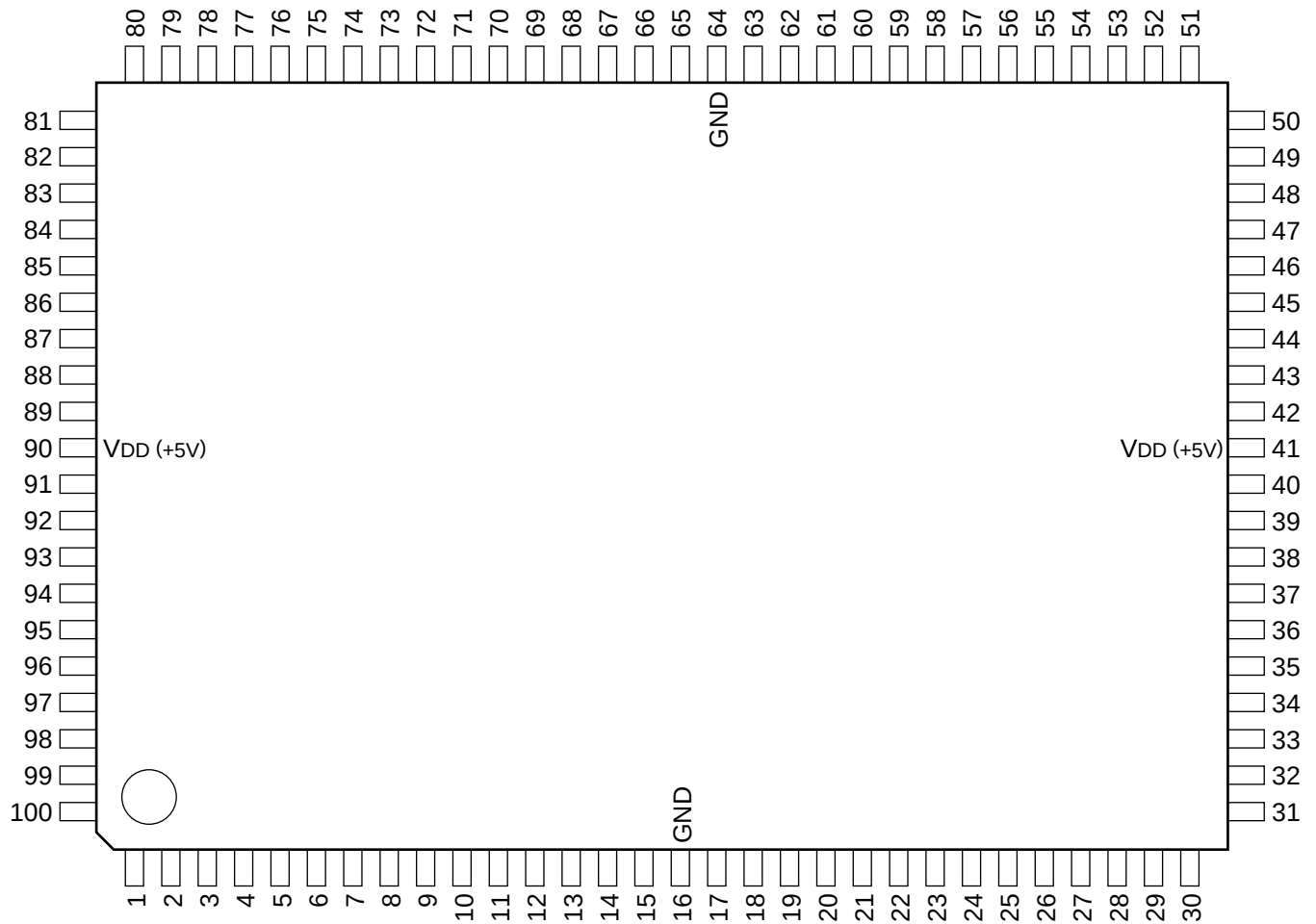

C-MOS INTELLIGENT PERIPHERAL CONTROLLER

-TOP VIEW-



(V_{DD} = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I/O	A5	26	I/O	PA3	51	I/O	$\overline{\text{SYNCB}}$	76	O	ZC/TO2
2	I/O	A4	27	I/O	PA2	52	O	$\overline{\text{W/RDYB}}$	77	O	ZC/TO3
3	I/O	A3	28	I/O	PA1	53	I/O	PB0	78	I	CLK/TG3
4	I/O	A2	29	I/O	PA0	54	I/O	PB1	79	I	CLK/TG2
5	I/O	A1	30	O	$\overline{\text{W/RDYA}}$	55	I/O	PB2	80	I	CLK/TG1
6	I/O	A0	31	I/O	$\overline{\text{SYNCA}}$	56	I/O	PB3	81	I	CLK/TG0
7	O	$\overline{\text{RFSH}}$	32	I	RXDA	57	I/O	PB4	82	I/O	D7
8	I/O	M1	33	I	$\overline{\text{RXCA}}$	58	I/O	PB5	83	I/O	D6
9	I	$\overline{\text{RESET}}$	34	I	$\overline{\text{TXCA}}$	59	I/O	PB6	84	I/O	D5
10	I	$\overline{\text{BUSREQ}}$	35	O	TXDA	60	I/O	PB7	85	I/O	D4
11	I	$\overline{\text{WAIT}}$	36	O	$\overline{\text{DTRA}}$	61	I	$\overline{\text{BSTB}}$	86	I/O	D3
12	O	$\overline{\text{BUSACK}}$	37	O	$\overline{\text{RTSA}}$	62	O	BRDY	87	I/O	D2
13	I/O	$\overline{\text{WR}}$	38	I	$\overline{\text{CTSA}}$	63	I	$\overline{\text{NMI}}$	88	I/O	D1
14	I/O	$\overline{\text{RD}}$	39	I	$\overline{\text{DCDA}}$	64	—	GND	89	I/O	D0
15	I/O	$\overline{\text{IORQ}}$	40	O	ICT	65	I	XTAL1	90	—	V _{DD}
16	—	GND	41	—	V _{DD}	66	O	XTAL2	91	I/O	A15
17	I/O	$\overline{\text{MREQ}}$	42	O	ICT	67	I	EV	92	I/O	A14
18	O	$\overline{\text{HALT}}$	43	I	$\overline{\text{DCDB}}$	68	O	CLKOUT	93	I/O	A13
19	I	$\overline{\text{INT}}$	44	I	$\overline{\text{CTSB}}$	69	I	CLKIN	94	I/O	A12
20	O	ARDY	45	O	$\overline{\text{RTSB}}$	70	O	A7RF	95	I/O	A11
21	I	$\overline{\text{ASTB}}$	46	O	$\overline{\text{DTRB}}$	71	O	IEO	96	I/O	A10
22	I/O	PA7	47	O	TXDB	72	I	IEI	97	I/O	A9
23	I/O	PA6	48	I	$\overline{\text{TXCB}}$	73	O	$\overline{\text{WDTOUT}}$	98	I/O	A8
24	I/O	PA5	49	I	$\overline{\text{RXC B}}$	74	O	ZC/TO0	99	I/O	A7
25	I/O	PA4	50	I	RXDB	75	O	ZC/TO1	100	I/O	A6

6	A0	D0	89
5	A1	D1	88
4	A2	D2	87
3	A3	D3	86
2	A4	D4	85
1	A5	D5	84
100	A6	D6	83
99	A7	D7	82
98	A8	RFSH	7
97	A9	WR	13
96	A10	RD	14
95	A11	IORQ	15
94	A12	MREQ	17
93	A13	BUSACK	12
92	A14	M1	8
91	A15	HALT	18
63	NMI	WAIT	11
65	XTAL1	BUSREQ	10
66	XTAL2	EV	67
69	CLKIN	RESET	9
68	CLKOUT	INT	19
81	CLK/TRG0	ZC/TO0	74
80	CLK/TRG1	ZC/TO1	75
79	CLK/TRG2	ZC/TO2	76
78	CLK/TRG3	ZC/TO3	77
38	CTSA	RTSA	37
39	DCDA	DTRA	36
32	RXDA	TXDA	35
33	RXCA	TXCA	34
31	SYNCA	W/RDYA	30
44	CTSB	RTSB	45
43	DCDB	DTRB	46
50	RXDB	TXDB	47
49	RXCB	TXCB	48
51	SYNCB	W/RDYB	52
29	PA0	PB0	53
28	PA1	PB1	54
27	PA2	PB2	55
26	PA3	PB3	56
25	PA4	PB4	57
24	PA5	PB5	58
23	PA6	PA6	59
22	PA7	PA7	60
21	ASTB	BSTB	61
20	ARDY	BRDY	62
72	IEI	IEO	71
40	ICT	WDTOUT	73
42	ICT	A7RF	70

INPUT

ASTB, BSTB	; PORT A, B STROBE
BUSACK	; BUS ACKNOWLEDGE
BUSREQ	; BUS REQUEST
CLK/TRG0 - CLK/TRG3	; EXTERNAL CLOCK/TRIGGER
CLKIN	; SYSTEM CLOCK
CTSA, CTSB	; CLEAR TO SEND
DCDA, DCDB	; DATA CARRIER DETECT
EV	; EVALUATOR
IEI	; INTERRUPT ENABLE
INT	; MASKABLE INTERRUPT REQUEST
NMI	; NON-MASKABLE INTERRUPT REQUEST
RESET	; RESET
RXCA, RXCB	; RECEIVE CLOCK A, B
RXDA, RXDB	; SERIAL RECEIVE DATA A, B
TXCA, TXCB	; TRANSMIT CLOCK A, B
WAIT	; WAIT
XTAL1	; CRYSTAL OSCILLATOR

OUTPUT

A7RF	; 1-BIT AUXILIARY ADDRESS BUS
ARDY, BRDY	; REGISTER A, B READY
CLKOUT	; SYSTEM CLOCK
DTRA, DTRB	; DATA TERMINAL READY
HALT	; HALT
ICT	; TEST
IEO	; INTERRUPT ENABLE
RFSH	; REFRESH
RTSA, RTSB	; REQUEST TO SEND
SYNCA, SYNCB	; SYNCHRONOUS A, B
TXDA, TXDB	; SERIAL TRANSMIT DATA A, B
W/RDYA, W/RDYB	; WAIT/READY A, B
WDTOUT	; WATCH DOG TIMER
XTAL2	; CRYSTAL OSCILLATOR
ZC/TO0 - ZC/TO3	; ZERO COUNT/TIMER

INPUT/OUTPUT

A0 - A15	; 16-BIT ADDRESS BUS
D0 - D7	; 8-BIT BIDIRECTIONAL DATA BUS
M1	; MACHINE SYCLE "1"
MREQ	; I/O REQUEST
PA0 - PA7, PB0 - PB7	; PORT A, B DATA
RD	; READ
WR	; WRITE

