CHAPTER 8
POWER-DOWN MODES

8.1 INTRODUCTION

In addition to the standard RUN mode, the Z8® MCU supports two Power-Down modes to minimize device current consumption. The two modes supported are HALT and STOP.

8.2 HALT MODE OPERATION

The HALT mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active so the internal clock continues to run and is applied to the Counter/Timer(s) and interrupt logic.

To enter the HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the application program must execute a NOP instruction (opcode = FFH) immediately before the HALT instruction (opcode 7FH), that is,

```
FF    NOP     ;clear the instruction pipeline
7F    HALT    ;enter HALT mode
```

The HALT mode is exited by interrupts, either externally or internally generated. Upon completion of the interrupt service routine, the user program continues from the instruction after HALT.

The HALT mode may also be exited via a POR/RESET activation or a Watch-Dog Timer (WDT) timeout. (See the product data sheet for WDT availability). In this case, program execution will restart at the reset restart address 000CH.

To further reduce power consumption in the HALT mode, some Z8 family devices allow dynamic internal clock scaling. Clock scaling may be accomplished on the fly by reprogramming bit 0 and/or bit1 of the STOP-Mode Recovery register (SMR). See Figure 8-1.

Note: Internal clock scaling directly effects Counter/Timer operation — adjustment of the prescaler and downcounter values may be required. To determine the actual HALT mode current (I_{CC1}) value for the various optional modes available, see the related Z8 device's product specification.

8.3 STOP MODE OPERATION

The STOP mode provides the lowest possible device standby current. This instruction turns off the on-chip oscillator and internal system clock.

To enter the STOP mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the application program must execute a NOP instruction (opcode=FFH) immediately before the STOP instruction (opcode=6FH), that is,

```
FF    NOP    ;clear the instruction pipeline
6F    STOP   ;enter STOP mode
```

The STOP mode is exited by any one of the following resets: Power-On Reset activation, WDT time out (if available), or a STOP-Mode Recovery source. Upon reset generation, the processor will always restart the application program at address 000CH.

POR/RESET activation is present on all Z8 devices and is implemented as a reset pin and/or an on-chip power on reset circuit.

Some Z8 devices allow for the on-chip WDT to run in the STOP mode. If so activated, the WDT timeout will generate a reset some fixed time period after entering the STOP mode.

Note: STOP-Mode Recovery by the WDT will increase the STOP mode standby current (I_{CC2}). This is due to the WDT clock and divider circuitry that is now enabled and running to support this recovery mode. See the product data sheet for actual I_{CC2} values.

All Z8 devices provide some form of dedicated STOP-Mode Recovery (SMR) circuitry. Two SMR methods are implemented — a single fixed input pin or a flexible, programmable set of inputs. The selected Z8 device product specification should be reviewed to determine the SMR options available for use.

Note: For devices that support SPI, the slave mode compare feature also serves as a SMR source.

In the simple case, a low level applied to input pin P27 will trigger a SMR. To use this mode, pin P27 (I/O Port 2, bit 7) must be configured as an input before the STOP mode is entered. The low level on P27 must meet a minimum pulse width T_{WSM}. (See the product data sheet) to trigger the device reset mode). Some Z8 devices provide multiple SMR input sources. The desired SMR source is selected via the SMR Register.

Note: Use of specialized SMR modes (P2.7 input or SMR register based) or the WDT timeout (only when in the STOP mode) provide a unique reset operation. Some control registers are initialized differently for a SMR/WDT triggered POR than a standard reset operation. See the product specification (register file map) for exact details.

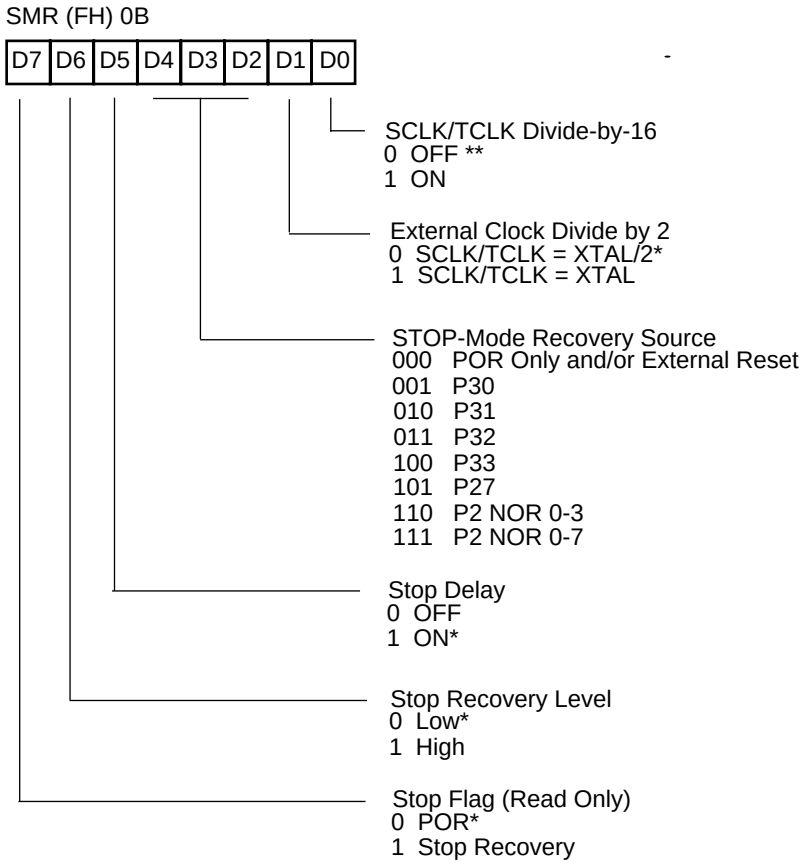
To determine the actual STOP mode current (I_{CC2}) value for the optional SMR modes available, see the selected Z8 device's product data sheet.

Note: The STOP mode current (I_{CC2}) will be minimized when:

- V_{CC} is at the low end of the devices operating range.
- WDT is off in the STOP mode.
- Output current sourcing is minimized.
- All inputs (digital and analog) are at the low or high rail voltages.

8.4 STOP-MODE RECOVERY REGISTER (SMR)

This register selects the clock divide value and determines the mode of STOP-Mode Recovery (Figure 8-1). All bits are Write-Only, except bit 7, that is Read-Only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, of the SMR register, specify the source of the STOP-Mode Recovery signal. Bits 0 and 1 control internal clock divider circuitry. The SMR is located in Bank F of the Expanded Register File at address 0BH.



* Default setting after RESET.

** Default setting after RESET and STOP-Mode Recovery.

Figure 8-1. STOP-Mode Recovery Register (Write-Only Except Bit D7, Which Is Read-Only)

Note: The SMR register is available in select Z8 MCU products. Refer to the device product specification to determine SMR options available.

SCLK/TCLK Divide-by-16 Select (DO). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON helps further lower EMI (D7 (PCON) =0, D1 (SMR) =1). The default setting is zero.

8.4 STOP-MODE RECOVERY REGISTER (SMR) (Continued)

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake-up source of the STPO recovery and (Table 8-1 and Figures 8-2).

Table 8-1. STOP-Mode Recovery Source

SMR: 432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	P30 transition
0	1	0	P31 transition (not in Analog Mode)
0	1	1	P32 transition (not in Analog Mode)
1	0	0	P33 transition (not in Analog Mode)
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

STOP-Mode Recovery Delay Select (D5). This bit, if High, enables the T_{POR} /RESET delay after Stop-Mode Recovery. The default configuration of this bit is 1. If the "fast" wake up is selected, the Stop-Mode Recovery source is kept active for at least 5 TpC.

STOP-Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the Z8® from STOP mode. A 0 indicates low-level recovery. The default is 0 on POR (Figure 8-2).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. A 0 in this bit (cold) indicates that the device reset by POR/WDT RESET. A 1 in this bit (warm) indicates that the device awakens by a SMR source.

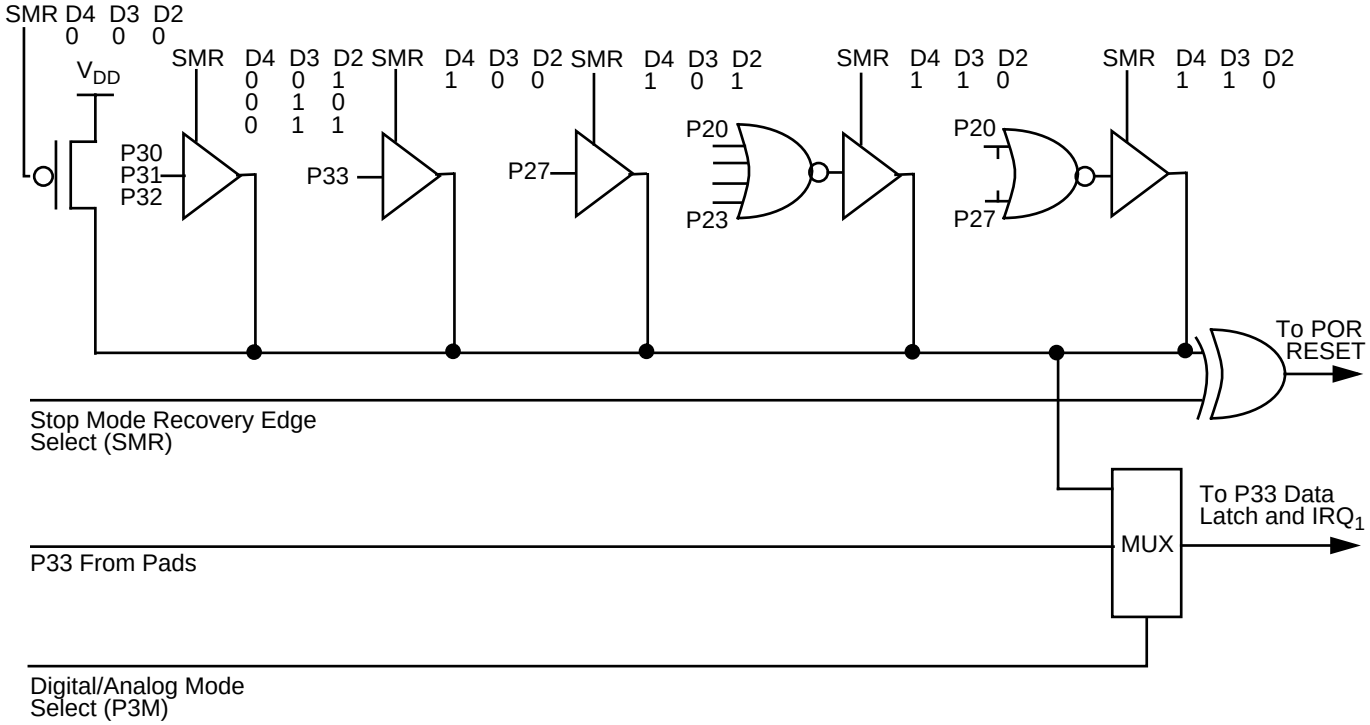


Figure 8-2. STOP-Mode Recovery Source

Note: If P31, P32, or P33 are to be used for a SMR source, the digital mode of operation must be selected prior to entering the STOP Mode.