CHAPTER 6
COUNTER/TIMERS

6.1 INTRODUCTION

The Z8® MCU provides up to two 8-bit counter/timers, T0 and T1, each driven by its own 6-bit prescaler, PRE0 and PRE1 (Figure 6-1). Both counter/timers are independent of the processor instruction sequence, that relieves software from time-critical operations such as interval timing or event counting. Some MCUs offer clock scaling using the SMR register. See the device product specification for clock available options. The following description is typical.

Each counter/timer operates in either Single-Pass or Continuous mode. At the end-of-count, counting either stops or the initial value is reloaded and counting continues. Under software control, new values are loaded immediately or when the end-of-count is reached. Software also controls the counting mode, how a counter/timer is started or stopped, and its use of I/0 lines. Both the counter and prescaler registers can be altered while the counter/timer is running.

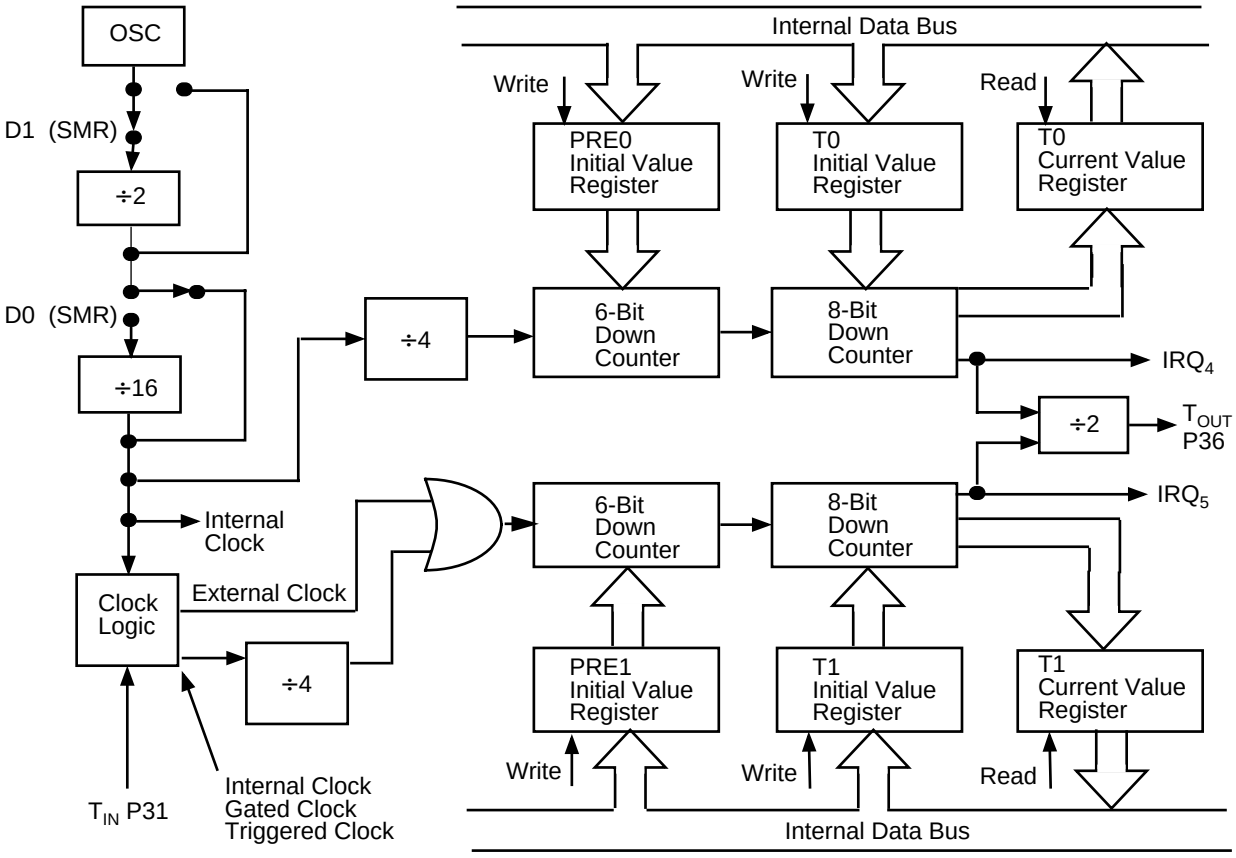

Figure 6-1. Counter/Timer Block Diagram

Counter/timers 0 and 1 are driven by a timer clock generated by dividing the internal clock by four. The divide-by-four stage, the 6-bit prescaler, and the 8-bit counter/timer form a synchronous 16-bit divide chain. Counter/timer 1 can also be driven by a external input (T_{IN}) using P31. Port 3 line P36 can serve as a timer output (T_{OUT}) through which T0, T1, or the internal clock can be output. The timer output will toggle at the end-of-count.

The counter/timer, prescaler, and associated mode registers are mapped into the register file as shown in Figure 6-2. This allows the software to treat the counter/timers as general-purpose registers, and eliminates the need for special instructions.

6.2 PRESCALERS AND COUNTER/TIMERS

The prescalers, PRE0 (F5H) and PRE1 (F3H), each consist of an 8-bit register and a 6-bit down-counter as shown in Figure 6-1. The prescaler registers are write-only registers. Reading the prescalers returns the value FFH. Figures 6-3 and 6-4 show the prescaler registers.

The six most significant bits (D2-D7) of PRE0 or PRE1 hold the prescalers count modulo, a value from 1 to 64 decimal. The prescaler registers also contain control bits that specify T0 and T1 counting modes. These bits also indicate whether the clock source for T_1 is internal or external. These control bits will be discussed in detail throughout this chapter.

The counter/timer registers, T0 (F4H) and T1 (F2H), each consist of an 8-bit down-counter, a write-only register that holds the initial count value, and a read-only register that holds the current count value (Figure 6-1). The initial value can range from 1 to 256 decimal (01H,02H,..,00H). Figure 6-5 illustrates the counter/timer registers.

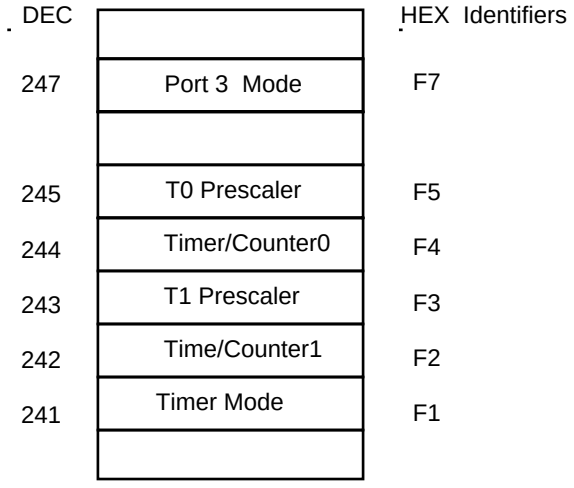

Figure 6-2. Counter/Timer Register Map

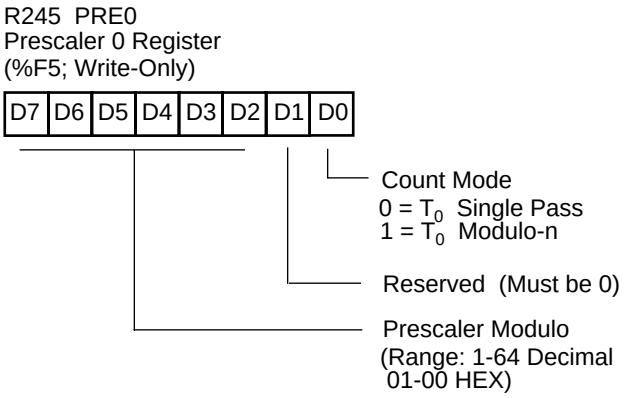

Figure 6-3. Prescaler 0 Register

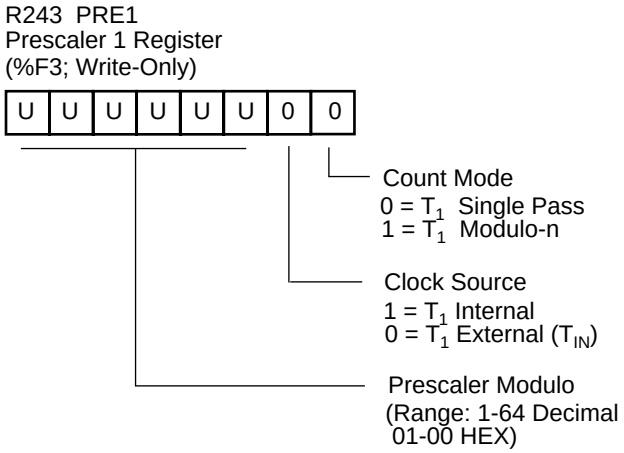

Figure 6-4. Prescaler 1 Register

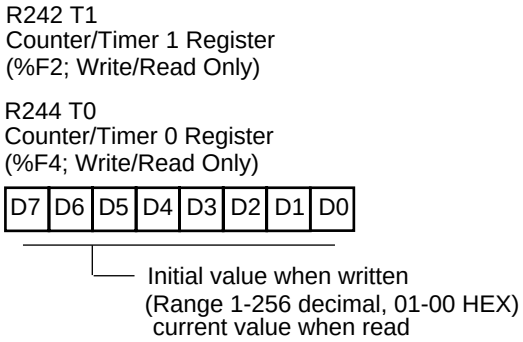

Figure 6-5. Counter / Timer 0 and 1 Registers

6.3 COUNTER/TIMER OPERATION

Under software control, counter/timers are started and stopped via the Timer Mode Register (TMR,F1H) bits D_0-D_3 (Figure 6-6). Each counter/timer is associated with a Load bit and an Enable Count bit.

6.3.1 Load and Enable Count Bits

Setting the Load bit (D_0 for T0 and D_2 for T1) transfers the initial value in the prescaler and the counter/timer registers into their respective down-counters. The next internal clock resets bits D_0 and D_2 to 0, readying the Load bit for the next load operation. New values may be loaded into the down-counters at any time. If the counter/timer is running, it continues to do so and starts the count over with the new value. Therefore, the Load bit actually functions as a software re-trigger.

The counter timers remain at rest as long as the Enable Count bits are 0. To enable counting, the Enable Count bit (D_1 for T0 and D_3 for T1) must be set to 1. Counting actually starts when the Enable Count bit is written by an instruction. The first decrement occurs four internal clock periods after the Enable Count bit has been set. If T1 is configured to use an external clock, the first decrement begins on the next clock period. The Load and Enable Count bits can be set at the same time. For example, using the instruction:

OR TMR,#03H

sets both D0 and D1 of the TMR. This loads the initial values of PRE0 and T0 into their respective counters and starts the count after the M2T2 machine state after the operand is fetched (Figure 6-7).

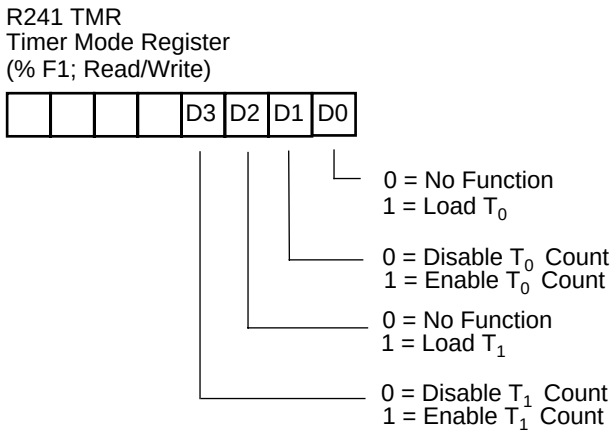

Figure 6-6. Timer Mode Register

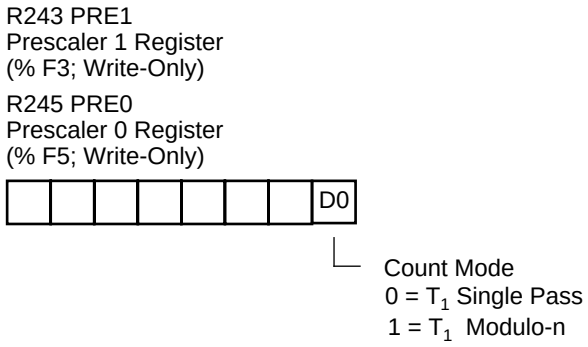

Figure 6-7. Starting The Count

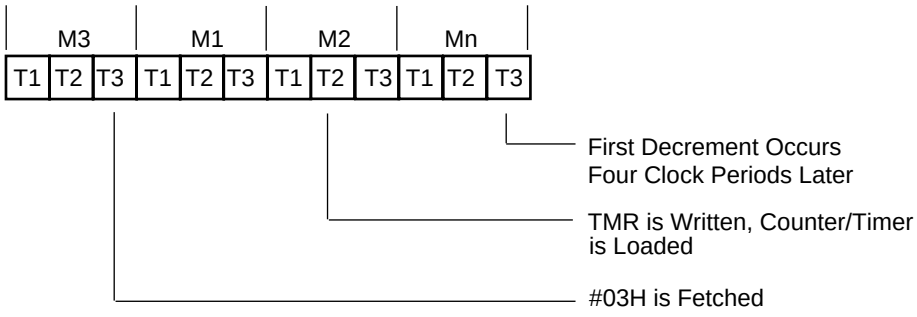

Figure 6-8. Counting Modes

6.3.2 Prescaler Operations

During counting, the programmed clock source drives the 6-bit Prescaler Counter. The counter is counted down from the value specified by bits of the corresponding Prescaler Register, PRE0 (bit 7 to bit 2) or PRE1 (bit 7 to bit 2). (Figures 6-3, 6-4). When the Prescaler Counter reaches its end-of-count, the initial value is reloaded and counting continues. The prescaler never actually reaches 0. For example, if the prescaler is set to divide-by-three, the count sequence is:

3–2–1–3–2–1–3–2–1–3...

Each time the prescaler reaches its end of count a carry is generated, that allows the Counter/Timer to decrement by one on the next timer clock input. When the Counter/Timer and the prescaler both reach the end-of-count, an interrupt request is generated (IRQ4 for T0, IRQ5 for T1). Depending on the counting mode selected, the Counter/Timer will either come to rest with its value at 00H (Single-Pass Mode) or the initial value will be automatically reloaded and counting will continue (Continuous Mode). The counting modes are controlled by bit 0 of PRE0 and bit 0 of PRE1. (Figure 6-8). A 0, written to this bit configures the counter for Single-pass counting mode, while a 1 written to this bit configures the counter for Continuous mode.

The Counter/Timer can be stopped at any time by setting the Enable Count bit to 0, and restarted by setting it back to 1. The Counter/Timer will continue its count value at the time it was stopped. The current value in the Counter/Timer can be read at any time without affecting the counting operation.

Note: The prescaler registers are write-only and cannot be read.

New initial values can be written to the prescaler or the Counter/Timer registers at any time. These values will be transferred to their respective down counters on the next load operation. If the Counter/Timer mode is continuous, the next load occurs on the timer clock following an end-of-count. New initial values should be written before the desired load operation, since the prescalers always effectively operate in Continuous count mode.

The time interval (i) until end-of-count, is given by the equation:

$i = t \times p \times v$

in which:

t = four times the internal clock period.

The internal clock frequency defaults to the external clock source (XTAL, ceramic resonator, and others) divided by 2. Some Z8® microcontrollers allow this divisor to be changed via the Stop-Mode Recovery register. See the product data sheet for available clock divisor options.

Note that t is equal to eight divided-by-XTAL frequency of the external clock source for T1 (external clock mode only).

p = the prescaler value (1 – 63) for T_0 and T_1.

The minimum prescaler count of 1 is achieved by loading 000001xx. The maximum prescaler count of 63 is achieved by loading 111111xx.

v = the Counter/Timer value (1-256)

Minimum duration is achieved by loading 01H (1 prescaler output count), maximum duration is achieved by loading 00H (256 prescaler outputs counts).

The prescaler and counter/timer are true divide-by-n counters.

6.4 T_{OUT} MODES

The Timer Mode Register TMR (F1H) (Figure 6-9), is used in conjunction with the Port 3 Mode Register P3M (F7H) (Figure 6-10) to configure P36 for T_{OUT} operation for T0 and T1. In order for T_{OUT} to function, P36 must be defined as an output line by setting P3M bit 5 to 0. Output is controlled by one of the counter/timers (T0 or T1) or the internal clock.

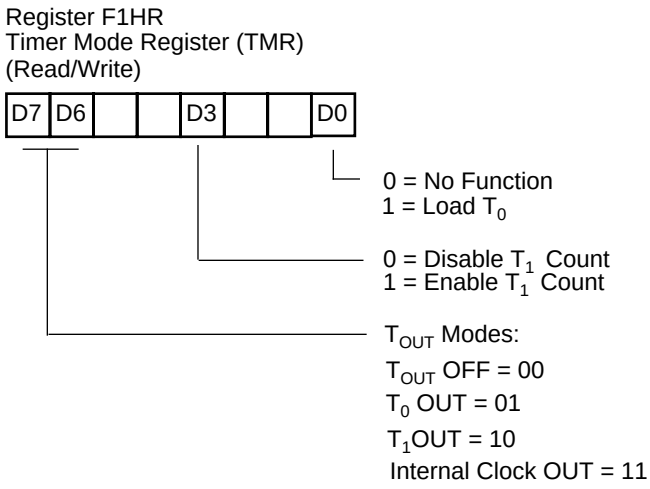

Figure 6-9. Timer Mode Register (T_{OUT} Operation)

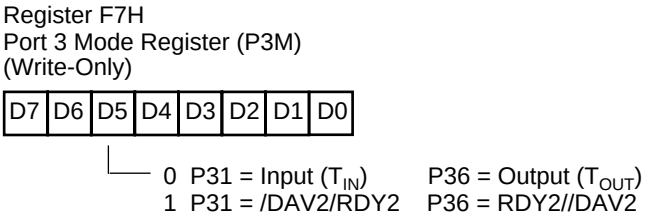

Figure 6-10. Port 3 Mode Register (T_{OUT} Operation)

6.4 T_{OUT} MODES (Continued)

The counter/timer to be output is selected by TMR bit 7 and bit 6. T0 is selected to drive the T_{OUT} line by setting bit 7 to 0 and bit 6 to 1. Likewise, T1 is selected by setting bit 7 and bit 6 to 1 and 0, respectively. The counter/timer T_{OUT} mode is turned off by setting TMR bit and bit 6 both to 0, freeing P36 to be a data output line.

T_{OUT} is initialized to a logic 1 whenever the TMR Load bit (bit 0 for T0 or bit 1 for T2) is set to 1. The T_{OUT} configuration timer load, and Timer Enable Count bits for the counter/timer driving the T_{OUT} pin can be set at the same time. For example, using the instruction:

OR TMR,#43H

- Configures T0 to drive the T_{OUT} pin (P36).
- Sets the P36 T_{OUT} pin to a logic 1 level.
- Loads the initial PRE0 and T0 levels into their respective counters and starts the counter after the M2T2 machine state after the operand is fetched.

At end-of-count, the interrupt request line (IRQ4 or IRQ5), clocks a toggle flip-flop. The output of this flip-flop drives the T_{OUT} line, P36. In all cases, when the selected counter/timer reaches its end-of-count, T_{OUT} toggles to its opposite state (Figure 6-11). If, for example, the counter/timer is in Continuous Counting Mode, Tout will have a 50 percent duty cycle output. This duty cycle can easily be controlled by varying the initial values after each end-of-count.

The internal clock can be selected as output instead of T0 or T1 by setting TMR bit 7 and bit 6 both to 1. The internal clock (XTAL frequency/2) is then directly output on P36 (Figure 6-12).

While programmed as T_{OUT}, P36 cannot be modified by a write to port register P3. However, the Z8® software can examine the P36 current output by reading the port register.

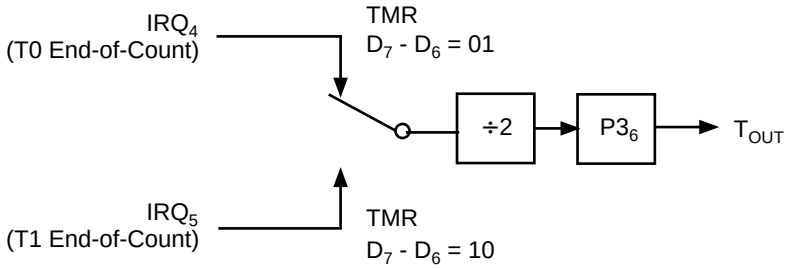

Figure 6-11. T0 and T1 Output Through T_{OUT}

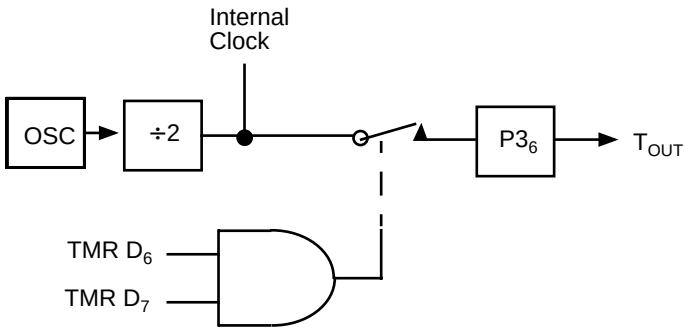

Figure 6-12. Internal Clock Output Through T_{OUT}

6.5 T_{IN} MODES

The Timer Mode Register TMR (F1H) (Figure 6-13) is used in conjunction with the Prescaler Register PRE1 (F3H) (Figure 6-14) to configure P31 as T_{IN}. T_{IN} is used in conjunction with T1 in one of four modes:

- External Clock Input
- Gated Internal Clock
- Triggered Internal Clock
- Retriggerable Internal Clock

Note: The T_{IN} mode is restricted for use with timer 1 only. To enable the T_{IN} mode selected (via TMR bits 4- 5), bit 1 of PRE1 must be set to 0.

The counter/timer clock source must be configured for external by setting the PRE1 Register bit 2 to 1. The Timer Mode Register bit 5 and bit 4 can then be used to select the desired T_{IN} operation.

For T1 to start counting as a result of a T_{IN} input, the Enable Count bit (bit 3 in TMR) must be set to 1. When using T_{IN} as an external clock or a gate input, the initial values must be loaded into the down counters by setting the Load bit (bit 2 in TMR) to a 1 before counting begins. In the descriptions of T_{IN} that follow, it is assumed the programmer has performed these operations. Initial values are automatically loaded in Trigger and Retrigger modes so software loading is unnecessary.

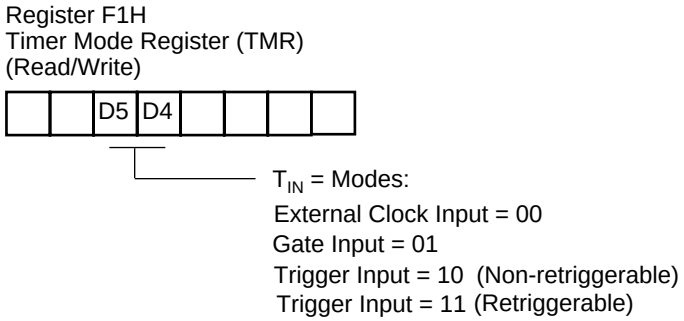

Figure 6-13. Timer Mode Register (T_{IN} Operation)

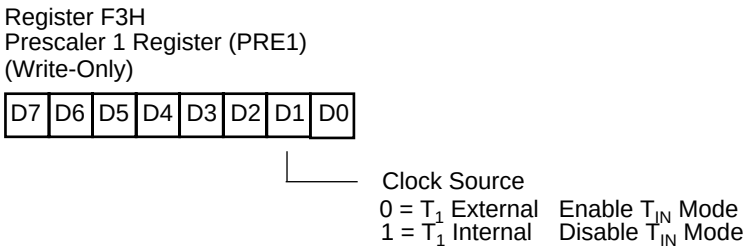

Figure 6-14. Prescaler 1 Register (T_{IN} Operation)

It is suggested that P31 be configured as an input line by setting P3M Register bit 5 to 0, although T_{IN} is still functional if P31 is configured as a handshake input.

Each High-to-Low transition on T_{IN} generates an interrupt request IRQ2, regardless of the selected T_{IN} mode or the enabled/disabled state of T1. IRQ2 must therefore be masked or enabled according to the needs of the application.

6.5.1 External Clock Input Mode

The T_{IN} External Clock Input Mode (TMR bit 5 and bit 4 both set to 0) supports counting of external events, where an event is considered to be a High-to-Low transition on T_{IN} (Figure 6-15).

Note: See the product data sheet for the minimum allowed T_{IN} external clock input period (T_P T_{IN}).

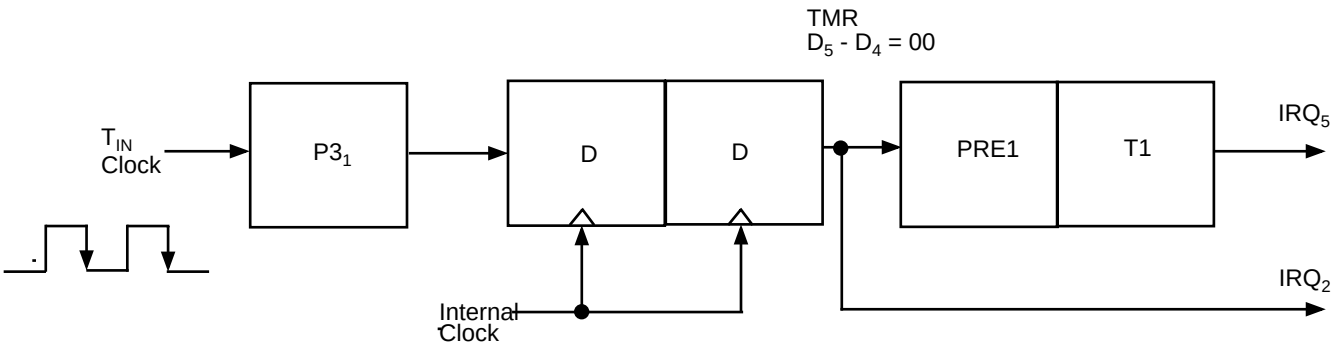

Figure 6-15. External Clock Input Mode

6.5.2 Gated Internal Clock Mode

The T_{IN} Gated Internal Clock Mode (TMR bit 5 and bit 4 set to 0 and 1 respectively) measures the duration of an external event. In this mode, the T1 prescaler is driven by the internal timer clock, gated by a High level on T_{IN} (Figure 6-16). T1 counts while T_{IN} is High and stops counting while T_{IN} is Low. Interrupt request IRQ2 is generated on the High-to-Low transition of T_{IN} signalling the end of the gate input. Interrupt request IRQ5 is generated if T1 reaches its end-of-count.

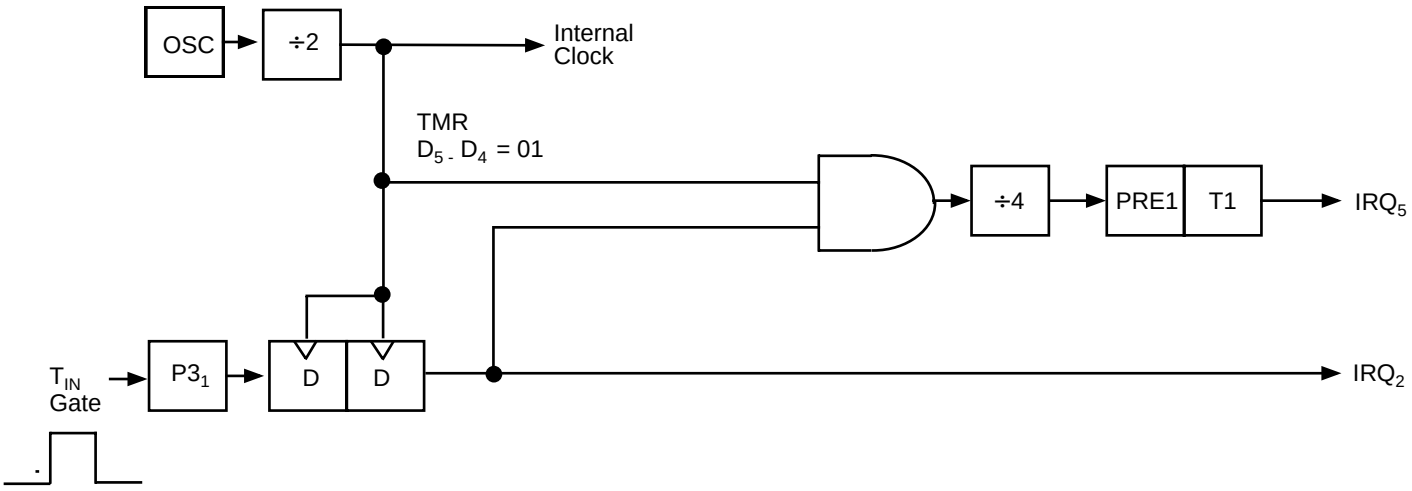

Figure 6-16. Gated Clock Input Mode

6.5.3 Triggered Input Mode

The T_{IN} Triggered Input Mode (TMR bits 5 and 4 are set to 1 and 0 respectively) causes T1 to start counting as the result of an external event (Figure 6-17). T1 is then loaded and clocked by the internal timer clock following the first High-to-Low transition on the T_{IN} input. Subsequent T_{IN} transitions do not affect T1. In the Single-Pass Mode, the Enable bit is reset whenever T1 reaches its end-of-count. Further T_{IN} transitions will have no effect on T1 until software sets the Enable Count bit again. In Continuous mode, once T1 is triggered counting continues until software resets the Enable Count bit. Interrupt request IRQ5 is generated when T1 reaches its end-of-count.

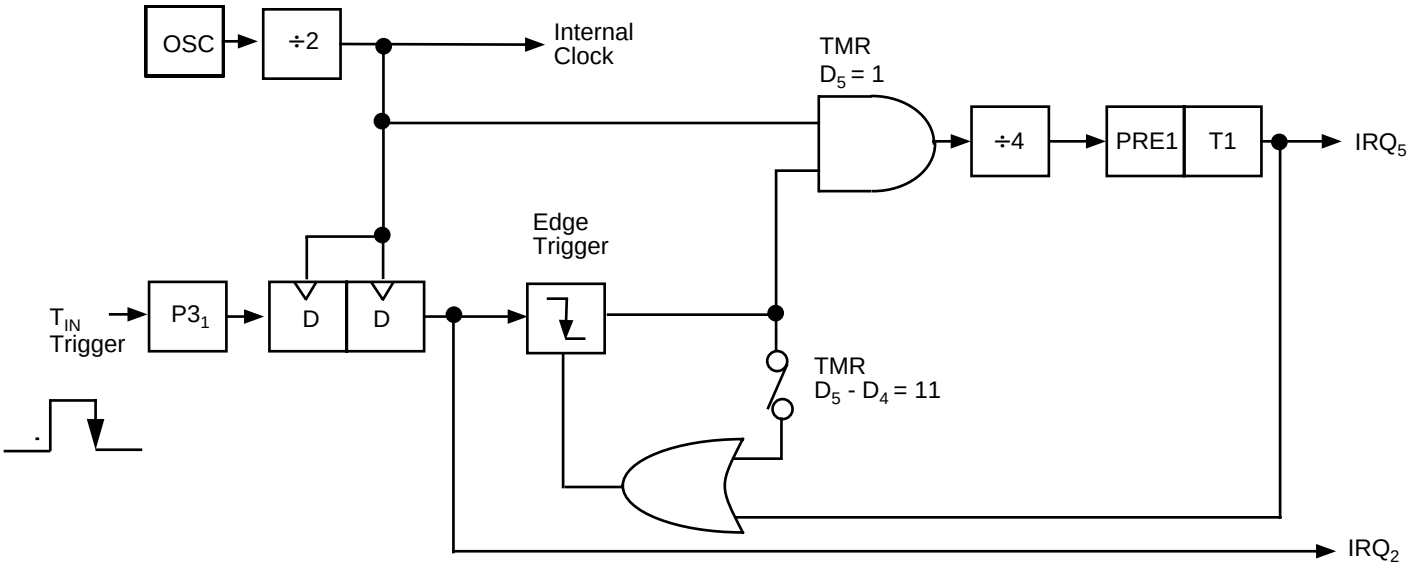

Figure 6-17. Triggered Clock Mode

6.5.4 Retriggerable Input Mode

The T_{IN} Retriggerable Input Mode (TMR bits 5 and 4 are set to 1) causes T1 to load and start counting on every occurrence of a High-to-Low transition on T_{IN} (Figure 6-17). Interrupt request IRQ5 will be generated if the programmed time interval (determined by T1 prescaler and counter/timer register initial values) has elapsed since the last High-to-Low transition on T_{IN}. In Single-Pass Mode, the end-of-count resets the Enable Count bit. Subsequent T_{IN} transitions will not cause T1 to load and start counting until software sets the Enable Count bit again. In Continuous Mode, counting continues once T1 is triggered until software resets the Enable Count bit. When enabled, each High-to-Low T_{IN} transition causes T1 to reload and restart counting. Interrupt request IRQ5 is generated on every end-of-count.

6.6 CASCADING COUNTER/TIMERS

For some applications, it may be necessary to measure a time interval greater than a single counter/timer can measure. In this case, T_{IN} and T_{OUT} can be used to cascade T0 and T1 as a single unit (Figure 6-18). T0 should be configured to operate in Continuous mode and to drive T_{OUT}. T_{IN} should be configured as an external clock input to T1 and wired back to T_{OUT}. On every other T0 end-of-count, T_{OUT} undergoes a High-to-Low transition that causes T1 to count.

T1 can operate in either Single-Pass or Continuous mode. When the T1 end-of-count is reached, interrupt request IRQ5 is generated. Interrupt requests IRQ2 (T_{IN} High-to-Low transitions) and IRQ4 (T0 end-of-count) are also generated but are most likely of no importance in this configuration and should be disabled.

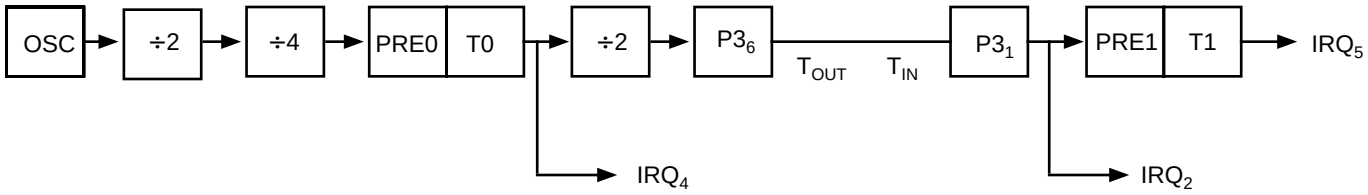

Figure 6-18. Cascaded Counter / Timers

6.7 RESET CONDITIONS

After a hardware reset, the counter/timers are disabled and the contents of the counter/timer and prescaler registers are undefined. However, the counting modes are configured for Single-Pass and the T1 clock source is set for external.

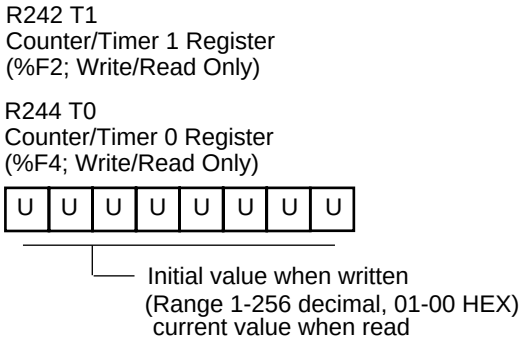

Figure 6-19. Counter / Timer Reset

T_{IN} is set for External Clock mode, and the T_{OUT} mode is off. Figures 6-19 through 6-22 show the binary reset values of the Prescaler, Counter/Timer, and Timer Mode registers.

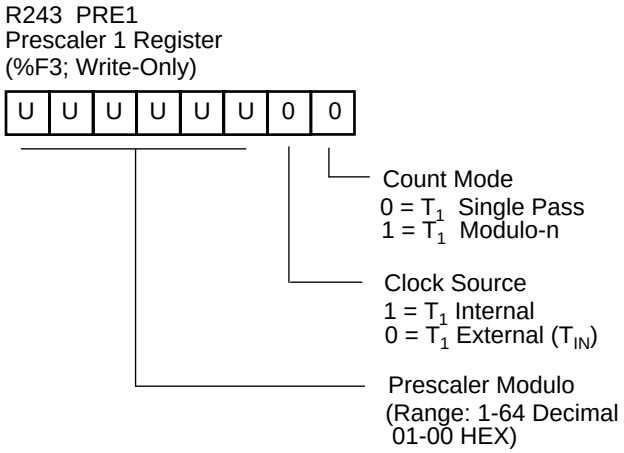

Figure 6-20. Prescaler 1 Register Reset

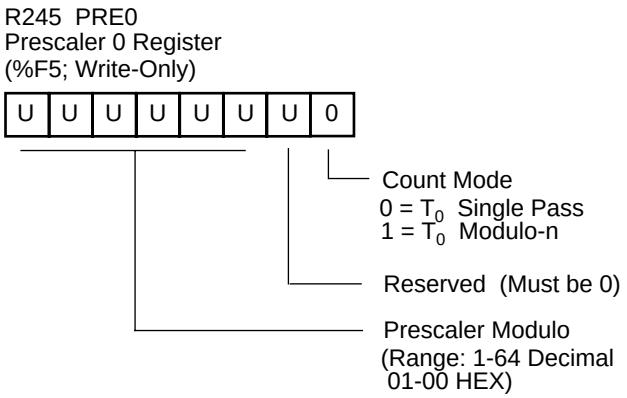

Figure 6-21. Prescaler 0 Reset

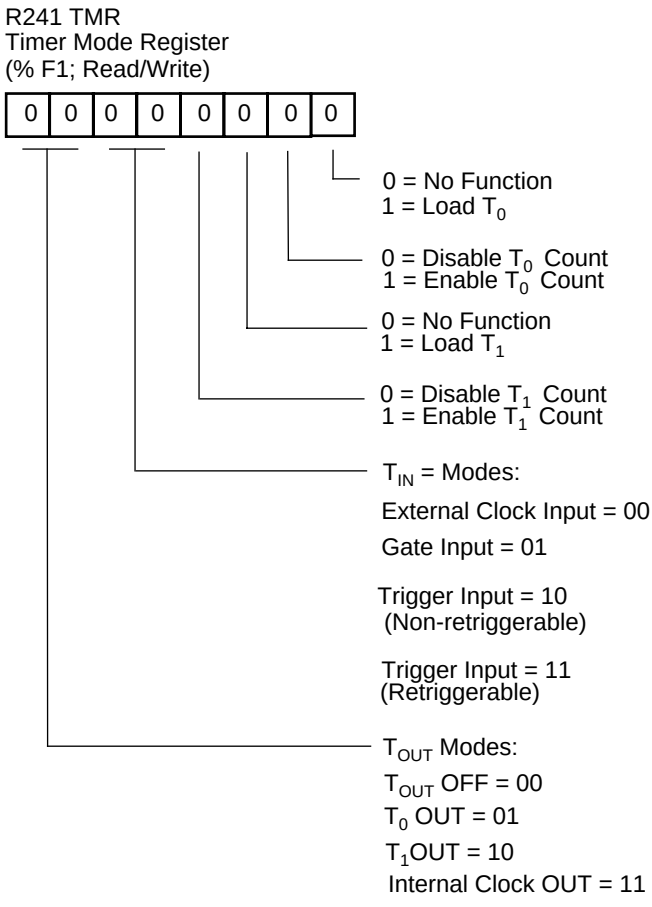

Figure 6-22. Timer Mode Register Reset