CHAPTER 5
I/O PORTS

5.1 I/O PORTS

The Z8® has up to 32 lines dedicated to input and output. These lines are grouped into four 8-bit ports known as Port 0, Port 1, Port 2, and Port 3. Port 0 is nibble programmable as input, output, or address. Port 1 is byte configurable as input, output, or address/data. Port 2 is bit programmable as either inputs or outputs, with or without handshake and SPI. Port 3 can be programmed to provide timing, serial and parallel input/output, or comparator input/output.

All ports have push-pull CMOS outputs. In addition, the push-pull outputs of Port 2 can be turned off for open-drain operation.

5.1.1 Mode Registers

Each port has an associated Mode Register that determines the port's functions and allows dynamic change in port functions during program execution. Port and Mode Registers are mapped into the Standard Register File as shown in Figure 5-1.

Register	HEX	Identifier
Port 0-1 Mode	F8H	P01M
Port 3 Mode	F7H	P3M
Port 2 Mode	F6H	P2M
Port 3	03H	P3
Port 2	02H	P2
Port 1	01H	P1
Port 0	00H	P0

Figure 5-1. I/O Ports and Mode Registers

Because of their close association, Port and Mode Registers are treated like any other general-purpose register. There are no special instructions for port manipulation. Any instruction which addresses a register can address the ports. Data can be directly accessed in the Port Register, with no extra moves.

5.1.2 Input and Output Registers

Each bit of Ports 0, 1, and 2, have an input register, an output register, associated buffer, and control logic. Since there are separate input and output registers associated with each port, writing to bits defined as inputs stores the data in the output register. This data cannot be read as long as the bits are defined as inputs. However, if the bits are reconfigured as outputs, the data stored in the output register is reflected on the output pins and can then be read. This mechanism allows the user to initialize the outputs prior to driving their loads (Figure 5-2).

Since port inputs are asynchronous to the Z8 internal clock, a READ operation could occur during an input transition. In this case, the logic level might be uncertain (somewhere between a logic 1 and 0). To eliminate this meta-stable condition, the Z8 latches the input data two clock periods prior to the execution of the current instruction. The input register uses these two clock periods to stabilize to a legitimate logic level before the instruction reads the data.

Note: The following sections describe the generic function of the Z8 ports. Any additional features of the ports such as SPI, C/T, and Stop-Mode Recovery are covered in their own section.

5.2 PORT 0

This section deals with only the I/O operation of Port 0. The port's external memory interface operation is covered later in this manual. Figure 5-2 shows a block diagram of Port 0. This diagram also applies to Ports 1 and 2.

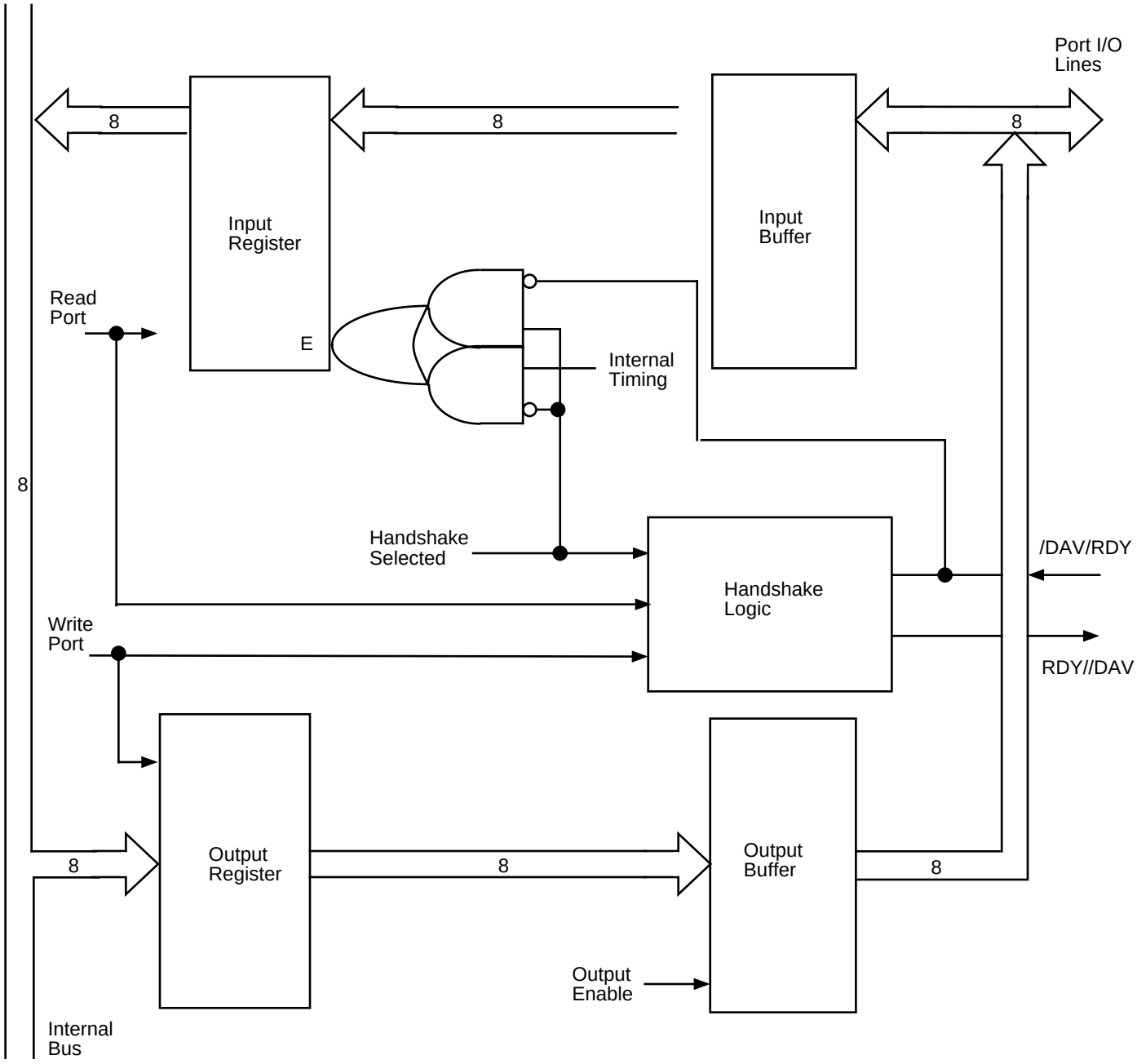


Figure 5-2. Ports 0, 1, 2 Generic Block Diagram

5.2.1 General I/O Mode

Port 0 can be an 8-bit, bidirectional, CMOS or TTL compatible I/O port. These eight I/O lines can be configured under software control as a nibble I/O port (P03-P00 input/output and P07-P04 input/output), or as an address port for interfacing external memory. The input buffers can be Schmitt-triggered, level shifted, or a single-trip point buffer and can be nibble programmed. Either nibble output can be globally programmed as push-pull or open-drain. Low EMI output buffers in some cases can be globally programmed by the software, as an OTP program option, or as a ROM mask option. In some, the Z8® has Auto Latches hardwired to the inputs. Please refer to specific product specifications for exact input/output buffer type features that are available (Figures 5-3 and 5-4).

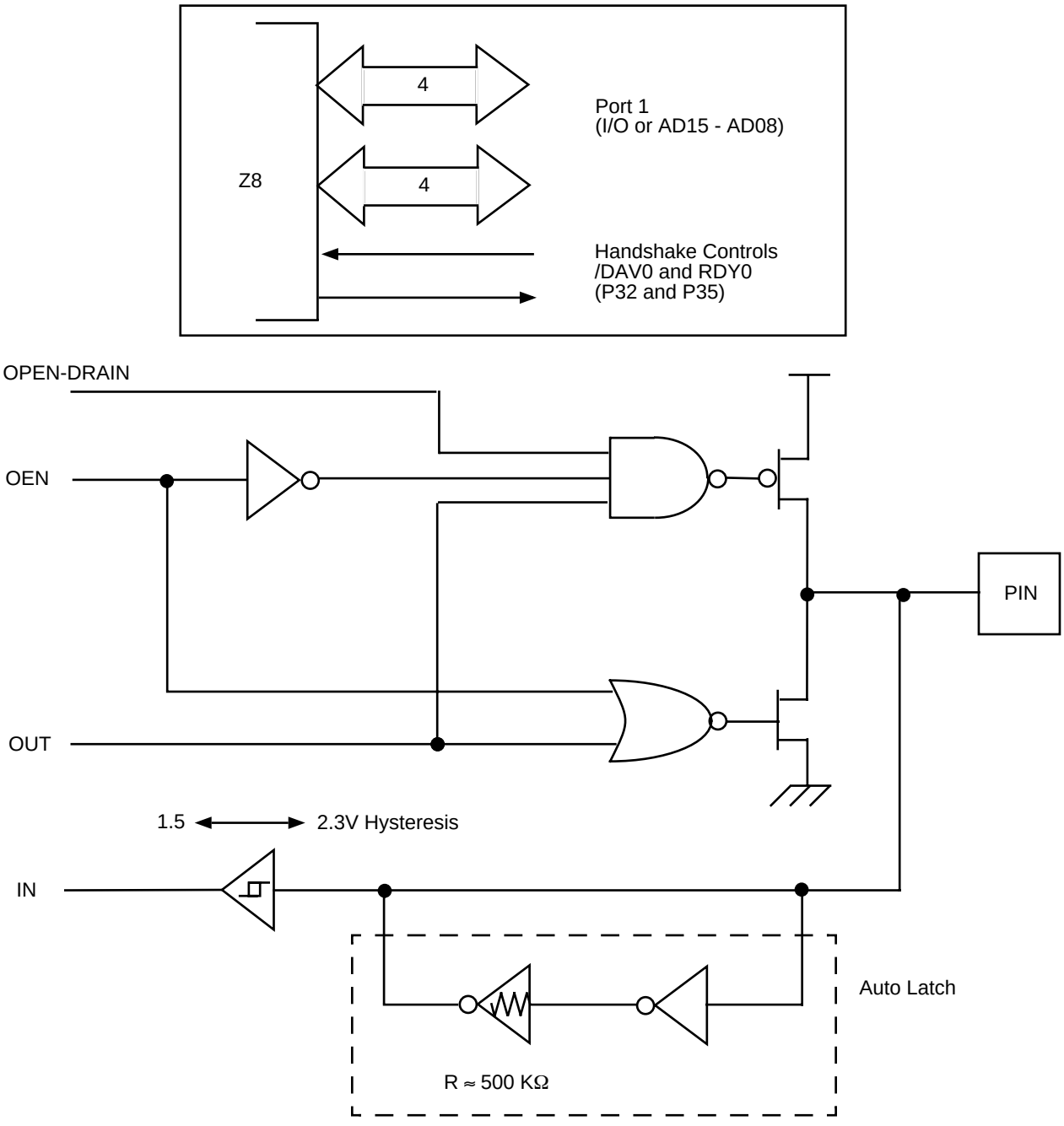


Figure 5-3. Port 0 Configuration with Open-Drain Capability, Auto Latch, and Schmitt-Trigger

5.2 PORT 0 (Continued)

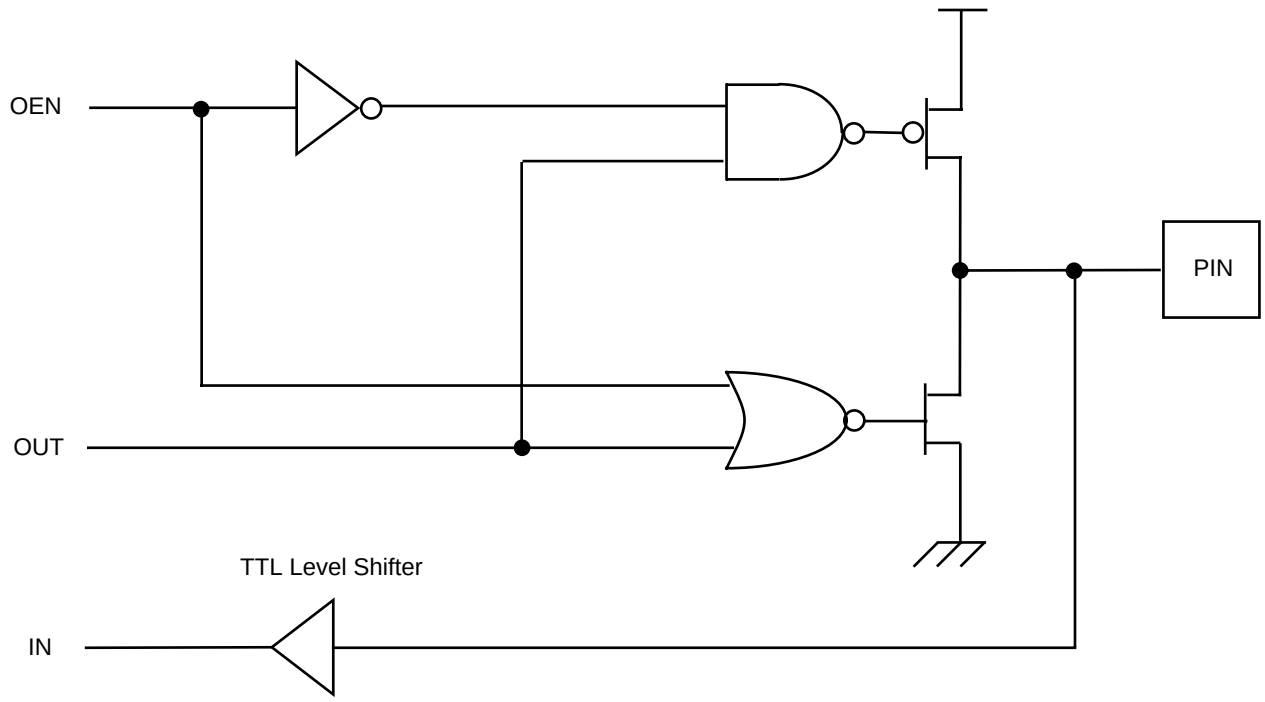


Figure 5-4. Port 0 Configuration with TTL Level Shifter

5.2.2 Read/Write Operations

In the nibble I/0 Mode, Port 0 is accessed as general-purpose register P0 (00H) with ERF Bank set to 0. The port is written by specifying P0 as an instruction's destination register. Writing to the port causes data to be stored in the port's output register.

The port is read by specifying P0 as the source register of an instruction. When an output nibble is read, data on the external pins is returned. Under normal loading conditions this is equivalent to reading the output register. However, for Port 0 outputs defined as open–drain, the data returned is the value forced on the output by the external system. This may not be the same as the data in the output register. Reading a nibble defined as input also returns data on the external pins. However, input bits under handshake control return data latched into the input register via the input strobe.

The Port 0–1 Mode resister bits D_1D_0 and D_7D_6 are used to configure Port 0 nibbles. The lower nibble ($P0_0$–$P0_3$) can be defined as inputs by setting bits D_1 to 0 and D_0 to 1, or as outputs by setting both D_1 and D_0 to 0. Likewise, the upper nibble ($P0_4$–$P0_7$) can be defined as inputs by setting bits D_7 to 0 and D_6 to 1, or as outputs by setting both D_6 and D_7 to 0 (Figure 5-5).

5.2.3 Handshake Operation

When used as an I/0 port, Port 0 can be placed under handshake control by programming the Port 3 Mode register bit D_2 to 1. In this configuration, handshake control lines are DAV_0 ($P3_2$) and RDY_0 ($P3_5$) when Port 0 is an input port, or RDY_0 ($P3_2$) and DAV_0 ($P3_5$) when Port 0 is an output port. (See Figure 5-6)

Handshake direction is determined by the configuration (input or output) assigned to the Port 0 upper nibble, $P0_4$–$P0_7$. The lower nibble must have the same I/0 configuration as the upper nibble to be under handshake control. Figure 5-3 illustrates the Port 0 upper and lower nibbles and the associated handshake lines of Port 3.

5.3 PORT 1

This section deals only with the I/0 operation. The port's external memory interface operation is discussed later in this manual. Figure 5-2 shows a block diagram of Port 1.

5.3.1 General I/O Mode

Port 1 can be an 8-bit, bidirectional, CMOS or TTL compatible port with multiplexed Address (A7–A0) and Data (D7–D0) ports. These eight I/O lines can be byte programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing to external memory. The input buffers can be Schmitt-triggered, level- shifted, or a single-point buffer. In some cases, the output buffers can be globally programmed as either push-pull or open-drain. Low-EMI output buffers can be globally programmed by software, as an OTP program option, or as a ROM Mask Option. In some cases, the Z8® can have auto latches hardwired to the inputs. Please refer to specific product specifications for exact input/output buffer-type features available (Figures 5-7 and 5-8).

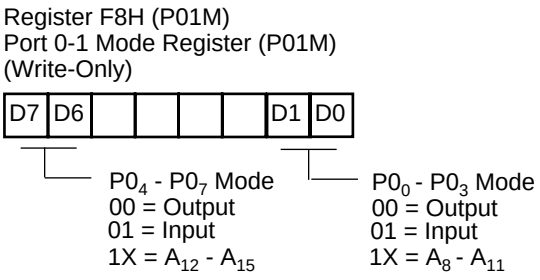


Figure 5-5. Port 0 I/O Operation

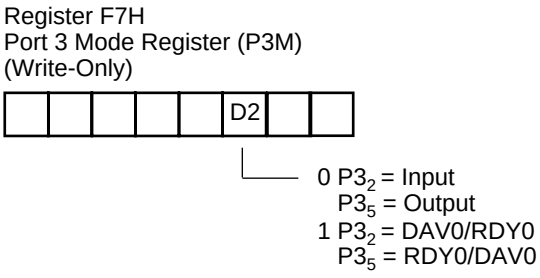


Figure 5-6. Port 0 Handshake Operation

5.3 PORT 1 (Continued)

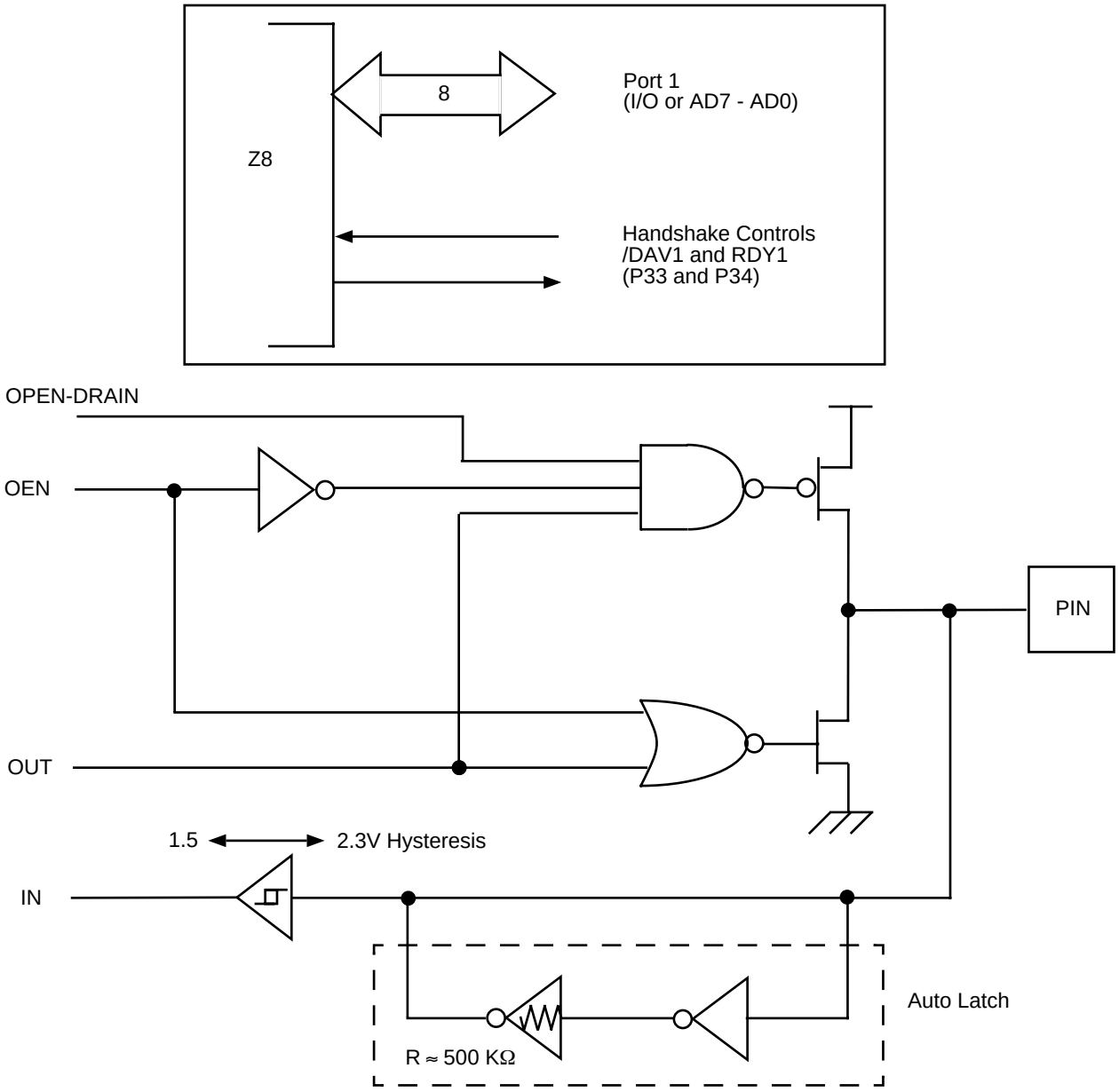


Figure 5-7. Port 1 Configuration with Open-Drain Capability, Auto Latch, and Schmitt-Trigger

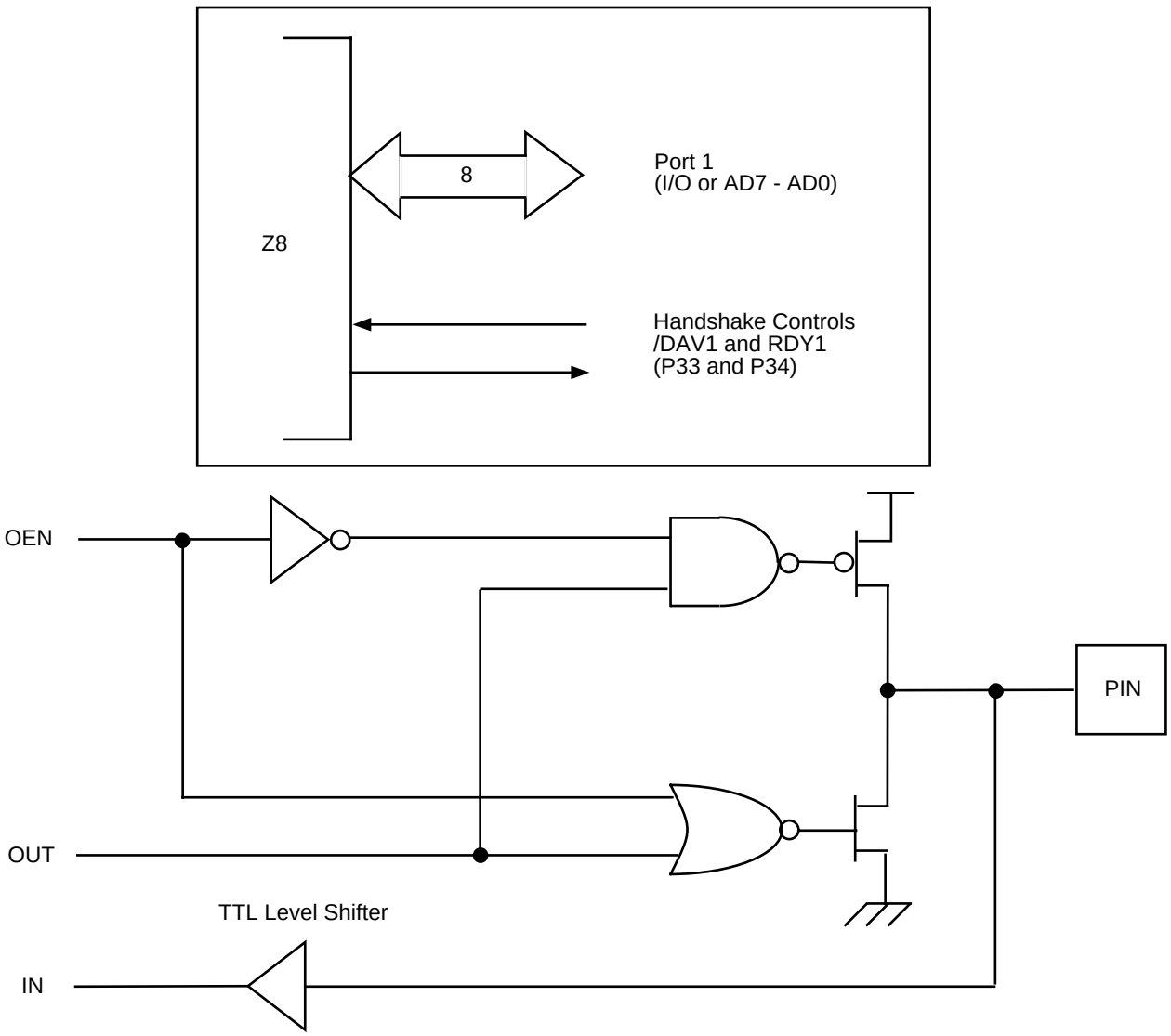


Figure 5-8. Port 1 Configuration with TTL Level Shifter

5.3.2 Read/Write Operations

In byte input or byte output mode, the port is accessed as General-Purpose Register P1 (01H). The port is written by specifying P1 as an instruction's destination register. Writing to the port causes data to be stored in the port's output register.

The port is read by specifying P1 as the source register of an instruction. When an output is read, data on the external pins is returned. Under normal loading conditions, this is equivalent to reading the output register. However, if Port 1 outputs are defined as open-drain, the data returned is the value forced on the output by the external system. This may not be the same as the data in the output register. When Port 1 is defined as an input, reading also returns data on the external pins. However, inputs under handshake control return data latched into the input register via the input strobe.

Using the Port 0-1 Mode Register, Port 1 is configured as an output port by setting bits D_4 and D_3 to 0, or as an input port by setting D_4 to 0 and D_3 to 1 (Figure 5-8).

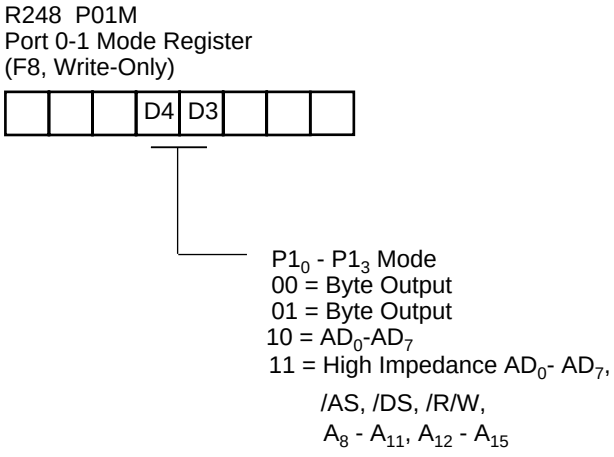


Figure 5-9. Port 1 I/O Operation

5.3.3 Handshake Operations

When used as an I/O port, Port 1 can be placed under handshake control by programming the Port 3 Mode register bits D_4 and D_3 both to 1. In this configuration, handshake control lines are DAV$_1$ (P3$_3$) and RDY1 (P3$_4$) when Port 1 is an input port, or RDY*1* (P3$_3$) and DAV1 (P3$_4$) when Port 1 is an output port. See Figures 5-8 and 5-10.

Handshake direction is determined by the configuration (input and output) assigned to Port 1. For example, if Port 1 is an output port then handshake is defined as output.

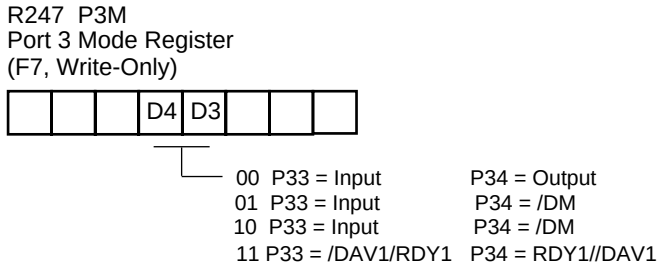


Figure 5-10. Handshake Operation

5.4 PORT 2

Port 2 is a general-purpose port. Figure 5-2 shows a block diagram of Port 2. Each of its lines can be independently programmed as input or output via the Port 2 Mode Register (F6H) as seen in Figure 5-11. A bit set to a 1 in P2M configures the corresponding bit in Port 2 as an input, while a bit set to 0 configures an output line.

Register F6H
Port 2 Mode Register (P2M)
(Write-Only)

D7	D6	D5	D4	D3	D2	D1	D0

Port 2 Mode
0 = Output
1 = Input

5.4.1 General Port I/O

Port 2 can be an 8-bit, bidirectional, CMOS- or TTL- compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Input buffers can be Schmitt-triggered, level-shifted, or a single trip point buffer and may contain Auto Latches. Bits programmed as outputs may be globally programmed as either push-pull or open-drain. Low-EMI output buffers can be globally programmed by the software, an OTP program option, or as a ROM mask option. In addition, when the SPI is featured and enabled, P20 functions as data-in (DI), and P27 functions as data-out (DO). Please refer to specific product specifications for exact input/output buffer type features available. See Figures 5-12 through 5-14.

Figure 5-11. Port 2 I/O Mode Configuration

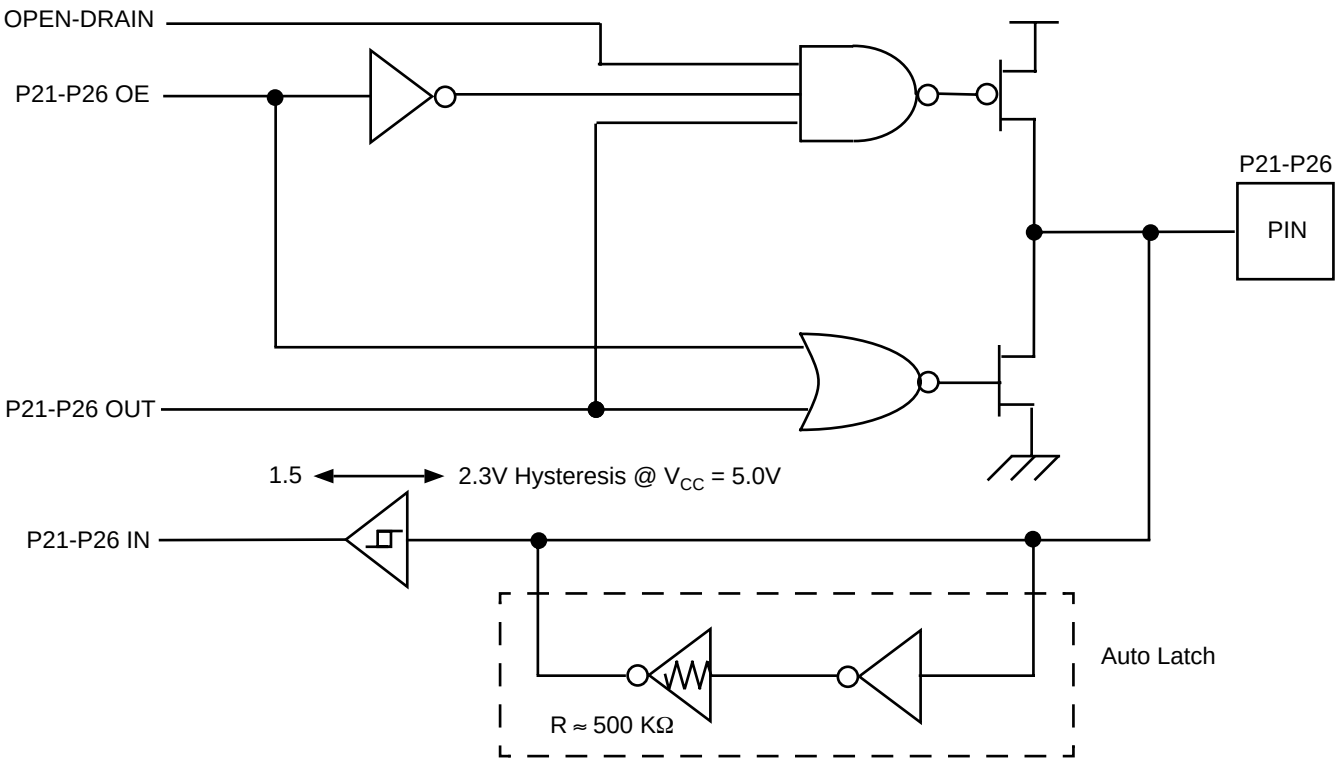


Figure 5-12. Port 2 Configuration with Open-Drain Capability, Auto Latch, and Schmitt-Trigger

5.4 PORT 2 (Continued)

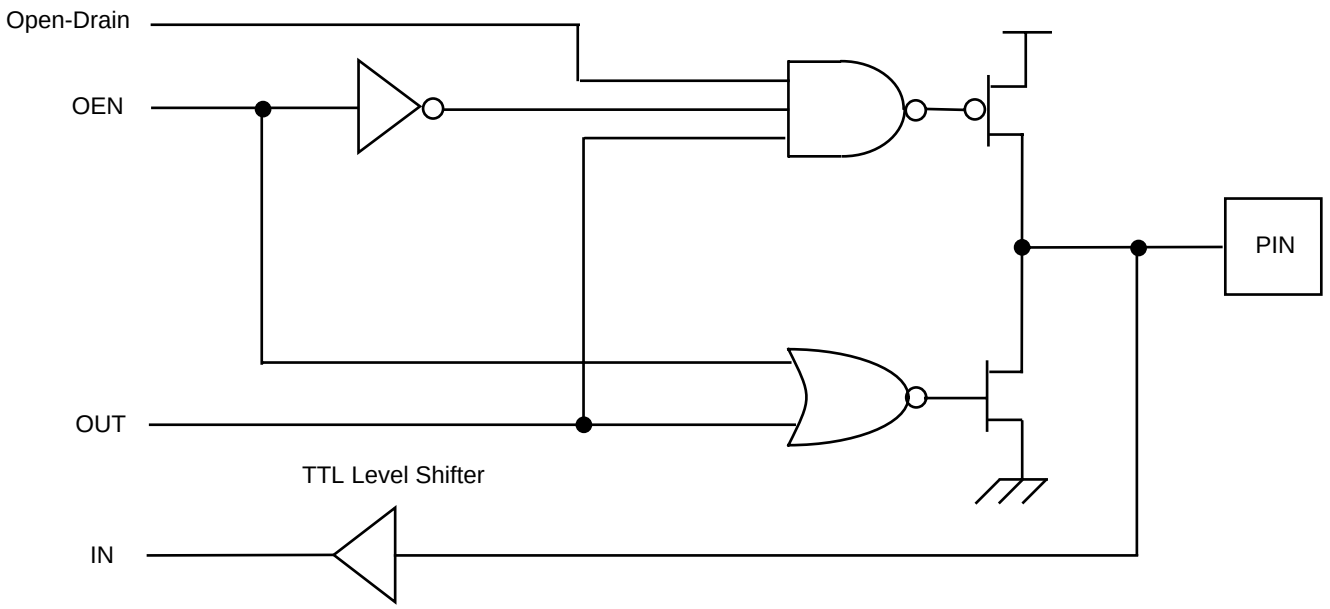


Figure 5-13. Port 2 Configuration with TTL Level Shifter

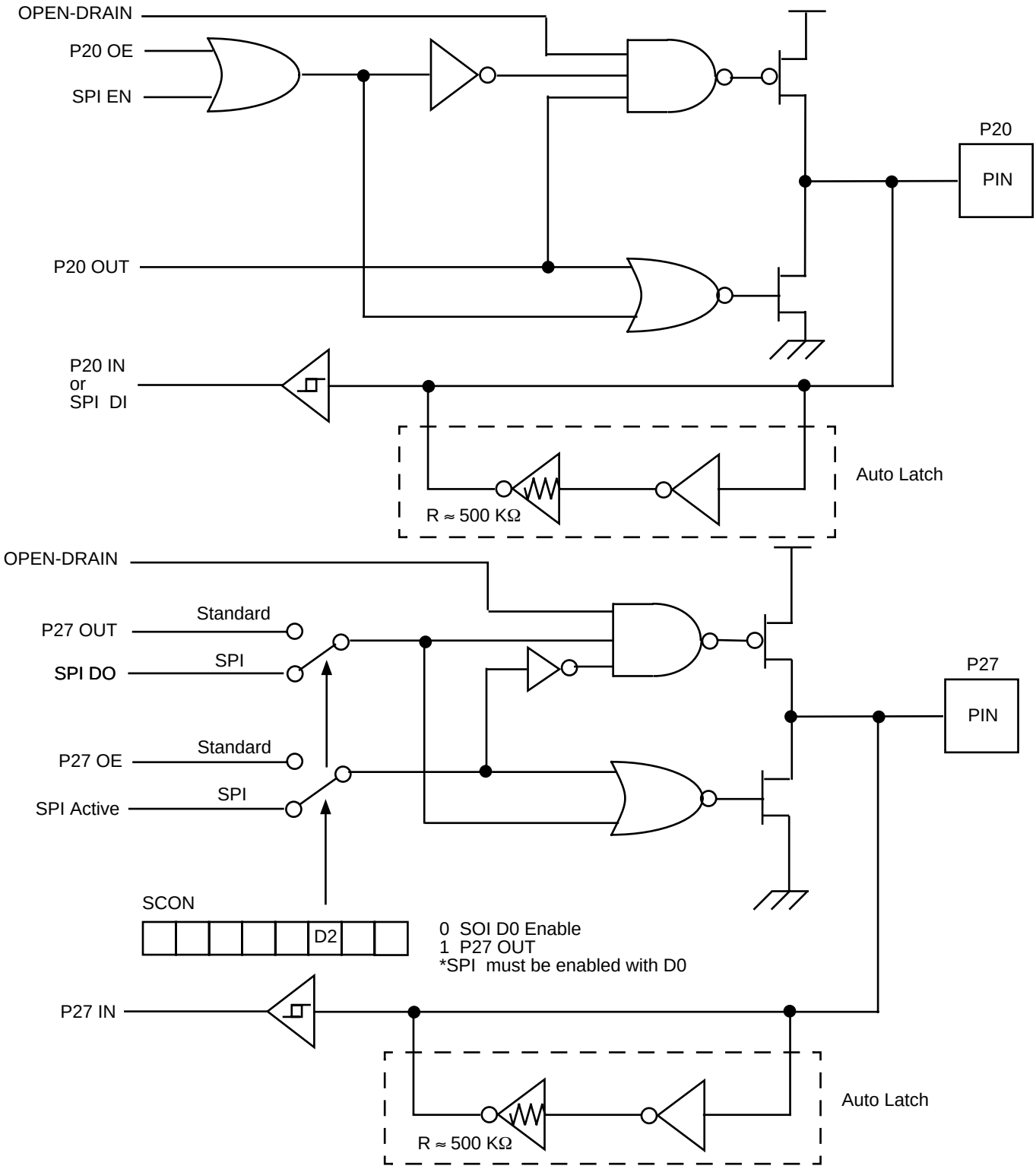


Figure 5-14. Port 2 Configuration with Open-Drain Capability, Auto Latch, Schmitt-Trigger and SPI

5.4.2 Read/Write Operations

Port 2 is accessed as General-Purpose Register P2 (02H). Port 2 is written by specifying P2 as an instruction's destination register. Writing to Port 2 causes data to be stored in the output register of Port 2, and reflected externally on any bit configured as an output.

Port 2 is read by specifying P2 as the source register of an instruction. When an output bit is read, data on the external pin is returned. Under normal loading conditions, this is equivalent to reading the output register. However, if a bit of Port 2 is defined as an open-drain output, the data returned is the value forced on the output pin by the external system. This may not be the same as the data in the output register. Reading input bits of Port 2 also returns data on the external pins. However, inputs under handshake control return data latched into the input register via the input strobe.

5.4.3 Handshake Operation

Port 2 can be placed under handshake control by programming bit 6 in the Port 3 Mode Register (Figure 5-15). In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2 for input handshake, or RDY2 and /DAV2 for output handshake.

Handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2. Only those bits with the same configuration as P27 will be under handshake control. Figure 5-16 illustrates bit lines of Port 2 and the associated handshake lines of Port 3.

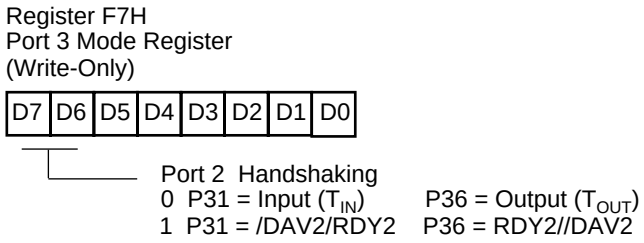


Figure 5-15. Port 2 Handshake Configuration

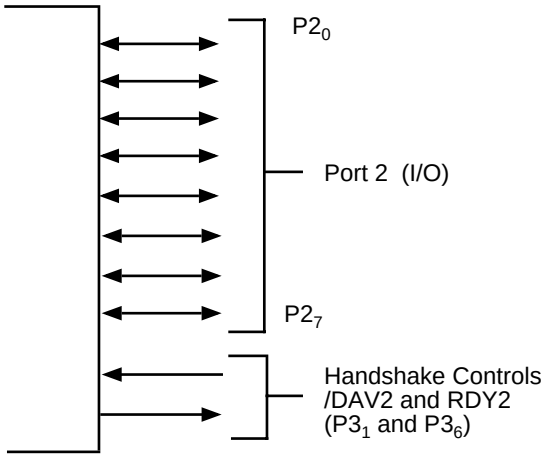


Figure 5-16. Port 2 Handshaking

5.5 PORT 3

5.5.1 General Port I/O

Port 3 differs structurally from Port 0, 1, and 2. Port 3 lines are fixed as four inputs (P33–P30) and four outputs (P37–P34) Port 3 does not have an input and output register for each bit. Instead, all the input lines have one input register, and all the output lines have an output register. Port 3 can be a CMOS- or TTL- compatible I/O port. Under software control, the lines can be configured as special control lines for handshake, comparator inputs, SPI control, external memory status, or I/O lines for the on-board serial and timer facilities. Figure 5-17 is a generic block diagram of Port 3.

The inputs can be Schmitt-triggered, level-shifted, or single-trip point buffered. In some cases, the Z8® may have auto latches hardwired on certain Port 3 inputs and Low-EMI capabilities on the outputs. Please refer to specific product specifications for exact input/output buffer type features. Please refer to the section on counter/timers, Stop-Mode Recovery, serial I/O, comparators, and interrupts for more information on the relationships of Port 3 to that feature.

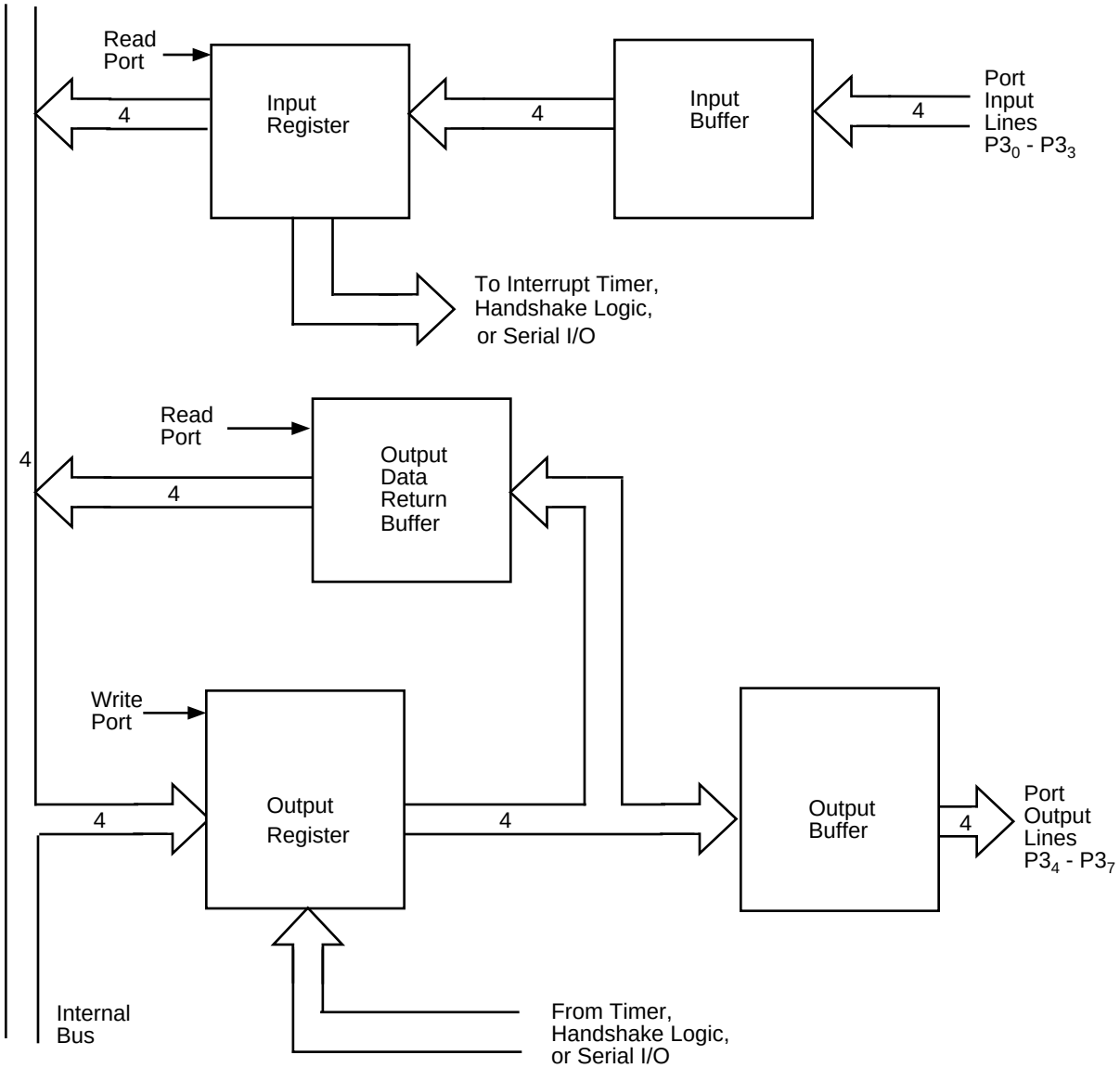


Figure 5-17. Port 3 Block Diagram

5.5 PORT 3 (Continued)

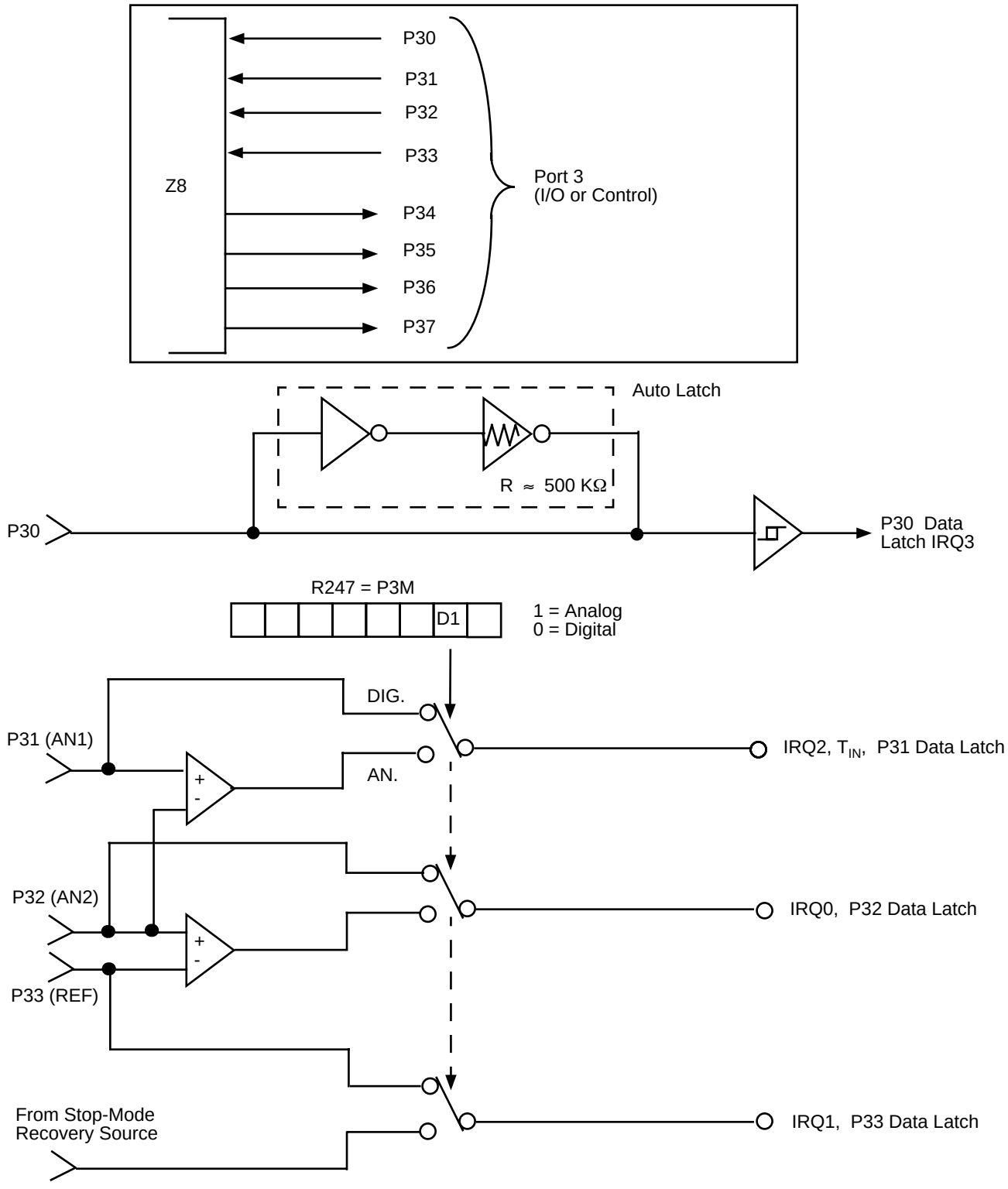


Figure 5-18. Port 3 Configuration with Comparator, Auto Latch, and Schmitt-Trigger

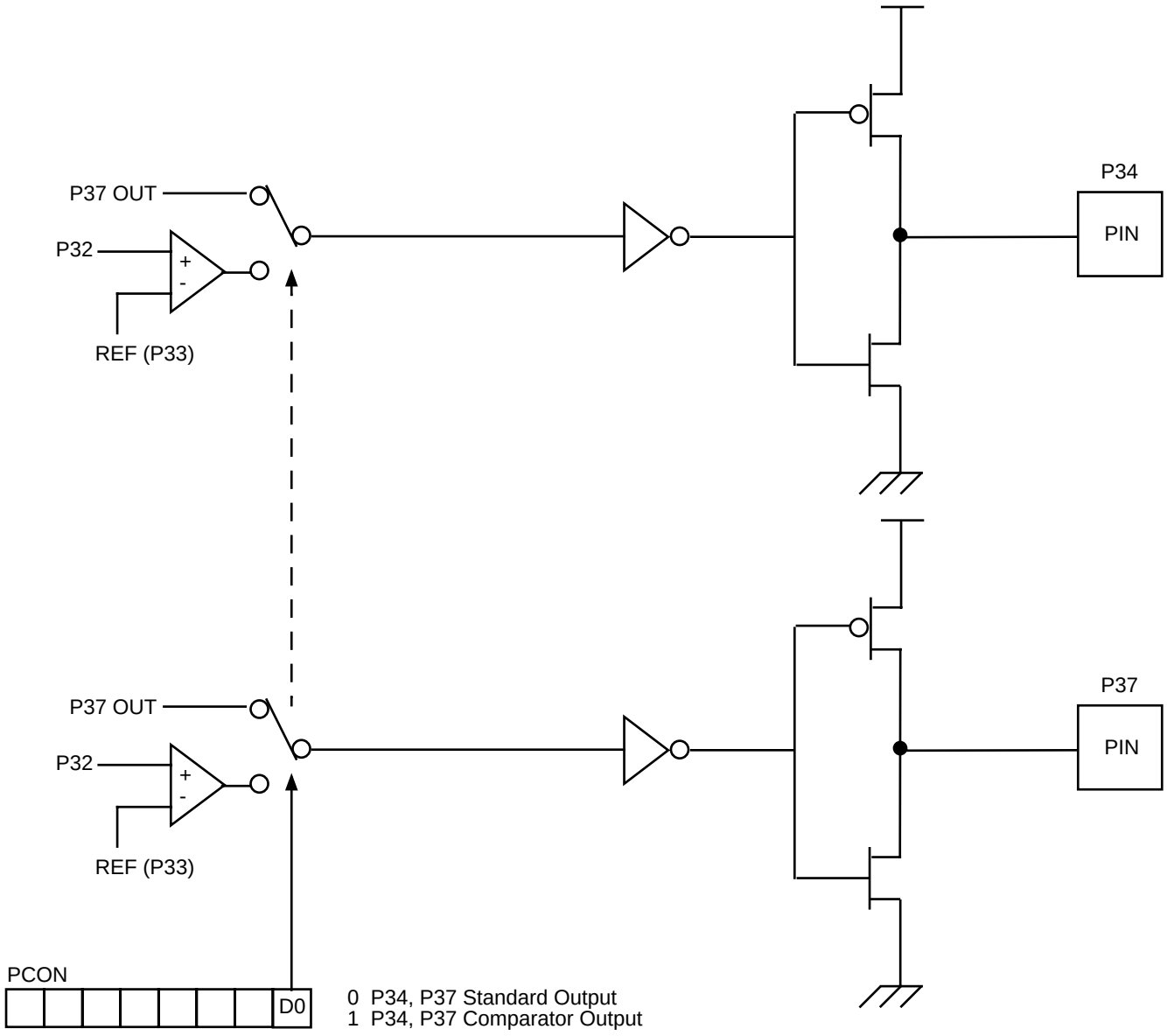


Figure 5-19. Port 3 Configuration with Comparator

5.5 PORT 3 (Continued)

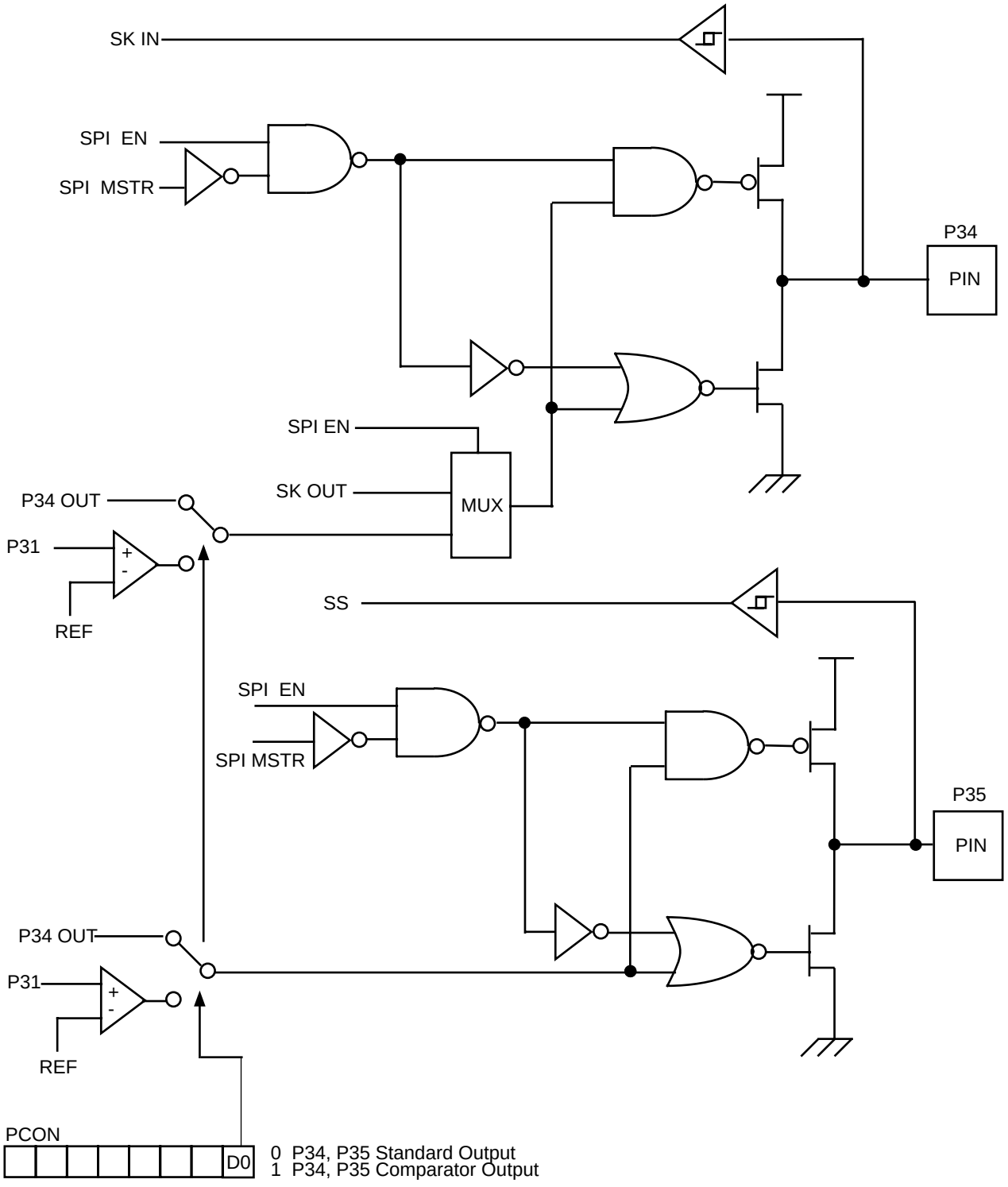


Figure 5-20. Port 3 Configuration with SPI and Comparator Outputs Using P34 and P35

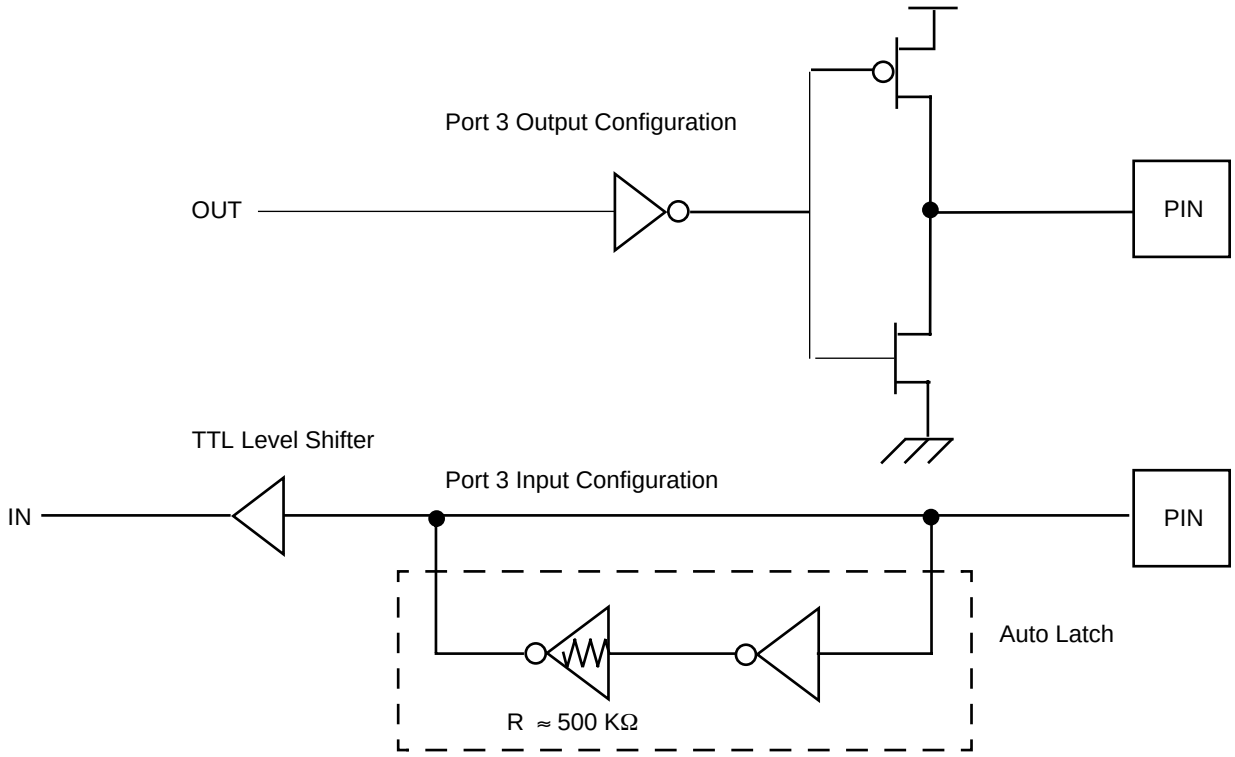


Figure 5-21. Port 3 Configuration with TTL Level Shifter and Auto Latch

5.5.2 Read/Write Operations

Port 3 is accessed as a General-Purpose Register P3 (03H). Port 3 is written by specifying P3 as an instruction's destination register. However, Port 3 outputs cannot be written to if they are used for special functions. When writing to Port 3, data is stored in the output register.

Port 3 is read by specifying P3 as the source register of an instruction. When reading from Port 3, the data returned is both the data on the input pins and in the output register.

5.5.3 Special Functions

Special functions for Port 3 are defined by programming the Port 3 Mode Register. By writing 0s in bit 6 through bit 1, lines P37–P30 are configured as input/output pairs (Figure 5-22). Table 5-1 shows available functions for Port 3. The special functions indicated in the figure are discussed in detail in their corresponding sections in this manual.

Port 3 input lines P33–P30 always function as interrupt requests regardless of the configuration specified in the Port 3 Mode Register.

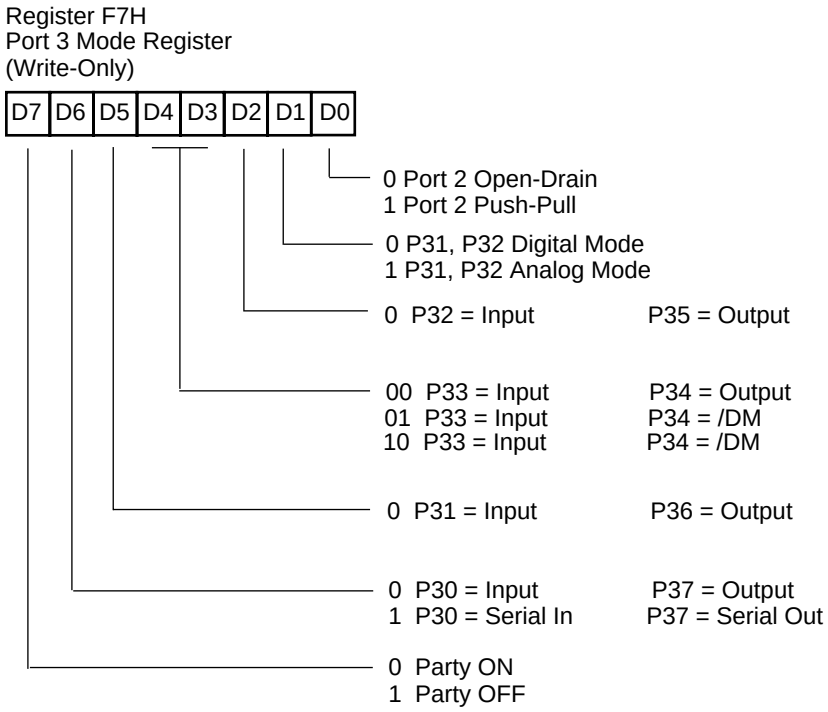


Figure 5-22. Port 3 Mode Register Configuration

Table 5-1. Port 3 Line Functions

Function	Line	Signal
Inputs	P30	Input
	P31	Input
	P32	Input
	P33	Input
Outputs	P34	Output
	P35	Output
	P36	Output
	P37	Output
Port 0 Handshake Input	P32	/DAV0/RDY0
Port 1 Handshake Input	P33	/DAV1/RDY1
Port 2 Handshake Input	P31	/DAV2/RDY2
Port 0 Handshake Output	P35	RDY0//DAV0
Port 1 Handshake Output	P34	RDY1//DAV1
Port 2 Handshake Output	P36	RDY2//DAV2
Analog Comparator Input	P31	AN1
	P32	AN2
	P33	REF
Analog Comparator Output	P34	AN1-OUT
	P35	AN2-OUT
	P37	AN2-OUT
Interrupt Requests	P30	IRQ3
	P31	IRQ2
	P32	IRQ0
	P33	IRQ1
Serial Input (UART)	P30	DI
Serial Output (UART)	P37	DO
SPI Slave Select	P35	SS
SPI Clock	P34	SK
Counter/Timer	P31	T_{IN}
	P36	T_{OUT}
External Memory Status	P34	/DM

5.6 PORT HANDSHAKE

When Ports 0, 1, and 2 are configured for handshake operation, a pair of lines from Port 3 are used for handshake controls. The handshake controls are interlocked to properly time asynchronous data transfers between the Z8® and a peripheral. One control line (/DAV) functions as a strobe from the sender to indicate to the receiver that data is available. The second control line (RDY) acknowledges receipt of the sender's data, and indicates when the receiver is ready to accept another data transfer.

In the input mode, data is latched into the Port's input register by the first /DAV signal, and is protected from being overwritten if additional pulses occur on the /DAV line. This overwrite protection is maintained until the port data is read. In the output mode, data written to the port is not protected and can be overwritten by the Z8 during the handshake sequence. To avoid losing data, the software must not overwrite the port until the corresponding interrupt request indicates that the external device has latched the data.

The software can always read Port 3 output and input handshake lines, but cannot write to the output handshake line.

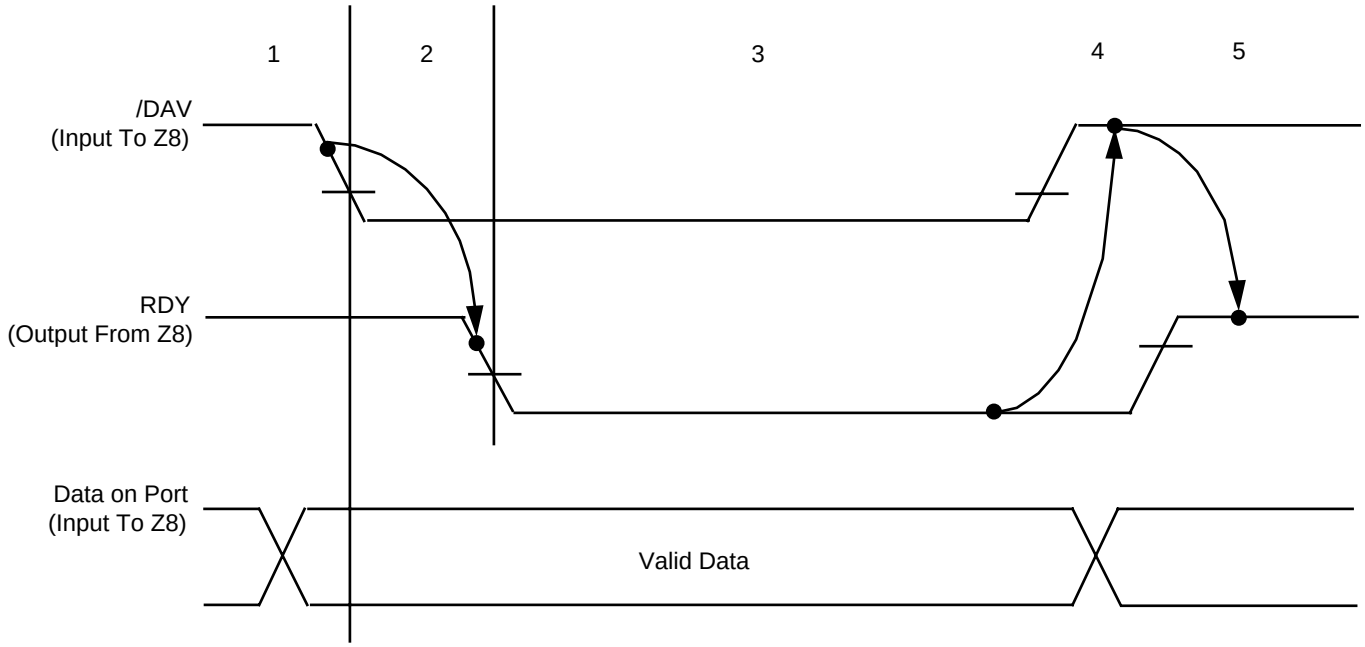
The following is the recommended setup sequence when configuring a Port for handshake operation for the first time after a reset:

- Load P01M or P2M to configure the port for input/output.
- Load P3 to set the Output Handshake bit to a logic 1.
- Load P3M to select the Handshake Mode for the port.

Once a data transfer begins, the configuration of the handshake lines should not be changed until the handshake is completed.

Figures 5-23 and 5-24 show detailed operation for the handshake sequence.

5.6 PORT HANDSHAKE (Continued)



State 1. Port 3 output is High, indicating that the I/O device is ready to accept data.

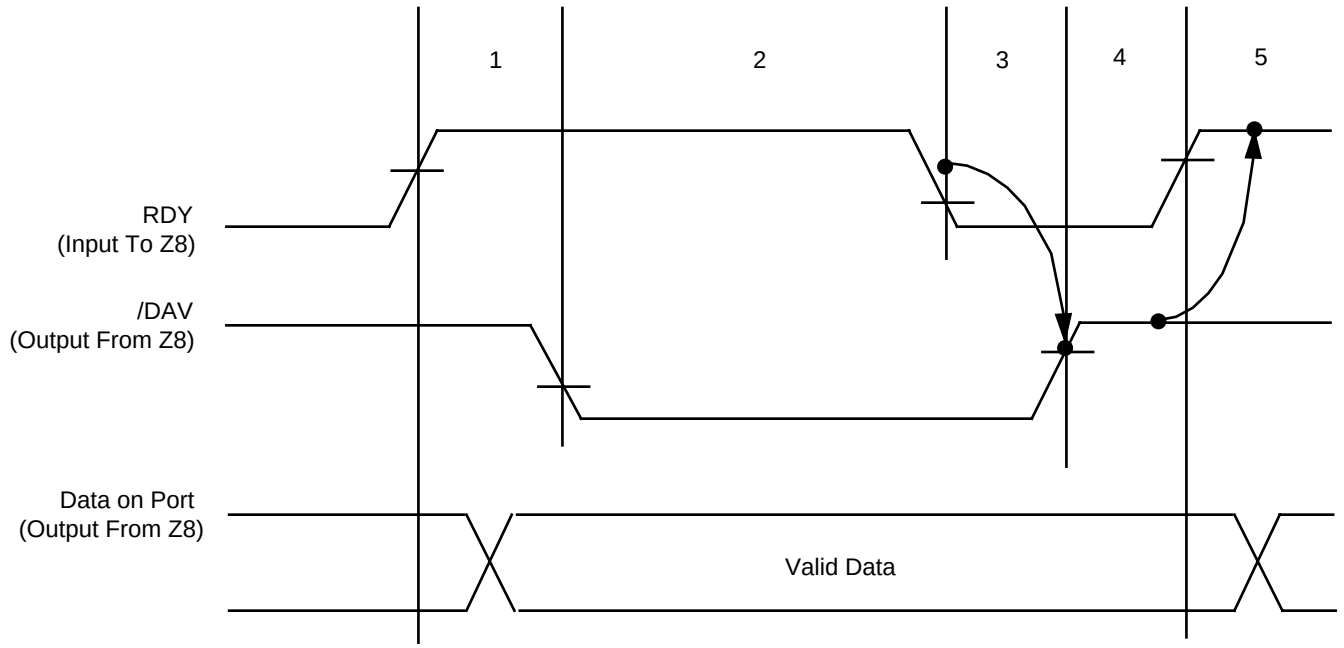
State 2. The I/O device puts data on the port and then activates the /DAV input. This causes the data to be latched into the port input register and generates an interrupt request.

State 3. The Z8 forces the Ready (RDY) output Low, signaling to the I/O device that the data has been latched.

State 4. The I/O device returns the /DAV line High in response to RDY going Low.

State 5. The Z8 RR software must respond to the interrupt request and read the contents of the port in order for the handshake sequence to be completed. The RDY line goes High if and only if the port has been read and /DAV is High. This returns the interface to its initial state.

Figure 5-23. Z8 Input Handshake



State 1. RDY input is High indicating that the I/O device is ready to accept data.

State 2. The Z8 Writes to the port register to initiate a data transfer. Writing to the port outputs new data and forces /DAV Low if and only if RDY is High.

State 3. The I/O device forces RDY Low after latching the data. RDY Low causes an interrupt request to be generated. The Z8 can write new data responses to RDY going Low; however, the data is not output until State 5.

State 4. The /DAV output from the Z8 is driven High in response to RDY going Low.

State 5. The /DAV goes High, the I/O device is free to raise RDY High thus returning the interface to its initial state.

Figure 5-24. Z8 Output Handshake

5.6 PORT HANDSHAKE (Continued)

In applications requiring a strobed signal instead of the interlocked handshake, the Z8® MCU can satisfy this requirement as follows:

- In the Strobed Input mode, data can be latched in the Port input register using the /DAV input. The data transfer rate must allow enough time for the software to read the Port before strobing in the next character. The RDY output is ignored.
- In the Strobed Output Mode, the RDY input should be tied to the /DAV output.

Figures 5-25 and 5-26 illustrate the strobed handshake connections.

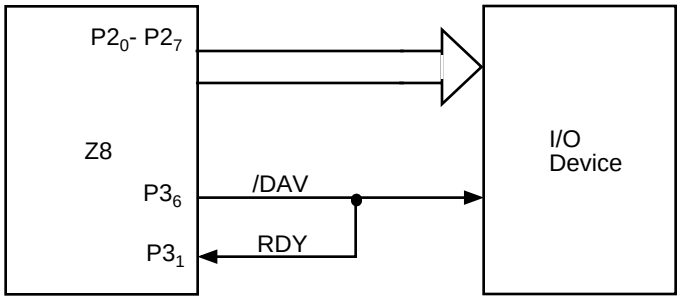


Figure 5-25. Output Strobed Handshake on Port 2

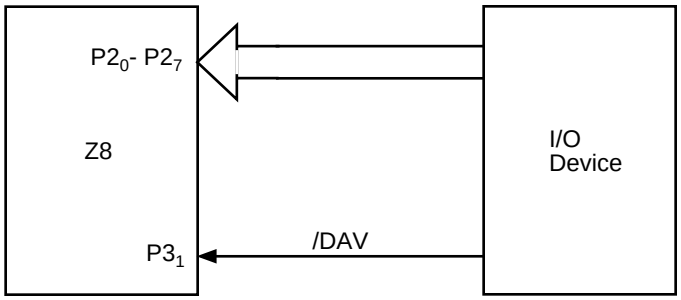


Figure 5-26. Input Strobed Handshake on Port 2

5.7 I/O PORT RESET CONDITIONS

5.7.1 Full Reset

After a hardware reset, Watch-Dog Timer (WDT) reset, or a Power-On Reset (POR), Port Mode Registers P01M, P2M, and P3M are set as shown in Figures 5-27 through 5-22. Port 2 is configured for input operation on all bits and is set for open-drain (Figure 5-29). If push-pull outputs are desired for Port 2 outputs, remember to configure them using P3M. Please note that a WDT time-out from Stop-Mode Recovery does not do a full reset. Certain registers that are not reset after Stop-Mode Recovery will not be reset.

For the condition of the Ports after Stop-Mode Recovery, please refer to specific device product specifications. In some cases, the Z8® has the P01M, P2M, and P3M control register set back to the default condition after reset while others do not.

All special I/O functions of Port 3 are inactive, with P33–P30 set as inputs and P37–P34 set as outputs (Figure 5-29).

Note: Because the types and amounts of I/O vary greatly among the Z8 family devices, the user is advised to review the selected device's product specifications for the register default state after reset.

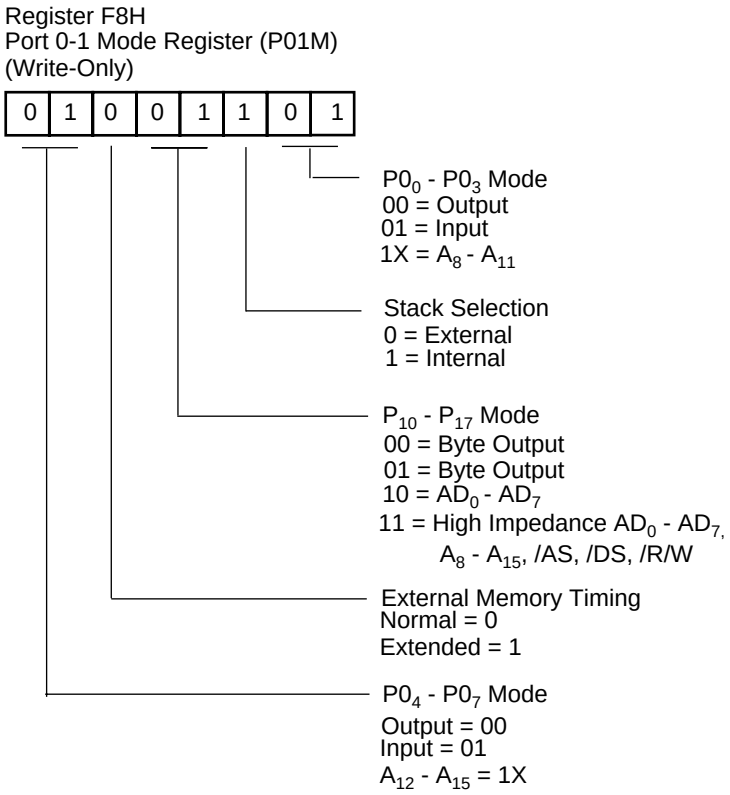


Figure 5-27. Port 0/1 Reset

5.7 I/O PORT RESET CONDITIONS (Continued)

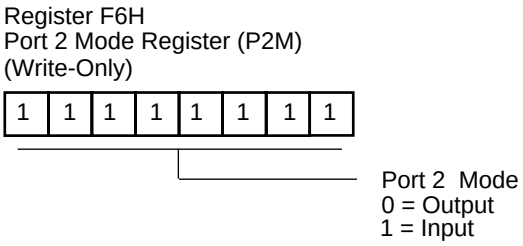


Figure 5-28. Port 2 Reset

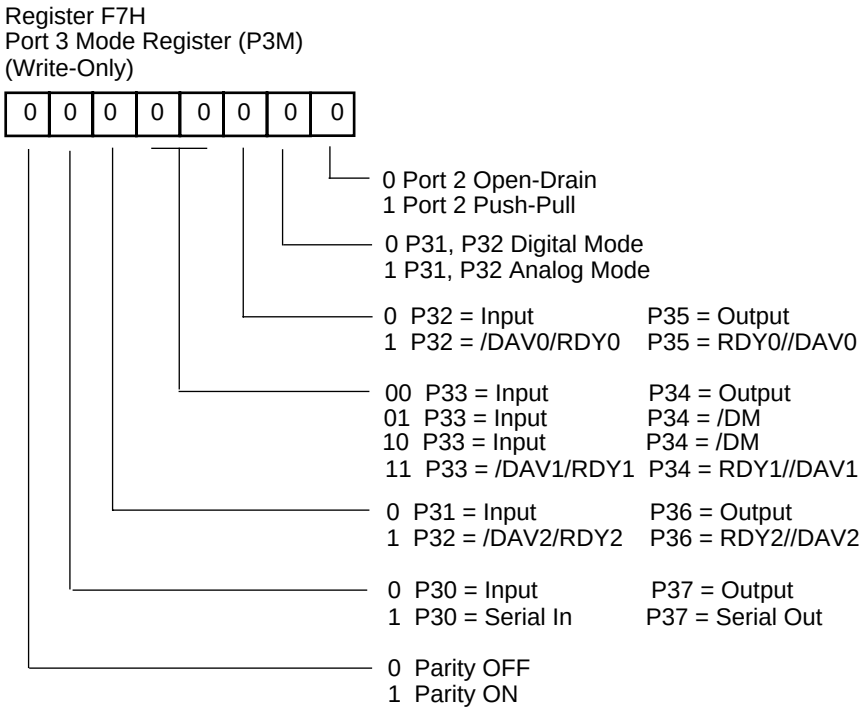


Figure 5-29. Port 3 Mode Reset

5.8 ANALOG COMPARATORS

Select Z8® devices include two independent on-chip analog comparators. See the device product specification for feature availability and use. Port 3, Pins P31 and P32 each have a comparator front end. The comparator reference voltage, pin P33, is common to both comparators. In Analog Mode, the P31 and P32 are the positive inputs to the comparators and P33 is the reference voltage supplied to both comparators. In Digital Mode, pin P33 can be used as a P33 register input or IRQ1 source. P34, P35, or P37 may output the comparator outputs by software-programming the PCON Register bit D0 to 1.

5.8.1 Comparator Description

Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming the Port 3 Mode Register (P3M bit 1). For interrupt functions during analog mode, P31 and P32 can be programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and bit 7).

Note: P33 cannot generate an external interrupt while in this mode. P33 can only generate interrupts in the Digital Mode.

Note: Port 3 inputs must be in digital mode if Port 3 is a Stop-Mode Recovery source. The analog comparator is disabled in STOP mode.

P31 can be used as T_{IN} in Analog or Digital Modes, but it must be referenced to P33, when in Analog Mode.

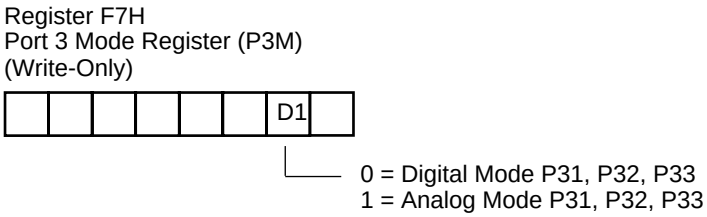


Figure 5-30. Port 3 Input Analog Selection

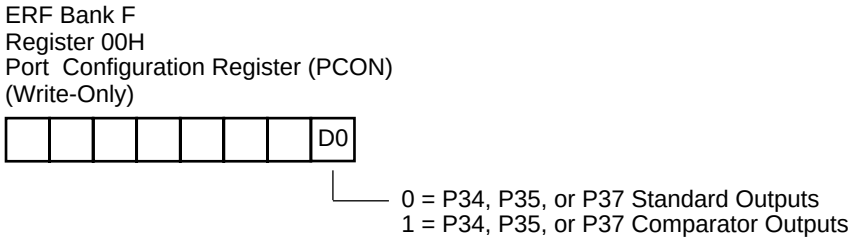


Figure 5-31. Port 3 Comparator Output Selection

5.8 ANALOG COMPARATORS (Continued)

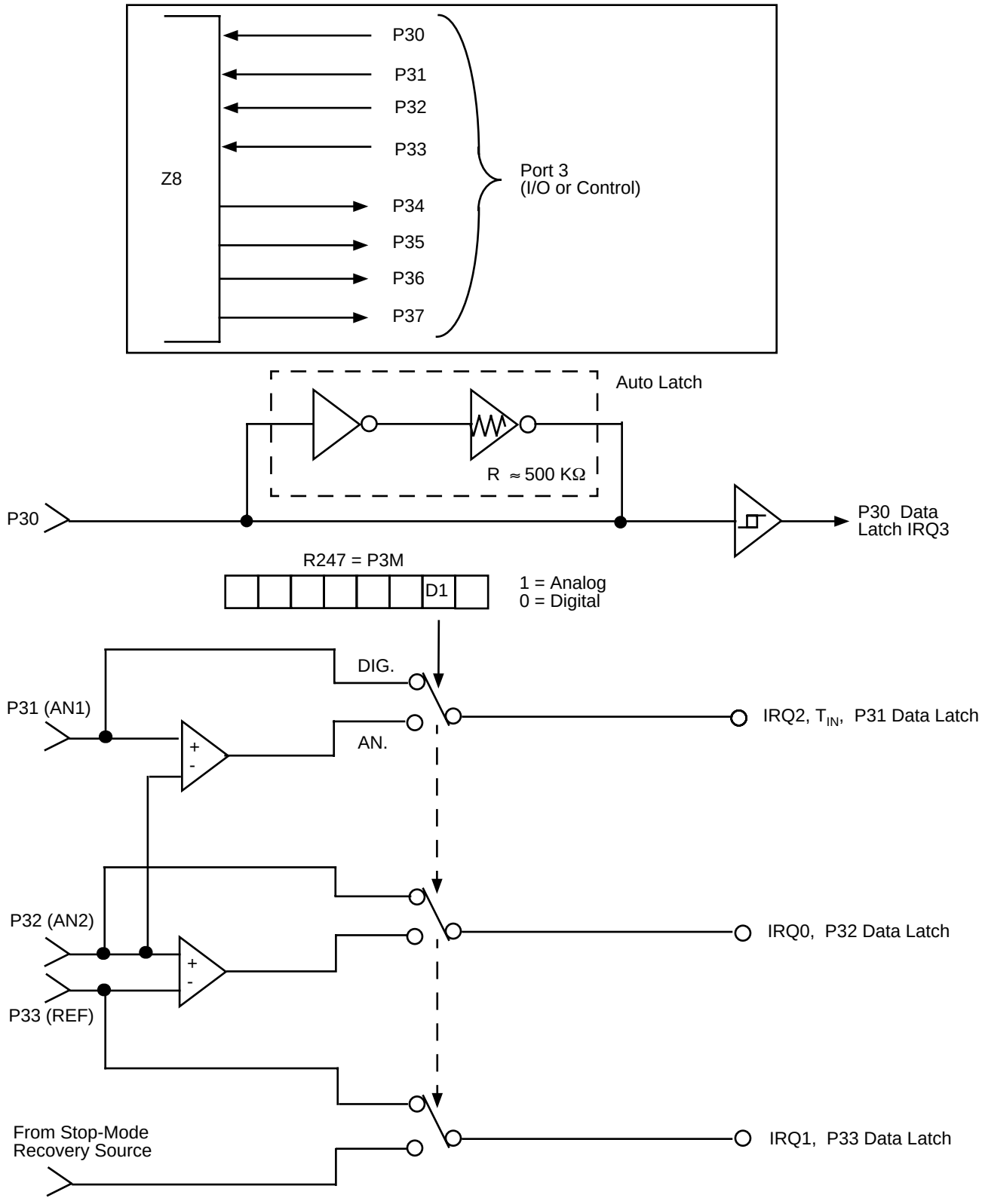


Figure 5-32. Port Configuration of Comparator Inputs on P31, P32, and P33

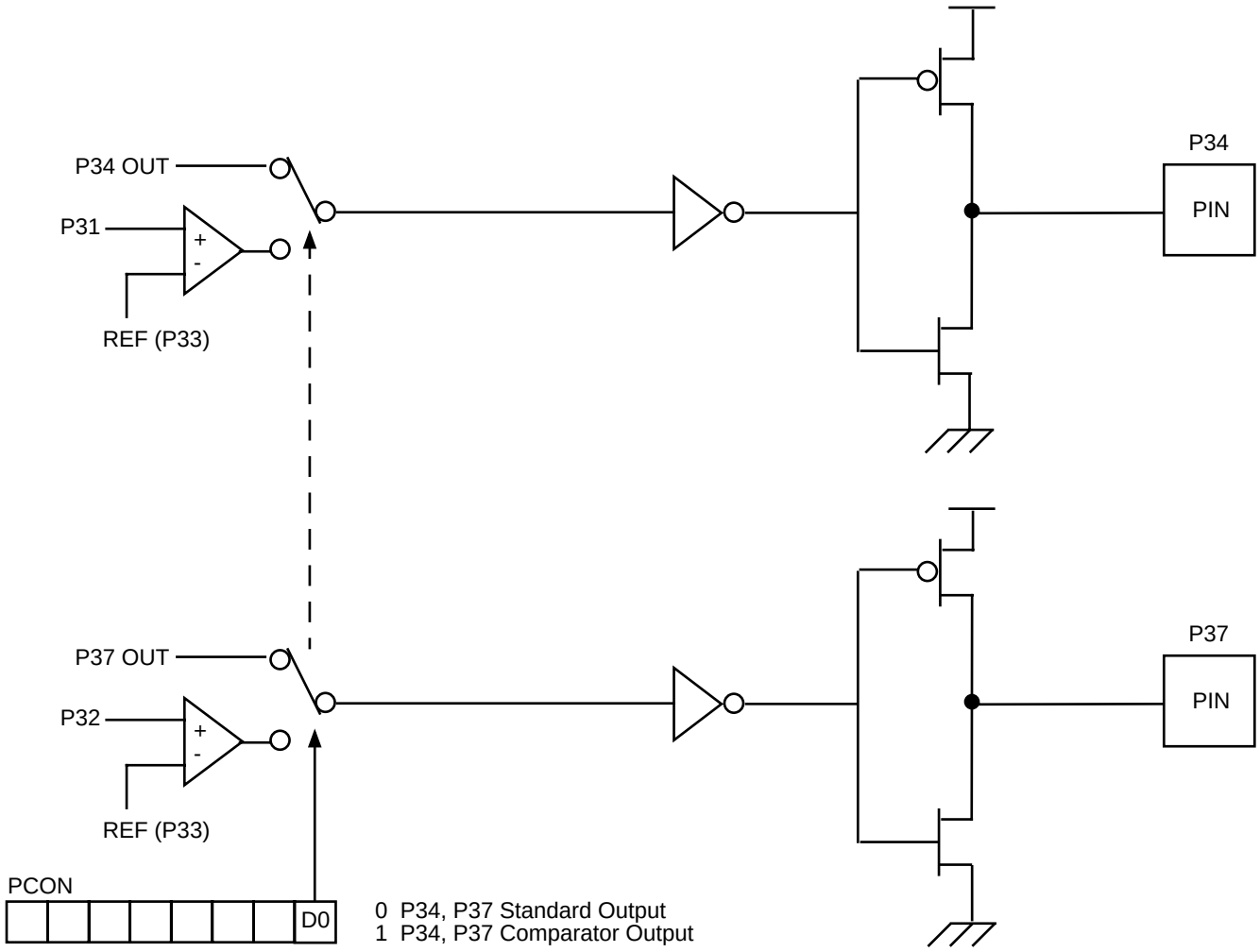


Figure 5-33. Port 3 Configuration

5.8.2 Comparator Programming

Example of enabling analog comparator mode.

```
LD P3M, #XXXX XX1XB
```

Note: X = don't care.

Example of enabling analog comparator output.

```
LD RP, #%0FH        ;Sets register pointer to
                    ;working register group 0
                    ;and Expanded Register
                    ;File Bank F.
LD R0, #XXXX XXX1B  ;Enables comparator
                    ;outputs using PCON

                    ;Register programming.
```

5.8.3 COMPARATOR OPERATION

After enabling the Analog Comparator mode, P33 becomes a common reference input for both comparators. The P33 (Ref) is hard wired to the reference inputs to both comparators and cannot be separated. P31 and P32 are always connected to the positive inputs to the comparators. P31 is the positive input to comparator AN1 while P32 is the positive input to comparator AN2. The outputs to comparators AN1 and AN2 are AN1-out and AN2-out, respectively.

The comparator output reflects the relationship between the positive input to the reference input.

Example: If the voltage on AN1 is higher than the voltage on Ref then AN1-out will be at a high state. If voltage on AN2 is lower than the voltage on Ref then AN2-out will be at a Low state. In this example, when the Port 3 register is read, Bits D1 = 1 and D2 = 0. If the comparator outputs are enabled to come out on P34 and P37, then P34 = 1 and P37 = 0. Please note that the previous data stored in P34 and P37 is not disturbed. Once the comparator outputs are de-selected the stored values in the P34 and P37 register bits will be reflected on these pins again.

5.8.4 Interrupts

In the example from Section 5.8.3, P32 (AN2) will generate an interrupt based on the result of the comparison being low and the Interrupt Request Register (IRQ FAH) having bits D7=0 and D6=0. If IRQ D7=1 and D6=0 then both P31 and P32 would generate interrupts.

5.8.5 Comparator Definitions

5.8.5.1 V_{ICR}

The usable voltage range for both positive inputs and the reference input is called the common mode voltage range (V_{ICR}). The comparator is not guaranteed to work if the inputs are outside of the V_{ICR} range.

5.8.5.2 V_{offset}

The absolute value of the voltage between the positive input and the reference input required to make the comparator output voltage switch is the input offset voltage (V_{offset}). If AN1 is 3.000V and Ref is 3.001V when the comparator output switches states then the Voffset = 1mV.

5.8.5.3 I_{IO}

For CMOS voltage comparator inputs, the input offset current (I_{IO}) is the leakage current of the CMOS input gate.

5.8.6 RUN Mode

P33 is not available as an interrupt input during Analog Mode. P31 and P32 are valid interrupt inputs in conjunction with P33 (Ref) when in the Analog Mode.

P31 can still be used as T_{IN} when the analog mode is selected. If comparator outputs are desired to be outputted on the Port 3 outputs, please refer to specific products specification for priority of mixing when other special features are sharing those same Port 3 pins.

5.8.7 HALT Mode

The analog comparators are functional during HALT Mode if the Analog Mode has been enabled. P31 and P32, in conjunction with P33 (Ref) will be able to generate interrupts. Only P33 cannot generate an interrupt since the P33 input goes directly to the Ref input of the comparators and is disconnected from the interrupt sensing circuits.

5.8.8 STOP Mode

The analog comparators are disabled during STOP Mode so it does not use any current at that time. If P31, P32, or P33 are used as a source for Stop-Mode Recovery, the Port 3 Digital Mode must be selected by setting bit D1=0 in the Port 3 Mode Register. Otherwise in STOP Mode, the P31, P32, and P33 cannot be sensed. If the Analog Mode was selected when entering STOP Mode, it will still be enabled after a valid SMR triggered reset.

5.9 OPEN-DRAIN CONFIGURATION

All Z8s can configure Port 2 to provide open-drain outputs by programming the Port 3 Mode Register (P3M) bit D0=0.

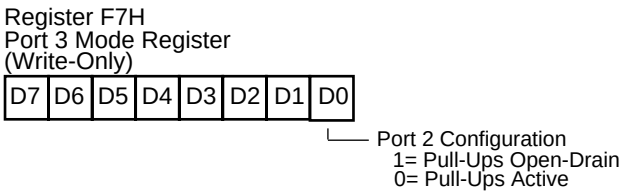


Figure 5-34. Port 2 Configuration

Other Z8s that have a Port Configuration Register (PCON) that can configure Port 0 and Port 1 to provide open-drain outputs. The PCON Register is located in Expanded Register File (ERF) Bank F, Register 00H. See Figure 5-35.

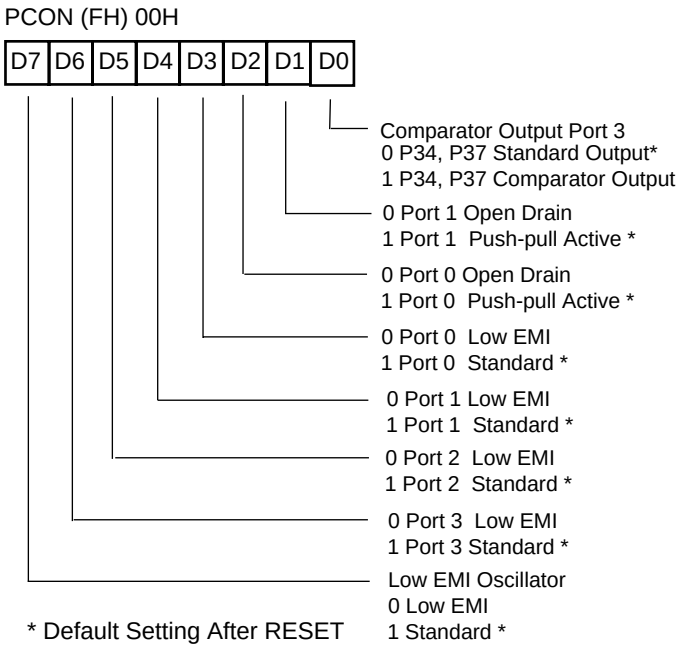


Figure 5-35. Port Configuration Register (PCON) (Write-Only)

Port 1 Open-Drain (D1). Port 1 can be configured as open-drain by resetting this bit (D1=0) or configured as push-pull active by setting this bit (D1=1). The default value is 1.

Port 0 Open Drain (D2). Port 0 can be configured as open-drain by resetting this bit (D2=0) or configured as push-pull active by setting this bit (D2=1). The default value is 1.

5.10 LOW EMI EMISSION

Some Z8s can be programmed to operate in a Low EMI Emission Mode using the Port configuration register (PCON). The PCON register allows the oscillator and all I/O ports to be programmed in the Low-EMI Mode independently. Other Z8s may offer a ROM Mask or OTP programming option to configure the Z8 Ports and oscillator globally to a Low-EMI mode (where the XTAL frequency is set equal to the internal system clock frequency.

Use of the Low EMI feature results in:

- The output pre-drivers slew rate reduced to 10 ns (typical).
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Low EMI Oscillator.
- All output drivers are approximately 25 percent of the standard drive.
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time, when Low EMI Oscillator is selected and system clock (SCLK=XTAL, SMR Reg. Bit D1=1).

For Z8s having the PCON register feature, the following bits control the Low EMI options:

- **Low EMI Port 0 (D3).** Port 0 can be configured as a Low EMI Port by resetting this bit (D3=0) or configured as a Standard Port by setting this bit (D3=1). The default value is 1.
- **Low EMI Port 1 (D4)**. Port 1 can be configured as a Low EMI Port by resetting this bit (D4=0) or configured as a Standard Port by setting this bit (D4=1). The default value is 1.
- **Low EMI Port 2 (D5).** Port 2 can be configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting this bit (D5=1). The default value is 1.
- **Low EMI Port 3 (D6).** Port 3 can be configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting this bit (D6=1). The default value is 1.
- **Low EMI OSC (D7).** This bit of the PCON Register controls the Low EMI oscillator. A 1 in this location configures the oscillator with standard drive, while a 0 configures the oscillator with low noise drive. The Low-EMI mode will reduce the drive of the oscillator (OSC). The default value is 1. XTAL/2 mode is not effected by this bit.

Note: The maximum external clock frequency is 4 MHz when running in the Low EMI oscillator mode.

Please refer to the selected device product specification for availability of the Low EMI feature and programming options.

5.11 INPUT PROTECTION

All CMOS ROM Z8s have I/O pins with diode input protection. There is a diode from the I/O pad to V_{CC} and to V_{SS}. See Figure 5-36.

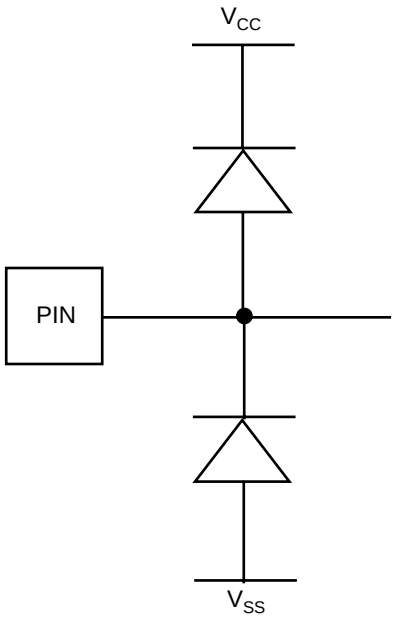


Figure 5-36. Diode Input Protection

On CMOS OTP EPROM Z8's, the Port 3 inputs P31, P32, P33 and the XTAL 1 pin have only the input protection diode from pad to V_{SS}. See Figure 5-37.

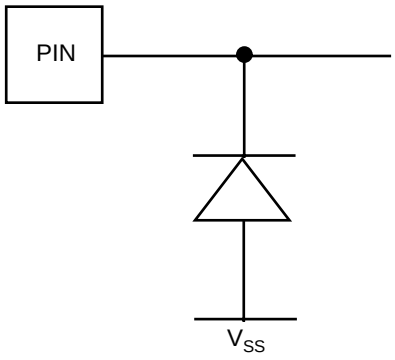


Figure 5-37. OTP Diode Input Protection

The high-side input protection diodes were removed on these pins to allow the application of +12.5V during the various OTP programming modes.

For better noise immunity in applications that are exposed to system EMI, a clamping diode to V_{CC} from these pins may be required to prevent entering the OTP programming mode or to prevent high voltage from damaging these pins.

5.12 CMOS Z8 AUTO LATCHES

I/O port bits that are configurable as inputs are protected against open circuit conditions using Auto Latches. An Auto Latch is a circuit which, in the event of an open circuit condition, latches the input at a valid CMOS level. This inhibits the tendency of the input transistors to self-bias in the forward active region, thus drawing excessive supply current. A simplified schematic of the CMOS Z8 I/O circuit is shown in Figure 5-38.

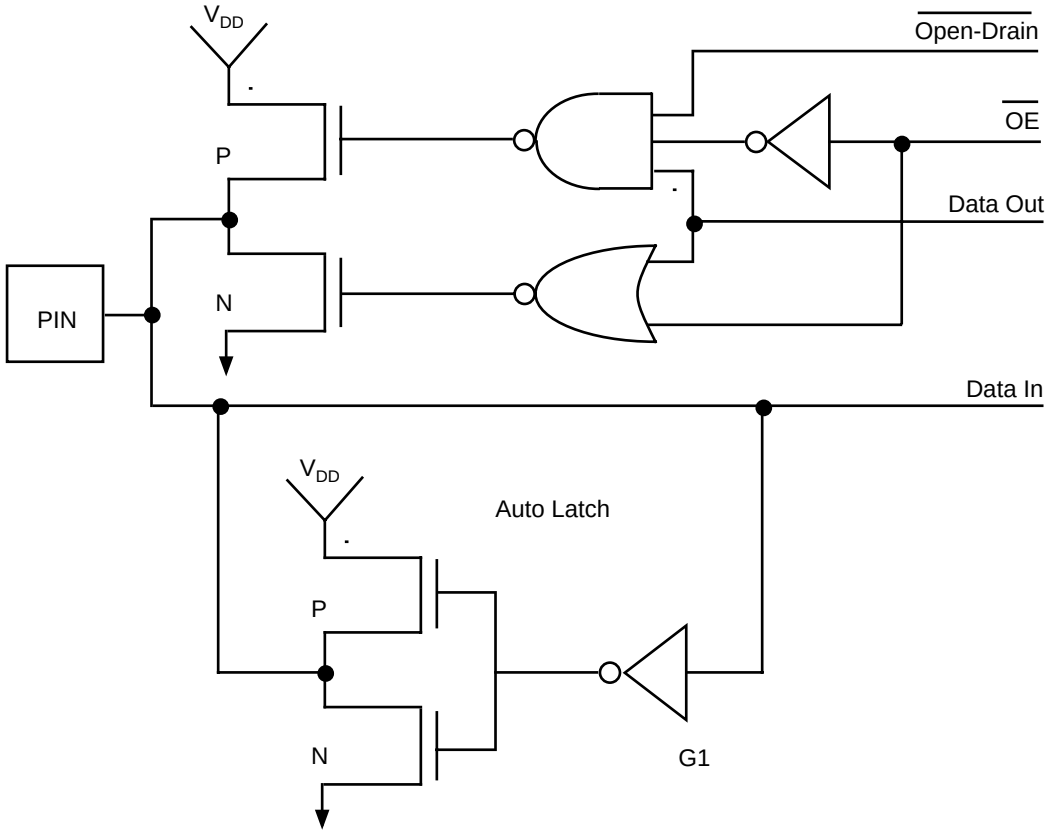


Figure 5-38. Simplified CMOS Z8 I/O Circuit

The operation of the Auto Latch circuit is straight-forward. Assume the input pad is latched at +5V (logic 1). The inverter G1 inverts the bit, turning the P-channel FET ON and the N-channel FET OFF. The output of the circuit is effectively shorted to V_{DD}, returning +5V to the input. If the pad is then disconnected from the +5V source, the Auto Latch will hold the input at the previous state. If the device is powered up with the input floating, the state of the Auto Latch will be at either supply, but which state is unpredictable.

There are four operating conditions which will activate the Auto Latches. The first, which occurs when the input pin is physically disconnected from any source, is the most obvious. The second occurs when the input is connected to the output of a device with tri-state capability.

The Auto Latch will also activate when the input voltage at the pin is not within 200 microvolts or so of either supply rail. In this case, the circuit will draw current, which is not significant compared to the Icc operating current of the device, but will increase I_{CC2} STOP Mode current of the device dramatically.

The fourth condition occurs when the I/O bit is configured as an output. Referring to the output section of Figure 5-38, there are two ways of tri-stating the port pin. The first is by configuring the port as an input, which disables the /OE signal turning both transistors off. The second can be achieved in output mode by writing a “1” to the output port, then activating the open drain mode. Both transistors are again off, and the port bit is in a high impedance state. The Auto Latches then pull the input section toward V_{DD}.

Auto Latch Model:

The Auto Latch's equivalent circuit is shown in Figure 5-39. When the input is high, the circuit consists of a resistance Rp from V_{DD} (the P-channel transistor in its ON state) and a much greater resistance Rh to G_{ND}. Current Iao flows from V_{DD} to the output. When the input is low, the circuit may be modeled as a resistance Rp from G_{ND} (the N-channel transistor in the ON state) and a much greater resistance Rh to V_{DD}. Current Iao now flows from the input to ground. The Auto Latch is characterized with respect to Iao, so the equivalent resistance Rp is calculated according to R_P= (V_{DD}-VIN)/Iao. The worst case equivalent resistance Rp (min) may be calculated at the worst case input voltage, V_i= V_{ih}(min).

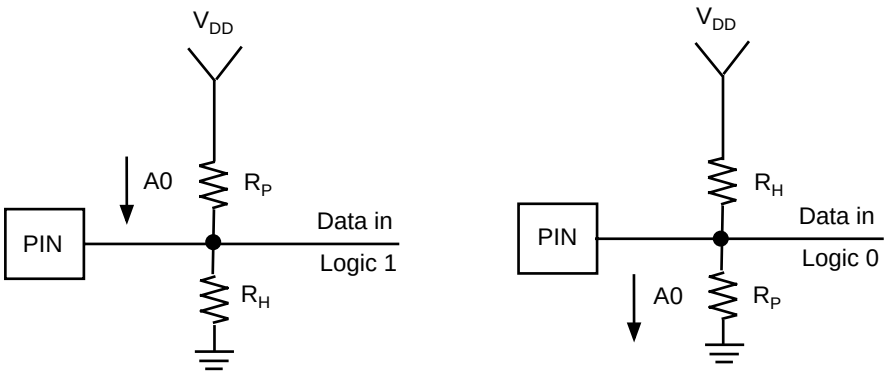


Figure 5-39. Auto Latch Equivalent Circuit

Design Considerations:

For circuits in which the Auto Latch is active, consideration should be given to the loading constraints of the Auto Latches. For example, with weak values of V_{IN}, close to Vih (min) or Vil (max), pullup or pull-down resistances must be calculated using Ref = R/Rp. For best case STOP mode operation, the inputs should be within 200 mV of the supply rails.

In output mode, if a port bit is forced into a tri-state condition, the Auto Latches will force the pad to V_{DD}. If there is an external pulldown resistor on the pin, the voltage at the pin may not switch to GND due to the Auto Latch. As shown in Figure 5-40, the equivalent resistance of the Auto Latch and the external pulldown form a voltage divider, and if the external resistor is large, the voltage developed across it will exceed Vil(max). For worst case:

Vil(max > V_{DD} [Rext/(Rext+Rp)]
Rext(max) = [(Vil(max)/V_{DD})Rp]/[1-(Vil(max)/V_{DD})]

For V_{DD} = 5.0V and Iao = 5 uA we have Vih(max) =0.8V:
Rext(max) = (0.16/1M)/(1–0.16) = 190 K ohms.

Rp increases rapidly with V_{DD}, so increased V_{DD} will relax the requirement on Rext.

In summary, the C_{MOS} Z8 Auto Latch inhibits excessive current drain in Z8 devices by latching an open input to either V_{DD} or GND. The effect of the Auto Latch on the I/O characteristics of the device may be modeled by a current Iao and a resistor Rp, whose value is V_{DD}/Iao.

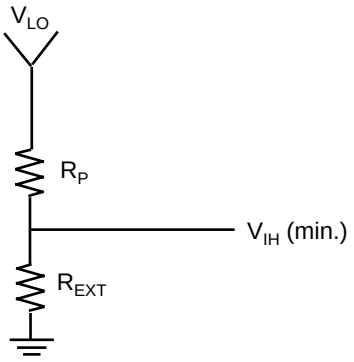


Figure 5-40. Effect of Pulldown Resistors on Auto Latches