CHAPTER 4
RESET—WATCH-DOG TIMER

4.1 RESET

This section describes the Z8® reset conditions, reset timing, and register initialization procedures. Reset is generated by Power-On Reset (POR), Reset Pin, Watch-Dog Timer (WDT), and Stop-Mode Recovery.

A system reset overrides all other operating conditions and puts the Z8 into a known state. To initialize the chip's internal logic, the /RESET input must be held Low for at least 21 SCP or 5 XTAL clock cycles. The control register and ports are reset to their default conditions after a POR, a reset from the /Reset pin, or Watch-Dog Timer timeout while in RUN mode and HALT mode. The control registers and ports are not reset to their default conditions after Stop-Mode Recovery and WDT timeout while in STOP mode.

While /RESET pin is Low, /AS is output at the internal clock rate, /DS is forced Low, and R//W remains High. The program counter is loaded with 000CH. I/O ports and control registers are configured to their default reset state.

Resetting the Z8 does not effect the contents of the general-purpose registers.

4.2 RESET PIN, INTERNAL POR OPERATION

In some cases, the Z8 hardware /RESET pin initializes the control and peripheral registers, as shown in Tables 4-1, 4-2, 4-3, and 4-4. Specific reset values are shown by 1 or 0, while bits whose states are unknown are indicated by the letter U. The Tables 4-1, 4-2, 4-3, and 4-4 show the reset conditions for the generic Z8.

Note: The register file reset state is device dependent. Please refer to the selected device product specifications for register availability and reset state.

4.2 RESET PIN, INTERNAL POR OPERATION (Continued)

Table 4-1. Sample Control and Peripheral Register Reset Values (ERF Bank 0)

Register (HEX)	Register Name	Bits 7	6	5	4	3	2	1	0	Comments
F0	Serial I/O	U	U	U	U	U	U	U	U	
F1	Timer Mode	0	0	0	0	0	0	0	0	Counter/Timers Stopped
F2	Counter/Timer1	U	U	U	U	U	U	U	U	
F3	T1 Prescaler	U	U	U	U	U	U	0	0	Single-Pass Count Mode, External Clock Source
F4	Counter/Timer0	U	U	U	U	U	U	U	U	
F5	T0 Prescaler	U	U	U	U	U	U	U	0	Single-Pass Count Mode
F6	Port 2 Mode	1	1	1	1	1	1	1	1	All Inputs
F7	Port 3 Mode	0	0	0	0	0	0	0	0	Port 2 Open-Drain, P33–P30 Input, P37–P34 Output
F8	Port 0–1 Mode	0	1	0	0	1	1	0	1	Internal Stack, Normal Memory Timing
F9	Interrupt Priority	U	U	U	U	U	U	U	U	
FA	Interrupt Request	0	0	0	0	0	0	0	0	All Interrupts Cleared
FB	Interrupt Mask	0	U	U	U	U	U	U	U	Interrupts Disabled
FC	Flags	U	U	U	U	U	U	U	U	
FD	Register Pointer	0	0	0	0	0	0	0	0	
FE	Stack Pointer (High)	U	U	U	U	U	U	U	U	
FF	Stack Pointer (Low)	U	U	U	U	U	U	U	U	

Program execution starts 5 to 10 clock cycles after /INTERNAL RESET has returned High. The initial instruction fetch is from location 000CH. Figure 4-1 shows reset timing.

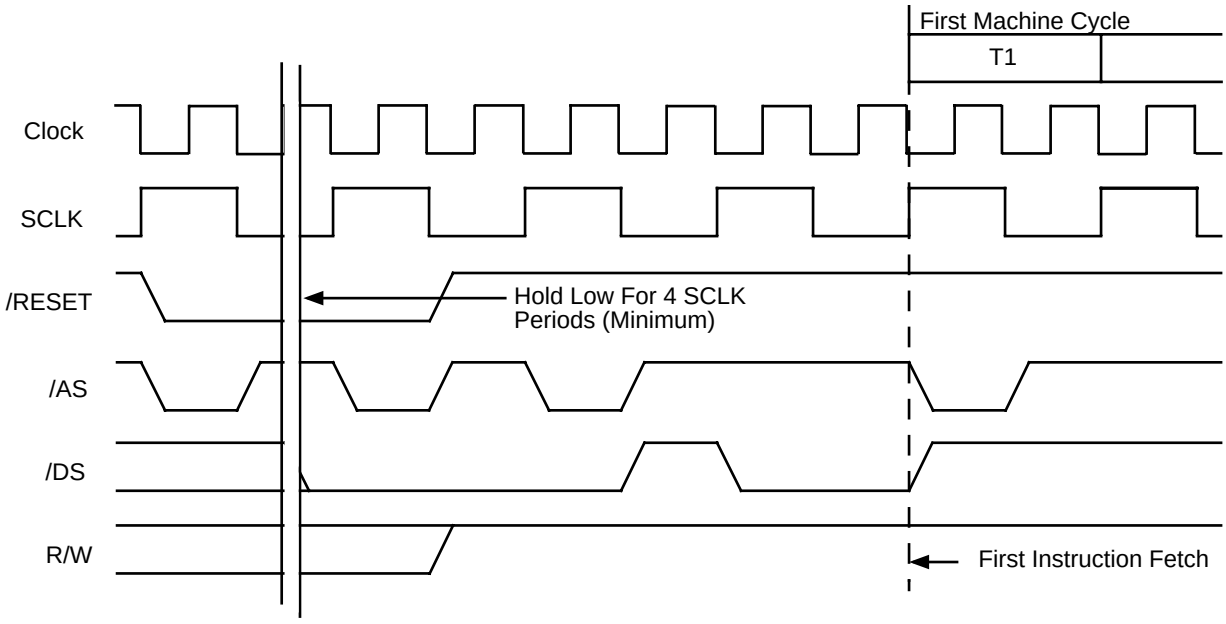

Figure 4-1. Reset Timing

After a reset, the first routine executed should be one that initializes the control registers to the required system configuration.

The /RESET pin is the input of a Schmitt-triggered circuit. Resetting the Z8® will initialize port and control registers to their default states. To form the internal reset line, the output of the trigger is synchronized with the internal clock. The clock must therefore be running for /RESET to function. It requires 4 internal system clocks after reset is detected for the Z8 to reset the internal circuitry. An internal pull-up, combined with an external capacitor of 1 uf, provides enough time to properly reset the Z8 (Figure 4-2). In some cases, the Z8 has an internal POR timer circuit that holds the Z8 in reset mode for a duration (T_{POR}) before releasing the device out of reset. On these Z8 devices, the internally generated reset drives the reset pin low for the POR time. Any devices driving the reset line must be open-drained in order to avoid damage from possible conflict during reset conditions. This reset time allows the on-board clock oscillator to stabilize.

To avoid asynchronous and noisy reset problems, the Z8 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. During the reset cycle, /DS is held active low while /AS cycles at a rate of the internal system clock. Program execution begins at location 000CH, 5-10 TpC cycles after /RESET is released. For the internal Power-On Reset, the reset output time is specified as T_{POR}. Please refer to specific product specifications for actual values.

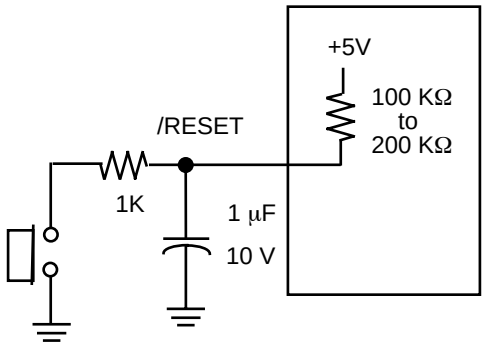

Figure 4-2. Example of External Power-On Reset Circuit

Table 4-2. Expanded Register File Bank 0 Reset Values at RESET

Register (HEX)	Register Name	Bits 7	6	5	4	3	2	1	0	Comments
00	Port 0	U	U	U	U	U	U	U	U	Input mode, output set to push-pull
01	Port 1	U	U	U	U	U	U	U	U	Input mode, output set to push-pull
02	Port 2	U	U	U	U	U	U	U	U	Input mode, output set to open drain
03	Port 3	1	1	1	1	U	U	U	U	Standard Digital input and output Z86L7X Family Device Port P34-P37 = 0 (Except Z86L70/71/75) All other Z8 = 1
04–EF	General-Purpose Registers 04-EF	U	U	U	U	U	U	U	U	Undefined

4.2 RESET PIN, INTERNAL POR OPERATION (Continued)

Table 4-3. Sample Expanded Register File Bank C Reset Values

Register (HEX)	Register Name	Bits 7	6	5	4	3	2	1	0	Comments
00	SPI Compare (SCOMP)	0	0	0	0	0	0	0	0	
01	Receive Buffer (RxBUF)	U	U	U	U	U	U	U	U	
02	SPI Control (SCON)	U	U	U	U	0	0	0	0	

Table 4-4. Sample Expanded Register File Bank F Reset Values

Register (HEX)	Register Name	Bits 7	6	5	4	3	2	1	0	Comments
00	Port Configuration (PCON)	1	1	1	1	1	1	1	0	Comparator outputs disabled on Port 3 Port 0 and 1 output is push-pull Port 0, 1, 2, 3, and oscillator with standard output drive
0B	STOP-Mode Recovery (SMR)	0	0	1	0	0	0	0	0	Clock divide by 16 off XTAL divide by 2 POR and / OR External Reset Stop delay on Stop recovery level is low, STOP flag is POR
0F	Watch-Dog Timer Mode (WDTMR)	U	U	U	0	1	1	0	1	512 TPC for WDT time out, WDT runs during STOP

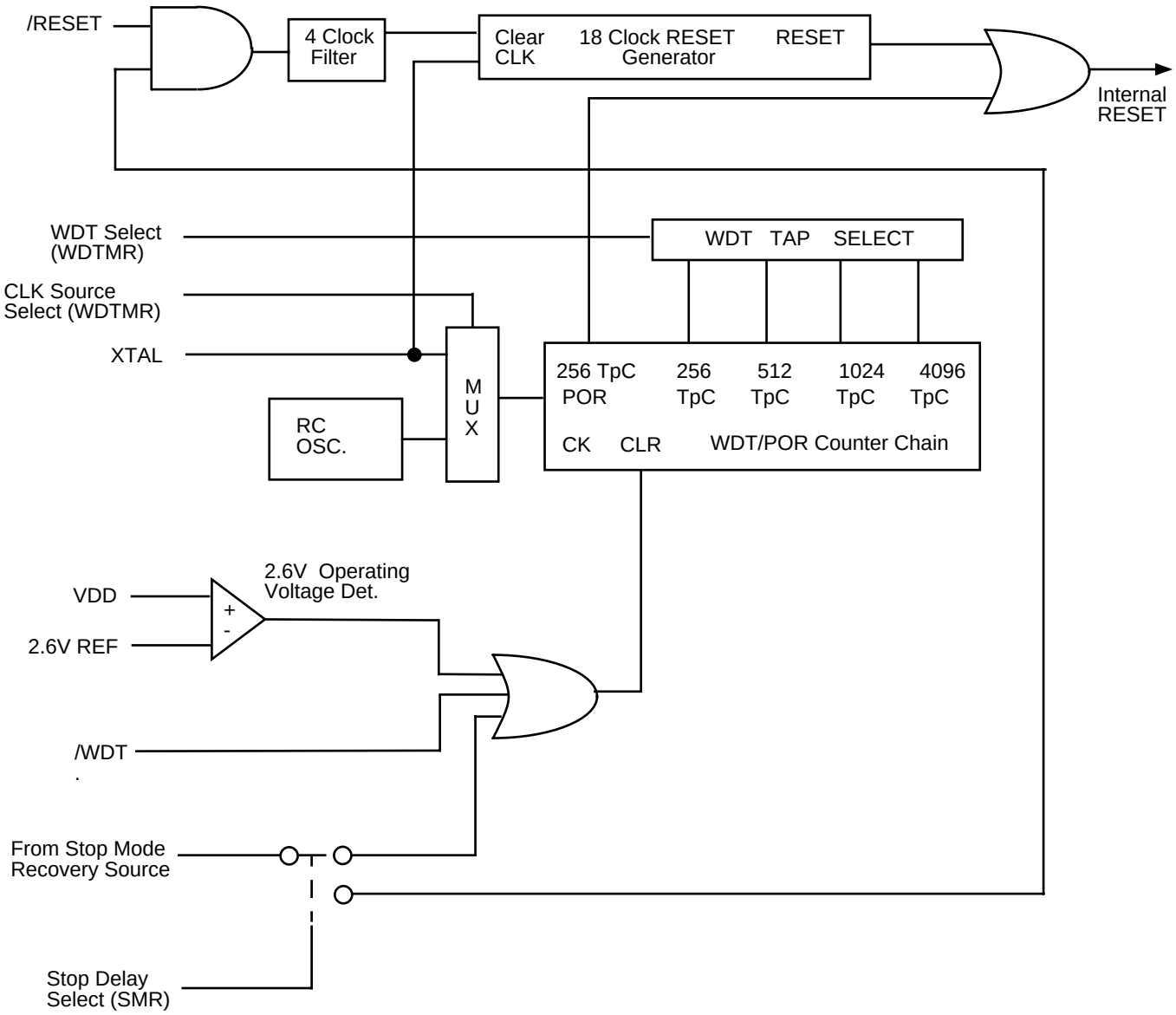

Figure 4-3. Example of Z8 Reset with /RESET Pin, WDT, SMR, and POR

4.2 RESET PIN, INTERNAL POR OPERATION (Continued)

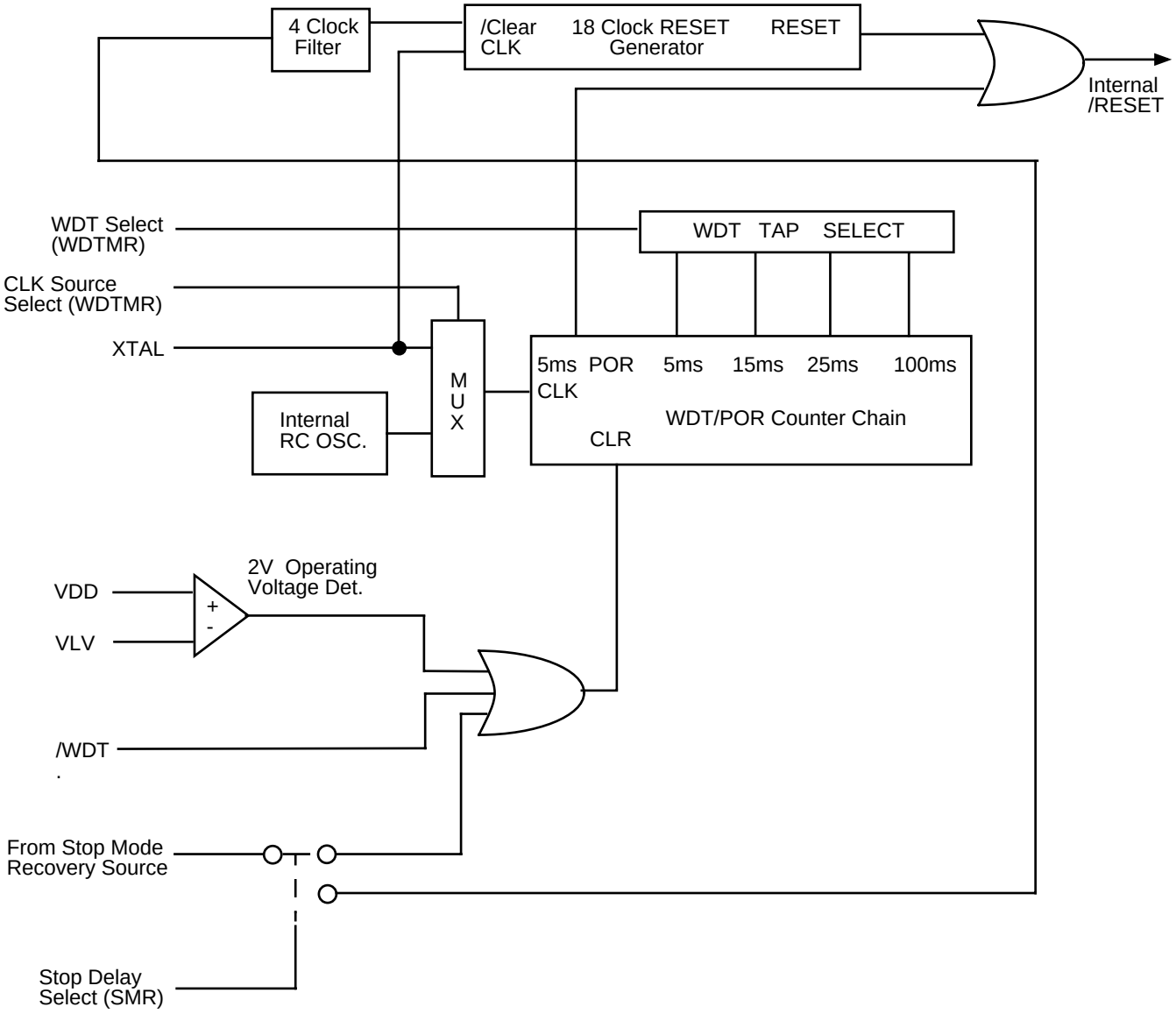

Figure 4-4. Example of Z8 Reset with WDT, SMR, and POR

4.3 WATCH-DOG TIMER (WDT)

The WDT is a retriggerable one-shot timer that resets the Z8® if it reaches its terminal count. When operating in the RUN or HALT modes, a WDT reset is functionally equivalent to a hardware /POR reset. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT cannot be disabled after it has been initially enabled. Permanently enabled WDTs are always enabled and the WDT instruction is used to refresh it. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the Watch-Dog Timer Mode register (WDTMR). In some cases, a Z8 that offers the WDT but does not have a WDTMR register, has a fixed WDT timeout and uses the on board RC oscillator as the only clock source. Please refer to specific product specifications for selectability of timeout, WDT during HALT and STOP modes, source of WDT clock, and availability of the permanently-on WDT option.

Note: Execution of the WDT instruction affects the Z (zero), S (sign), and V (overflow) flags.

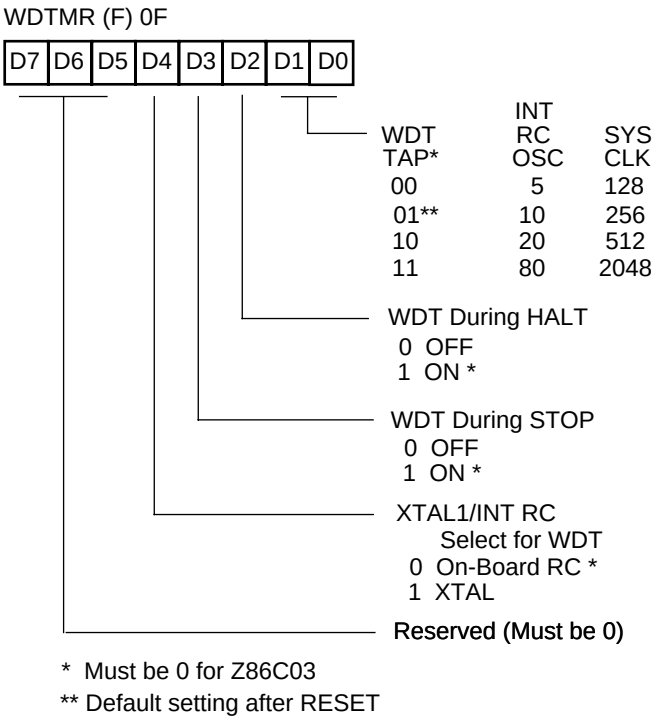

Figure 4-5. Example of Z8 Watch-Dog Timer Mode Register (Write-Only)

Note: The WDTMR register is accessible only during the first 60 processor cycles from the execution of the first instruction after Power-On Reset, Watch-Dog Reset or a Stop-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR is a write-only register.

The WDTMR is located in Expanded Register File Bank F, register 0FH. The control bits are described as follows:

WDT Time Select (D1, D0). Bits 0 and 1 control a tap circuit that determines the time-out period. Table 4-5 shows the different values that can be obtained. The default value of D1 and D0 are 0 and 1, respectively.

Table 4-5. Time-Out Period of the WDT

Time-Out of D1	D0	Typical Time-Out of Internal RC OSC	SYS Clock
0	0	5 ms min	256TpC
0	1	15 ms min	512TpC
1	0	25 ms min	1024TpC
1	1	100 ms min	4096TpC

Notes:
TpC = XTAL clock cycle
The default on reset is, D0 = 1 and D1 = 0.
The values given are for VCC = 5.0V.
See the device product specification for exact WDTMR time out select options available.

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1. A WDT time out during HALT mode will reset control register ports to their default reset conditions.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. Since XTAL clock is stopped during STOP Mode, unless as specified below, the on-board RC must be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1. If bits D3 and D4 are both set to 1, the WDT only, is driven by the external clock during STOP mode. This feature makes it possible to wake up from STOP mode from an internal source. Please refer to specific product specifications for conditions of control and port registers when the Z8 comes out of STOP mode. A WDT time out during STOP mode will not reset all control registers. The reset conditions of the ports from STOP mode due to WDT time out is the same as if recovered using any of the other STOP mode sources.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the internal RC oscillator.

Bits 5, 6 and 7. These bits are reserved.

V_{CC} Voltage Comparator. An on-board voltage comparator checks that V_{CC} is at the required level to insure correct operation of the device. Reset is globally driven if V_{CC} is below the specified voltage. This feature is available in select ROM Z8® devices. See the device product specification for feature availability and operating range.

4.4 POWER-ON-RESET (POR)

A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer (T_{POR}) function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status (cold start).
2. STOP-Mode Recovery (if bit 5 of SMR=1).
3. WDT timeout.

The POR time is specified as TPOR. On Z8 devices that feature a Stop-Mode Recovery register (SMR), bit 5 selects whether the POR timer is used after Stop-Mode Recovery or by-passed. If bit D5 = 1 then the POR timer is used. If bit 5 = 0 then the POR timer is by-passed. In this case, the Stop-Mode Recovery source must be held in the recovery state for 5 T_PC or 5 crystal clocks to pass the reset signal internally. This option is used when the clock is provided with an RC/LC clock. See the device product specification for timing details.

POR (cold start) will always reset the Z8 control and port registers to their default condition. If a Z8 has a SMR register, the warm start bit will be reset to a 0 to indicate POR.

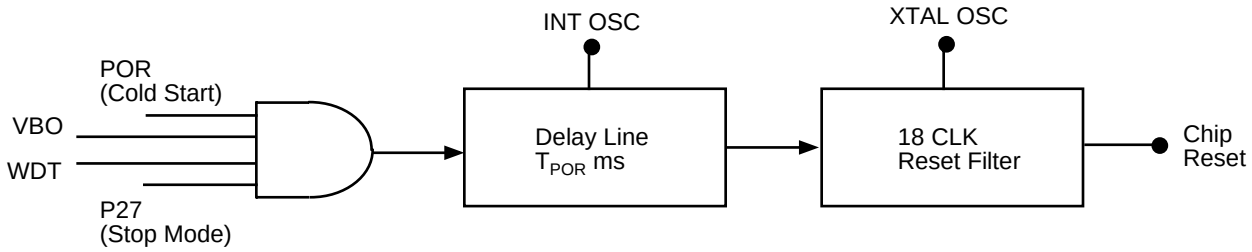

Figure 4-6. Example of Z8 with Simple SMR and POR