CHAPTER 3
CLOCK

3.1 CLOCK

The Z8® MCU derives its timing from on-board clock circuitry connected to pins XTAL1 and XTAL2. The clock circuitry consists of an oscillator, a divide-by-two shaping circuit, and a clock buffer. Figure 3-1 illustrates the clock circuitry. The oscillator's input is XTAL1 and its output is XTAL2. The clock can be driven by a crystal, a ceramic resonator, LC clock, RC, or an external clock source.

3.1.1 Frequency Control

In some cases, the Z8 has an EPROM/OTP option or a Mask ROM option bit to bypass the divide-by-two flip flop in Figure 3-1. This feature is used in conjunction with the low EMI option. When low EMI is selected, the device output drive and oscillator drive is reduced to approximately 25 percent of the standard drive and the divide-by-two flip flop is bypassed such that the XTAL clock frequency is equal to the internal system clock frequency. In this mode, the maximum frequency of the XTAL clock is 4 MHz. Please refer to specific product specification for availability of options and output drive characteristics.

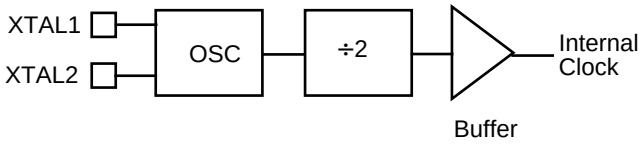

Figure 3-1. Z8 Clock Circuit

3.2 CLOCK CONTROL

In some cases, the Z8 offers software control of the internal system clock via programming register bits. The bits are located in the Stop-Mode Recovery Register in Expanded Register File Bank F, Register 0BH. This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 3-2). Please refer to the specific product specification for availability of this feature/register.

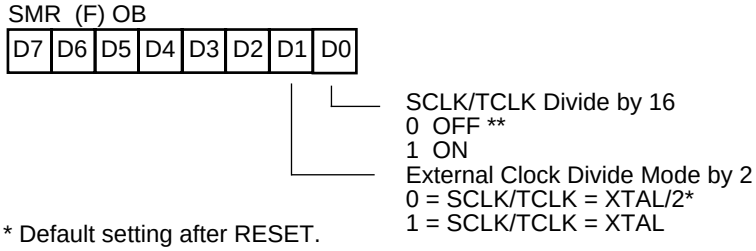

Figure 3-2. Stop-Mode Recovery Register (Write-Only Except D7, Which is Read-Only)

3.2.1 SCLK/TCLK Divide-By-16 Select (D0)

This bit of the SMR controls a divide-by-16 prescalar of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

3.2.2 External Clock Divide-By-Two (D1)

This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, SCLK (System Clock) and TCLK (Timer Clock) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1 = 1). Using this bit, together with D7 of PCON, further helps lower EMI (D7 (PCON) = 0, D1 (SMR) = 1). The default setting is 0. Maximum frequency is 4 MHz with D1=1 (Figure 3-3).

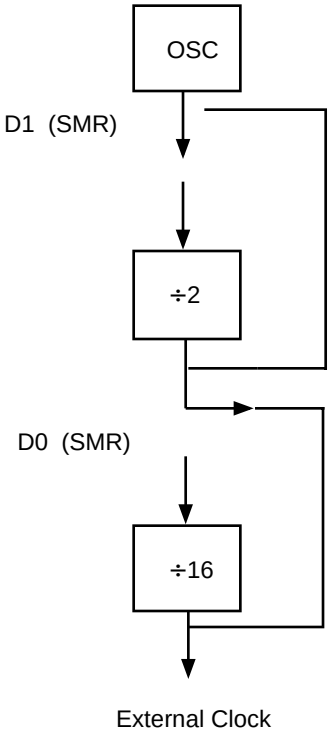

Figure 3-3. External Clock Circuit

3.3 OSCILLATOR CONTROL

In some cases, the Z8® MCU offers software control of the oscillator to select low EMI drive or standard drive. The selection is done by programming bit D7 of the Port Configuration (PCON) register (Figure 3-4). The PCON register is located in Expanded Register File Bank F, Register 00H.

A 1 in bit D7 configures the oscillator with standard drive, while a 0 configures the oscillator with Low EMI drive. This only affects the drive capability of the oscillator and does not affect the relationship of the XTAL clock frequency to the internal system clock (SCLK).

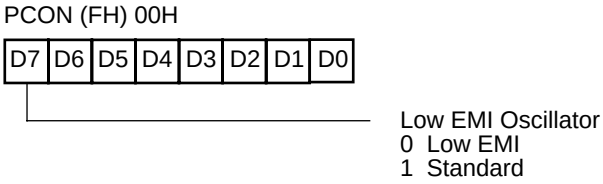

Figure 3-4. Port configuration register (PCON) (Write-Only)

3.4 OSCILLATOR OPERATION

The Z8® MCU uses a Pierce oscillator with an internal feedback (Figure 3-5). The advantages of this circuit are low cost, large output signal, low-power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects).

One draw back is the need for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements A x B = 1, where $A = V_0/V_i$ is the gain of the amplifier and $B = V_i/V_0$ is the gain of the feedback element. The total phase shift around the loop is forced to zero (360 degrees). Since VIN must be in phase with itself, the amplifier/inverter provides 180 degree phase shift and the feedback element is forced to provide the other 180 degrees of phase shift.

R1 is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and to provide the start-up transition.

Capacitor C_2 combined with the amplifier output resistance provides a small phase shift. It will also provide some attenuation of overtones.

Capacitor C_1 combined with the crystal resistance provides additional phase shift.

3.4.1 Layout

Traces connecting crystal, caps, and the Z8® oscillator pins should be as short and wide as possible. This reduces parasitic inductance and resistance. The components (caps, crystal, resistors) should be placed as close as possible to the oscillator pins of the Z8.

The traces from the oscillator pins of the IC and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC}, address/data lines, system ground) to reduce cross talk and noise injection. This is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit and by placing a Z8 device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace to the Z8 V_{SS} (GND) pin. It should not be shared with any other system ground trace or components except at the Z8 device V_{SS} pin. This is to prevent differential system ground noise injection into the oscillator (Figure 3-6).

C_1 and C_2 can affect the start-up time if they increase dramatically in size. As C_1 and C_2 increase, the start-up time increases until the oscillator reaches a point where it does not start up any more.

It is recommended for fast and reliable oscillator start-up (over the manufacturing process range) that the load capacitors be sized as low as possible without resulting in overtone operation.

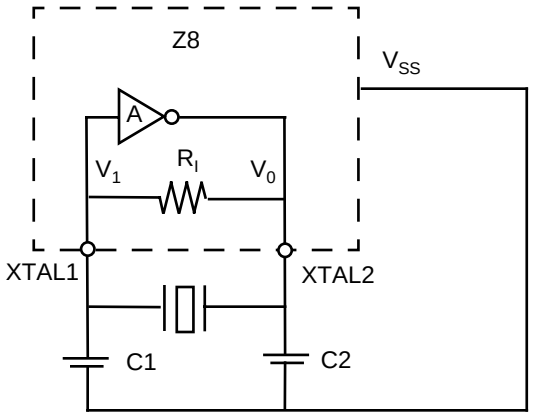

Figure 3-5. Pierce Oscillator with Internal Feedback Circuit

3.4.2 Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

Start-up Time. If start -up time is excessive, or varies widely from unit to unit, there is probably a gain problem. C1/C2 needs to be reduced; the amplifier gain is not adequate at frequency, or crystal Rs is too large.

Output Level. The signal at the amplifier output should swing from ground to V_{CC}. This indicates there is adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs, at which point the loop gain is effectively reduced to unity and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain may be a problem. Either C_1 or C_2 should be made smaller or a low-resistance crystal should be used.

3.4.3 Circuit Board Design Rules

The following circuit board design rules are suggested:

- To prevent induced noise the crystal and load capacitors should be physically located as close to the Z8® as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry and the internal system clock output should be separated as much as possible.
- V_{CC} power lines should be separated from the clock oscillator input circuitry.
- Resistivity between XTAL1 or XTAL2 and the other pins should be greater than 10 Mohms.

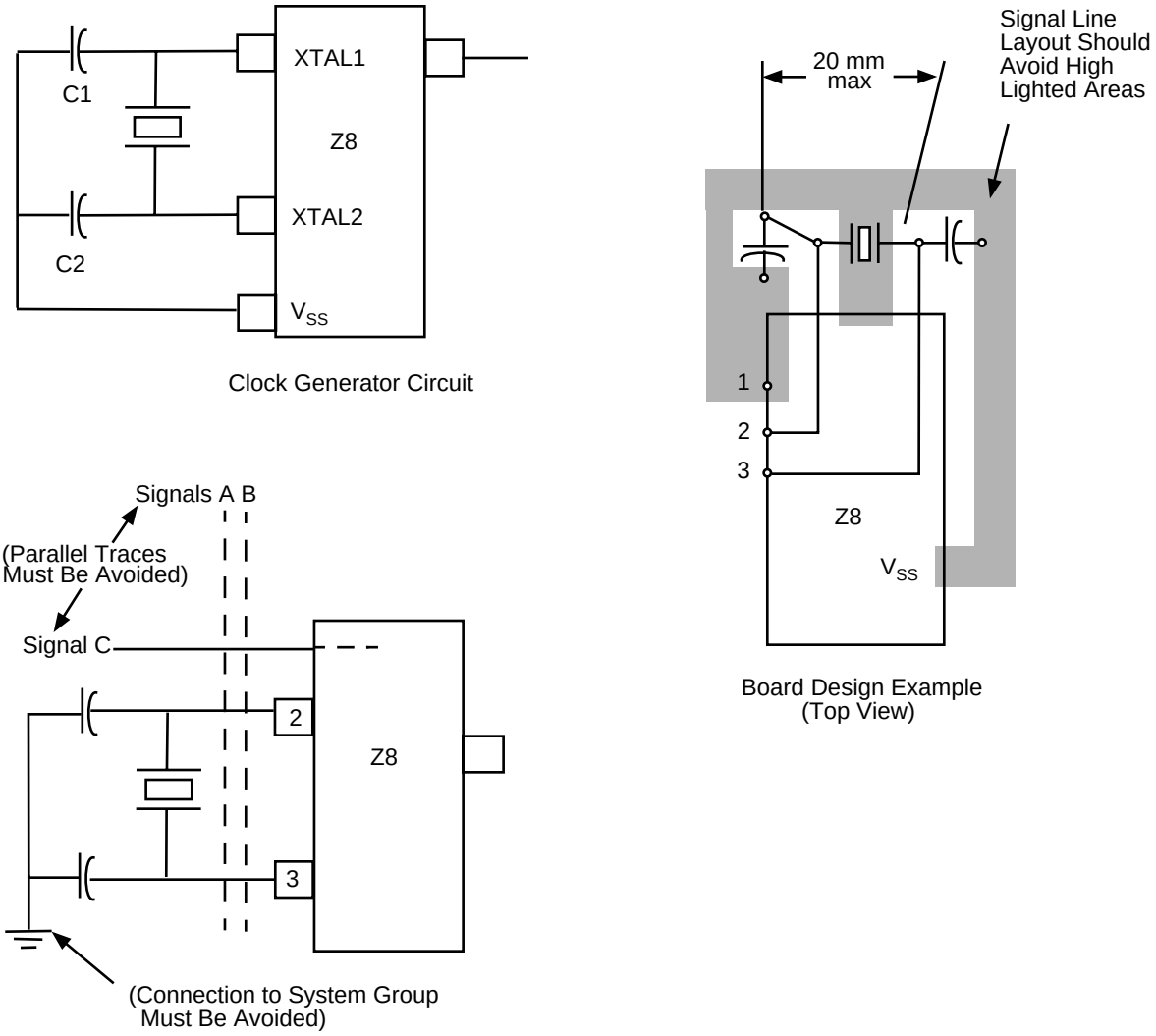

Figure 3-6. Circuit Board Design Rules

3.4.4 Crystals and Resonators

Crystals and ceramic resonators (Figure 3-7) should have the following characteristics to ensure proper oscillator operation:

Crystal Cut	AT (crystal only)
Mode	Parallel, Fundamental Mode
Crystal Capacitance	<7pF
Load Capacitance	10pF < CL < 220 pF, 15 typical
Resistance	100 ohms max

Depending on operation frequency, the oscillator may require the addition of capacitors C1 and C2 (shown in Figures 3-7). The capacitance values are dependent on the manufacturer's crystal specifications.

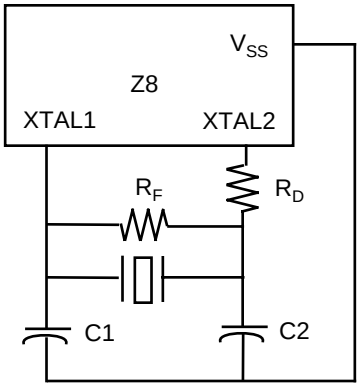

Figure 3-7. Crystal/Ceramic Resonator Oscillator

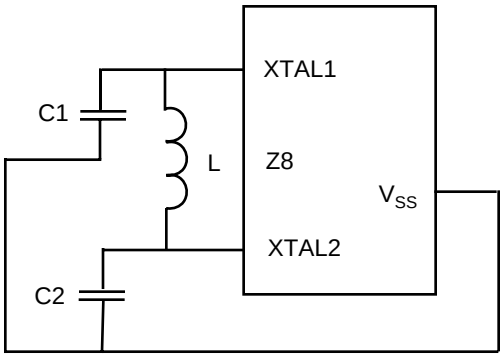

Figure 3-8. LC Clock

In most cases, the R_D is 0 Ohms and R_F is infinite. It is determined and specified by the crystal/ceramic resonator manufacturer. The R_D can be increased to decrease the amount of drive from the oscillator output to the crystal. It can also be used as an adjustment to avoid clipping of the oscillator signal to reduce noise. The R_F can be used to improve the start-up of the crystal/ceramic resonator. The Z8 oscillator already has an internal shunt resistor in parallel to the crystal/ceramic resonator.

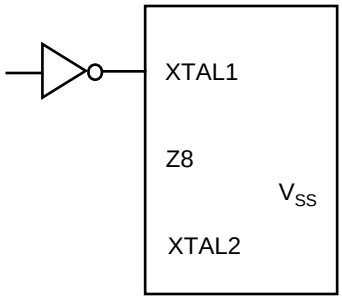

Figure 3-9. External Clock

It is recommended in Figures 3-7, 3-8, and 3-9 to connect the load capacitor ground trace directly to the V_{SS} (GND) pin of the Z8®. This ensures that no system noise is injected into the Z8 clock. This trace should not be shared with any other components except at the V_{SS} pin of the Z8.

In some cases, the Z8 XTAL1 pin also functions as one of the EPROM high-voltage mode programming pins or as a special factory test pin. In this case, applying 2 V above V_{CC} on the XTAL1 pin will cause the device to enter one of these modes. Since this pin accepts high voltages to enter these respective modes, the standard input protection diode to V_{CC} is not on XTAL1. It is recommended that in applications where the Z8 is exposed to much system noise, a diode from XTAL1 to V_{CC} be used to prevent accidental enabling of these modes. This diode will not affect the crystal/ceramic resonator operation.

Please note that a parallel resonant crystal or resonator data sheet will specify a load capacitor value that is the series combination of C_1 and C_2, including all parasitics (PCB and holder).

3.5 LC OSCILLATOR

The Z8 oscillator can use a LC network to generate a XTAL clock (Figure 3-8).

The frequency stays stable over V_{CC} and temperature. The oscillation frequency is determined by the equation:

$$\text{Frequency} = \frac{1}{2\,\pi\,(LCT)1/2}$$

where L is the total inductance including parasitics and C_T is the total series capacitance including the parasitics.

Simple series capacitance is calculated using the following equation:

$$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2}$$

$$\text{If } C_1 = C_2$$

$$\frac{1}{C_T} = \frac{2}{C_1}$$

$$C_1 = 2CT$$

Sample calculation of capacitance C_1 and C_2 for 5.83 MHz frequency and inductance value of 27 uH:

$$5.83\ (10\text{^}6) = \frac{1}{2\pi\,[2.7\ (10^{-6})\ CT]\ 1/2}$$

$$CT = 27.6\ pf$$

Thus C_1 = 55.2 pf and C_2 = 55.2 pf.

3.6 RC OSCILLATOR

In some cases, the Z8® has a RC oscillator option. Please refer to the specific product specification for availability. The RC oscillator requires a resistor across XTAL1 and XTAL2. An additional load capacitor is required from the XTAL1 input to V_{SS} pin (Figure 3-10).

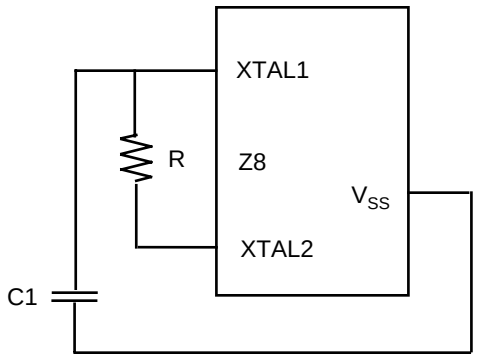

Figure 3-10. RC Clock