CHAPTER 10
EXTERNAL INTERFACE

10.1 INTRODUCTION

The Z8 can be a microcontroller with 20 pins for external memory interfacing. The external memory interface on the Z8 is generally for either RAM or ROM. This is only available for devices featuring Port 0, Port 1, R//W, /DM, /AS, and /DS. Please refer to specific product specifications for availability of these features.

The Z8 has a multiplexed external memory interface. In the multiplexed mode, eight pins from Port 1 form an Address/Data Bus (AD7-AD0), eight pins from Port 0 form a High Address Bus (A15-A8). Three additional pins provide the Address Strobe, Data Strobe, and the Read/Write Signal. Figure 10-1 shows the Z8 external interface pins.

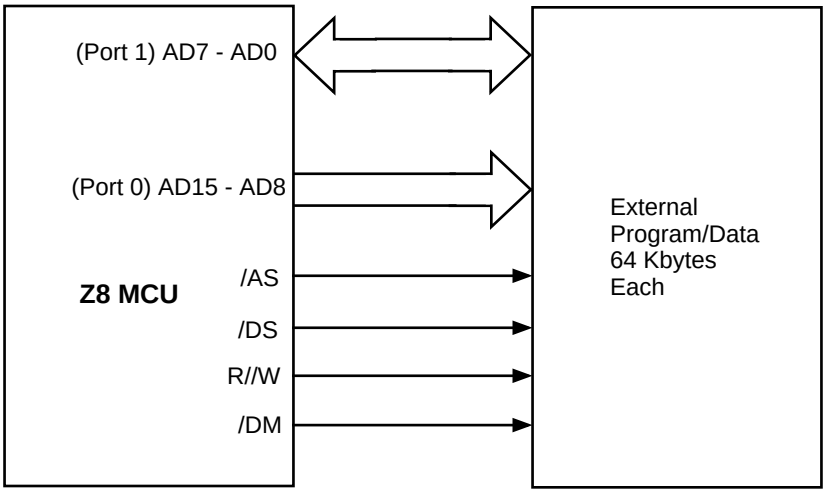


Figure 10-1. Z8 External Interface Pins

10.2 PIN DESCRIPTIONS

The following sections briefly describe the pins associated with the Z8® external memory interface.

10.2.1 /AS

Address Strobe (output, active Low). Address Strobe is pulsed Low once at the beginning of each machine cycle. The rising edge of /AS indicates the address, Read/Write (R//W), and Data Memory (/DM) signals are valid for program or data memory transfers. In some cases, the Z8 address strobe is pulsed low regardless of accessing external or internal memory. Please refer to specific product specifications for /AS operation.

10.2.2 /DS

Data Strobe (output, active Low). Data Strobe provides the timing for data movement to or from the Address/Data bus for each external memory transfer. During a Write Cycle, data out is valid at the leading edge of the /DS. During a Read Cycle, data in must be valid prior to the trailing edge of the /DS.

10.2.3 R//W

Read/Write (output). Read/Write determines the direction of data transfer for memory transactions. R//W is Low when writing to program or data memory, and High for all other transactions.

10.2.4 DM

Data Memory (output). Data Memory provides a signal to separate External Program Memory from External Data Memory. It is a programmable function on pin P34. Data memory is active low for External Data Memory accesses and high for External Program Memory accesses.

10.2.5 P07 - P00

High Address Lines A15 -A8 (Outputs can be CMOS- or TTL- compatible. Please refer to product specifications for actual type). A15-A8 provide the High Address lines for the memory interface. Port 0 - 1 mode register must have bits D7 = 1 and D1 = 1 to configure Port 0 as A15 - A8 (Figure 10-2).

10.2.6 P17 - P10

Address/Data Lines AD7 - AD0 (inputs/outputs, TTL-compatible). AD7-AD0 is a multiplexed Address/Data memory interface. The lower eight Address lines (A7-A0) are multiplexed with Data lines (D7-D0). Port 0 - 1 mode register must have bits D4 = 1 and D3 = 0 to configure Port 1 as AD7 - AD0 (Figure 10-2).

10.2.7 /RESET

Reset (input, active Low). /RESET initializes the Z8. When /RESET is deactivated, program execution begins from program location 000CH. If held Low, /RESET acts as a register file protect during power-down and power-up sequences. To avoid asynchronous and noisy reset problems, the Z8 is equipped with a reset filter of four external clocks ($4T_PC$). If the external /RESET signal is less than $4T_PC$ in duration, no reset will occur. On the fifth clock after the /RESET is detected, an internal reset signal is latched and held for an internal register count of 18 or more external clocks, or for the duration of the external /RESET, whichever is longer. Please refer to specific product specifications for length of reset delay time.

10.2.8 XTAL1, XTAL2.

Crystal1, Crystal2 (Oscillator input and output). These pins connect a parallel-resonant crystal, ceramic resonator, LC, RC network, or external single-phase clock to the on-chip oscillator input. Please refer to the device product specifications for information on availability of RC oscillator features.

10.3 EXTERNAL ADDRESSING CONFIGURATION

The minimum bus configuration uses Port 1 as a multiplexed address / data port (AD7 - AD0), allowing access to 256 bytes of external memory. In this configuration, the eight low order bits (A0 - A7) are multiplexed with the data (D7 - D0).

Port 0 can be programmed to provide either four additional address lines (A11- A8), which increases the addressable memory to 4K bytes, or eight additional address lines (A15 - A8), which increases the addressable external memory up to 64K bytes. It is required to add a NOP after configuring Port 0 / Port 1 for external addressing before jumping to external memory execution.

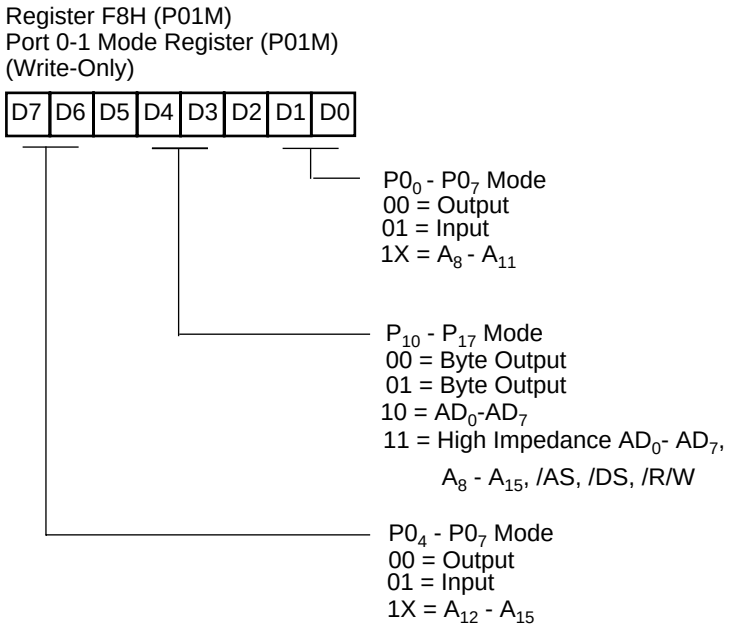


Figure 10-2. External Address Configuration

10.4 EXTERNAL STACKS

The Z8® architecture supports stack operations in either the Z8 Standard Register File or External Data Memory. A stack's location is determined by bit 2 in the Port 0-1 Mode Register (F8H). If bit 2 is set to 0, the stack is in External Data Memory. (Figure 10-3).

The instruction used to change the stack selection bit should not be immediately followed by the instructions RET or IRET, because this will cause indeterminate program flow. After a /RESET, the internal stack is selected.

Please note that if Port 0 is configured as A15 - A8 and the stack is selected as internal, any stack operation will cause the contents in register FEH to be displayed on Port 0.

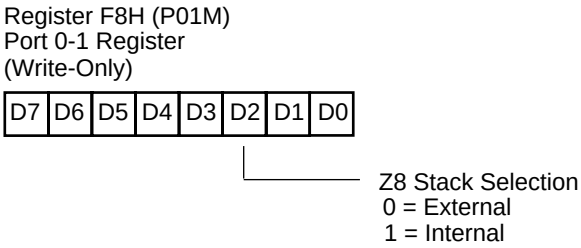


Figure 10-3. Z8 Stack Selection

10.5 DATA MEMORY

The two Z8 external memory spaces, data and program, are addressed as two separate spaces of up to 64 Kbytes each. External Program Memory and External Data Memory are logically selected by the Data Memory select output (/DM). /DM is made available on Port 3, bit 4 (P34) by setting bit 4 and bit 3 in the Port 3 Mode Register (F7H) to 10 or 01 (Figure 10-4). /DM is active Low during the execution of the LDE, LDEI instructions, and High for the execution of program instructions. /DM is also active Low during the execution of CALL, POP, PUSH, RET and IRET instructions if the stack resides in External Data Memory. After a /RESET, /DM is not selected.

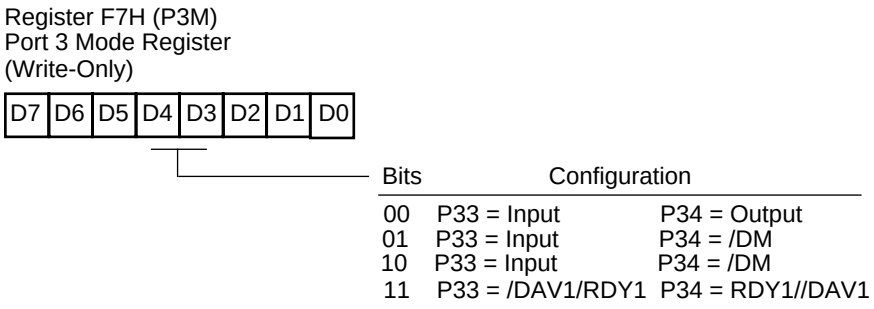
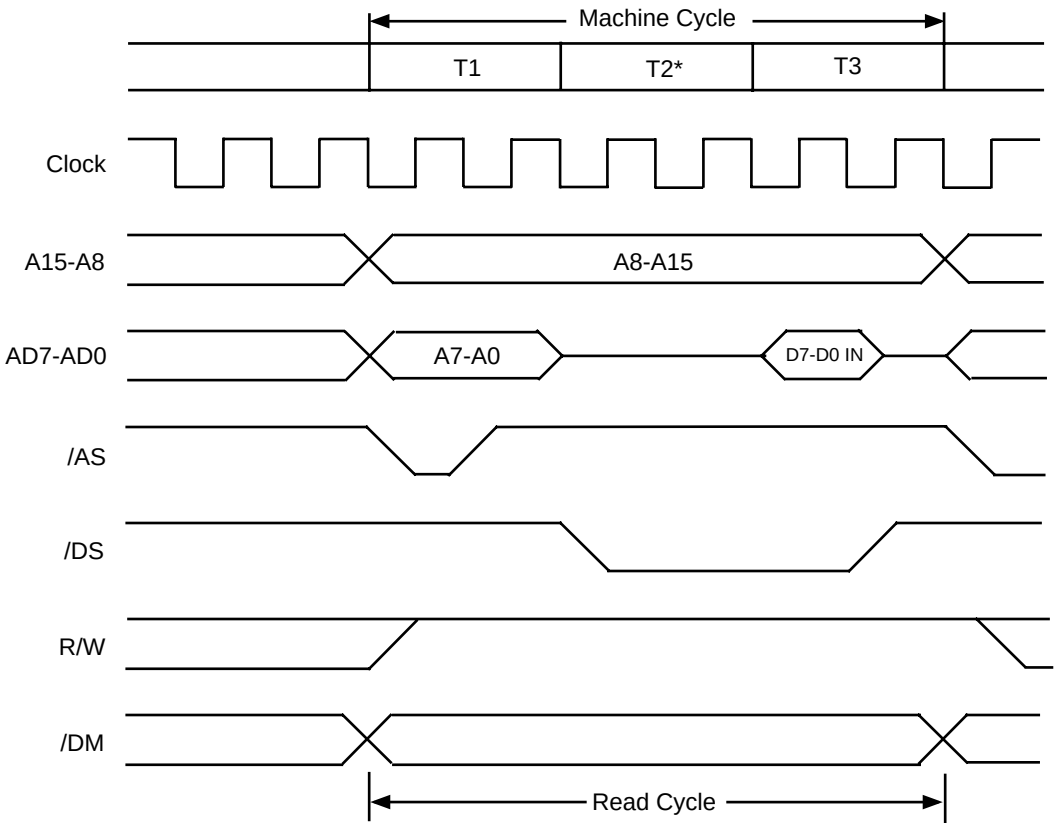


Figure 10-4. Port 3 Data Memory Operation

10.6 BUS OPERATION

Typical data transfers between the Z8 MCU and External Memory are illustrated in Figures 10-5 and 10-6. Machine cycles can vary from six to 12 clock periods depending on the operation being performed. The notations used to describe the basic timing periods of the Z8 are machine cycles (Mn), timing states (Tn), and clock periods. All timing references are made with respect to the output signals /AS and /DS. The clock is shown for clarity only and does not have a specific timing relationship with other signals.



*Port inputs are strobed during T2, which is two internal systems clocks before the execution cycle of the current instruction.

Figure 10-5. External Instruction Fetch or Memory Read Cycle

10.6 BUS OPERATION (Continued)

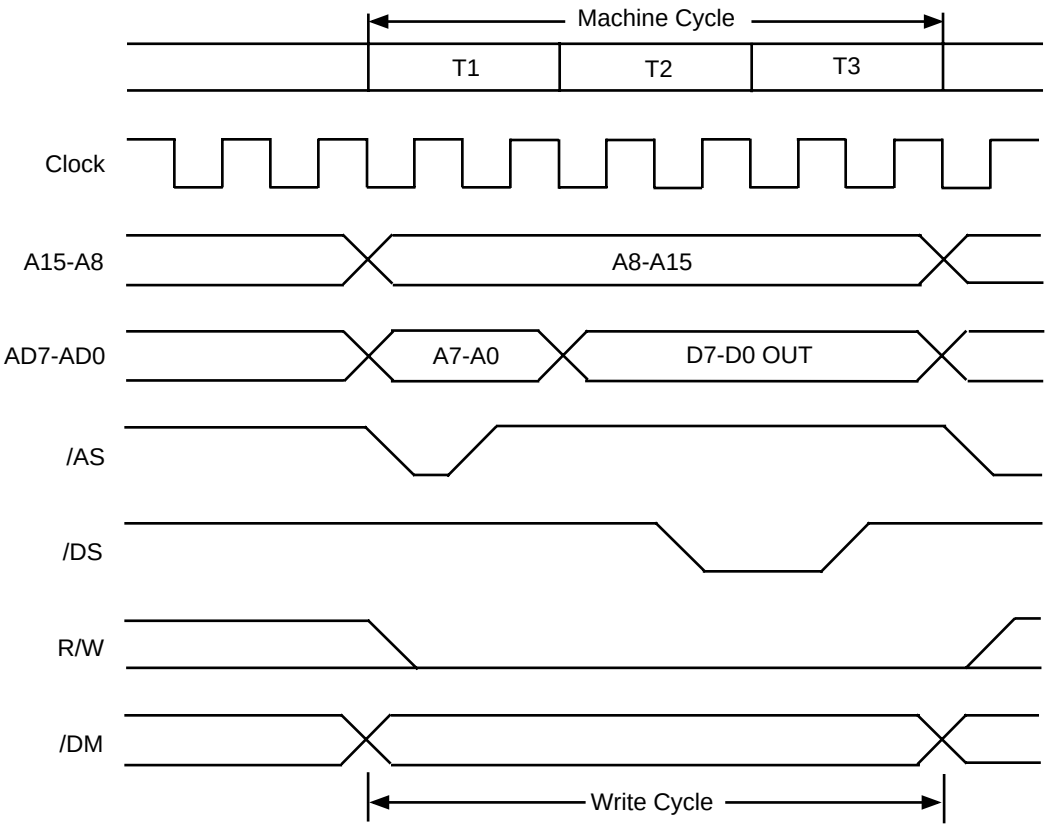


Figure 10-6. External Memory Write Cycle

10.6.1 Address Strobe (/AS)

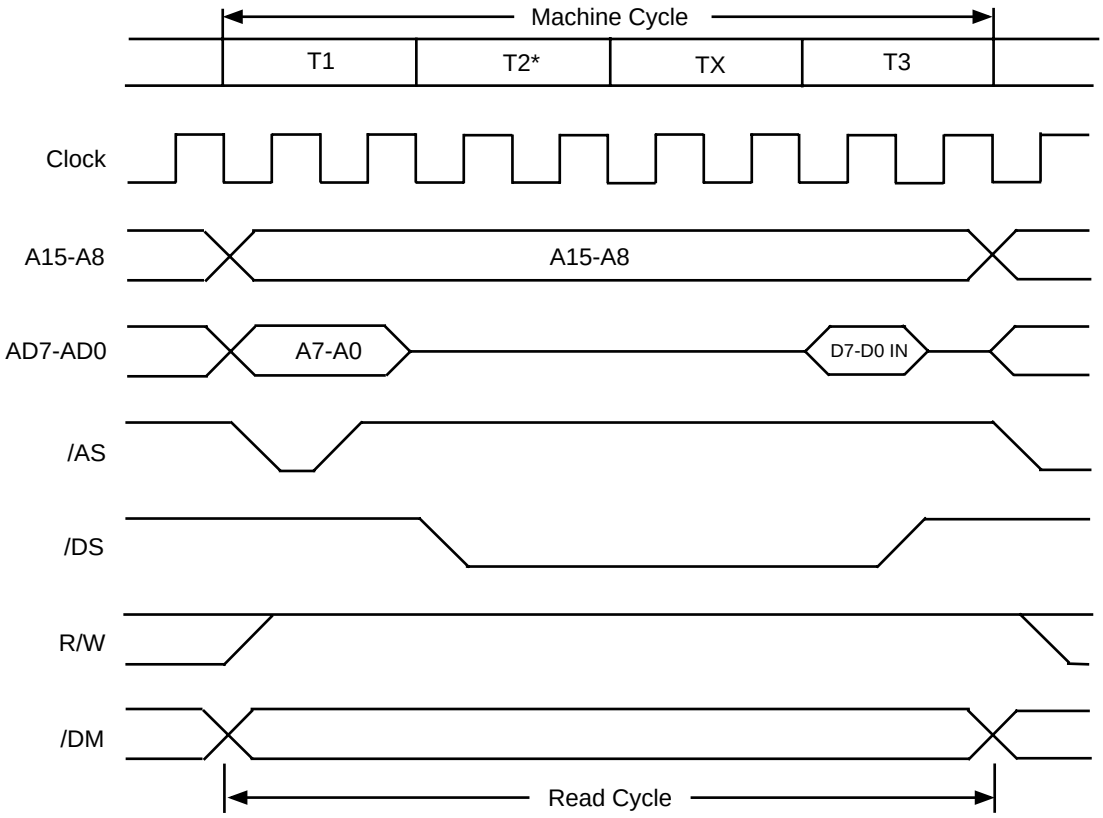
All transactions start with /AS driven Low and then raised High by the Z8 MCU. The rising edge of /AS indicates that R//W, /DM (if used), and the address outputs are valid. The address outputs (AD7-AD0), remain valid only during MnT1 and typically need to be latched using /AS. Address outputs (A15-A8) remain stable throughout the machine cycle, regardless of the addressing mode.

10.6.2 Data Strobe (/DS)

The Z8 uses /DS to time the actual data transfer. For Write operations (R//W = Low), a Low on /DS indicates that valid data is on the AD7-AD0 lines. For Read operations (R/W = High), the bus is placed in a high-impedance state before driving /DS Low, so the addressed device can put its data on the bus. The Z8 samples this data prior to raising /DS High.

10.7 EXTENDED BUS TIMING

Some products can accommodate slow memory access time by automatically inserting an additional software controlled state time (Tx). This stretches the /DS timing by two clock periods. Figures 10-7 and 10-8 illustrate extended external memory Read and Write cycles.



*Port inputs are strobed during T2, which is two internal system clocks before the execution of the current instruction.

Figure 10-7. Extended External Instruction Fetch or Memory Read Cycle

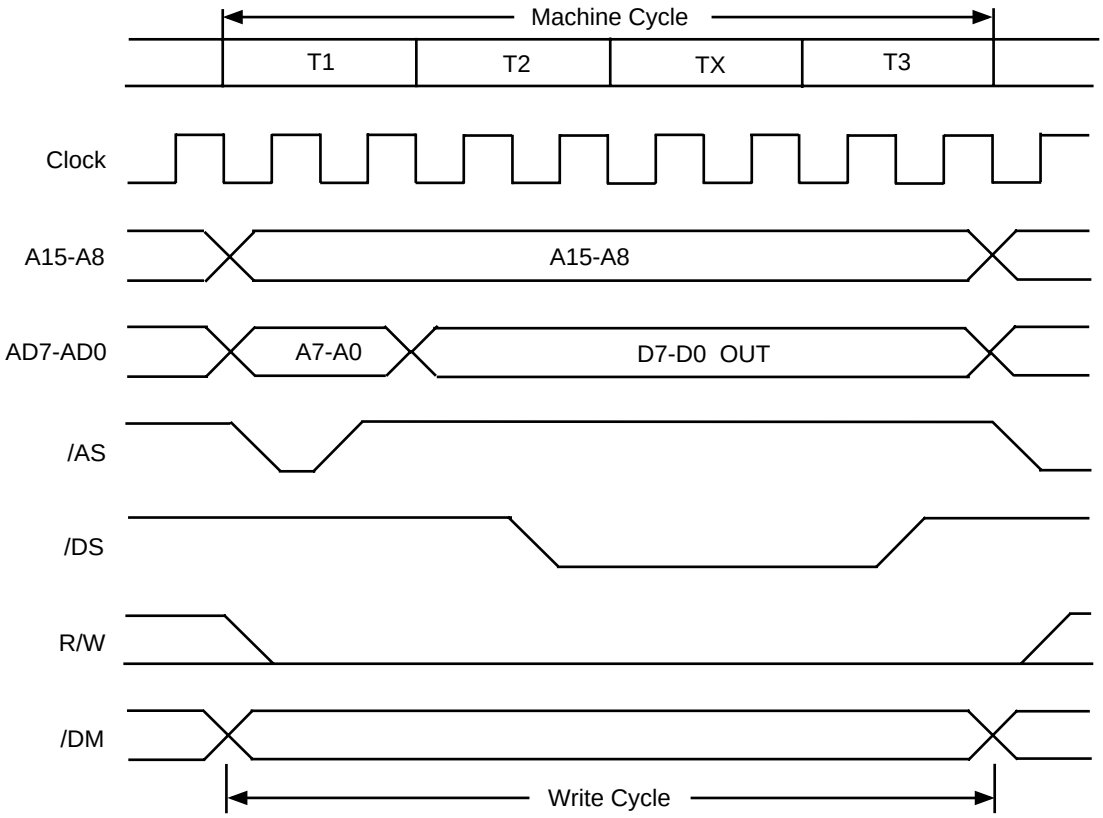


Figure 10-8. Extended External Memory Write Cycle

Timing is extended by setting bit D5 in the Port 0-1 Mode Register (F8H) to 1 (Figure 10-9). After a /RESET, this bit is set to 0.

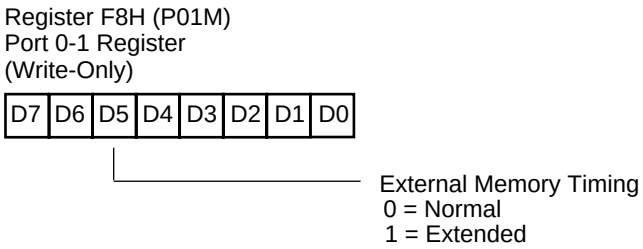


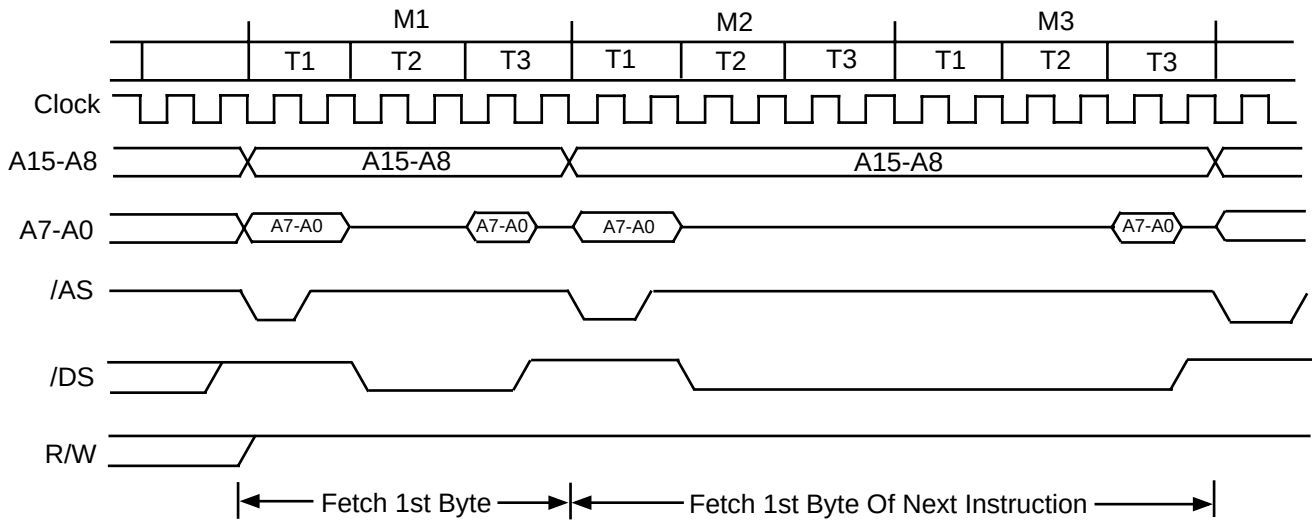
Figure 10-9. Extended Bus Timing

10.8 INSTRUCTION TIMING

The High throughput of the Z8 is due, in part, to the use of an instruction pipeline, in which the instruction fetch and execution cycles are overlapped. During the execution of the current instruction, the opcode of the next instruction is fetched. Instruction pipelining is illustrated in Figure 10-10.

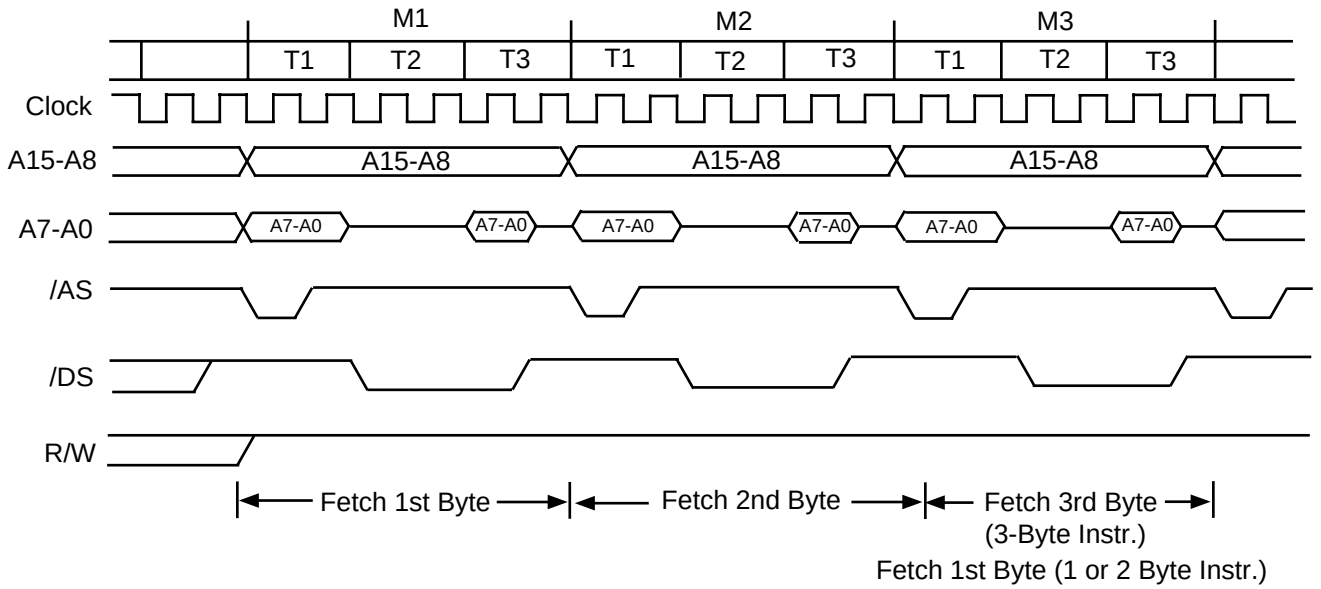
Figures 10-10 and 10-11 show typical instruction cycle timing for instructions fetched from memory. For those instructions that require execution time longer than that of the overlapped fetch, or reference program or data memory as part of their execution, the pipe must be flushed.

Figures 10-10 and 10-11 assume the XTAL/2 clock mode is selected.



* Port inputs are strobed during T2, which is two internal system clocks before the execution cycle of the current installation

Figure 10-10. Instruction Cycle Timing (One-Byte Instructions)



*Port inputs are strobed during T2, which is two internal system clocks before the execution cycle of the current instruction.

Figure 10-11. Instruction Cycle Timing (Two and Three Byte Instructions)

10.9 Z8 RESET CONDITIONS

After a hardware reset, extended timing is set to accommodate slow memory access during the configuration routine, /DM is inactive, the stack resides in the register file. Port 0, 1, and 2 are reset to input mode. Port 2 is set to Open-Drain Mode.