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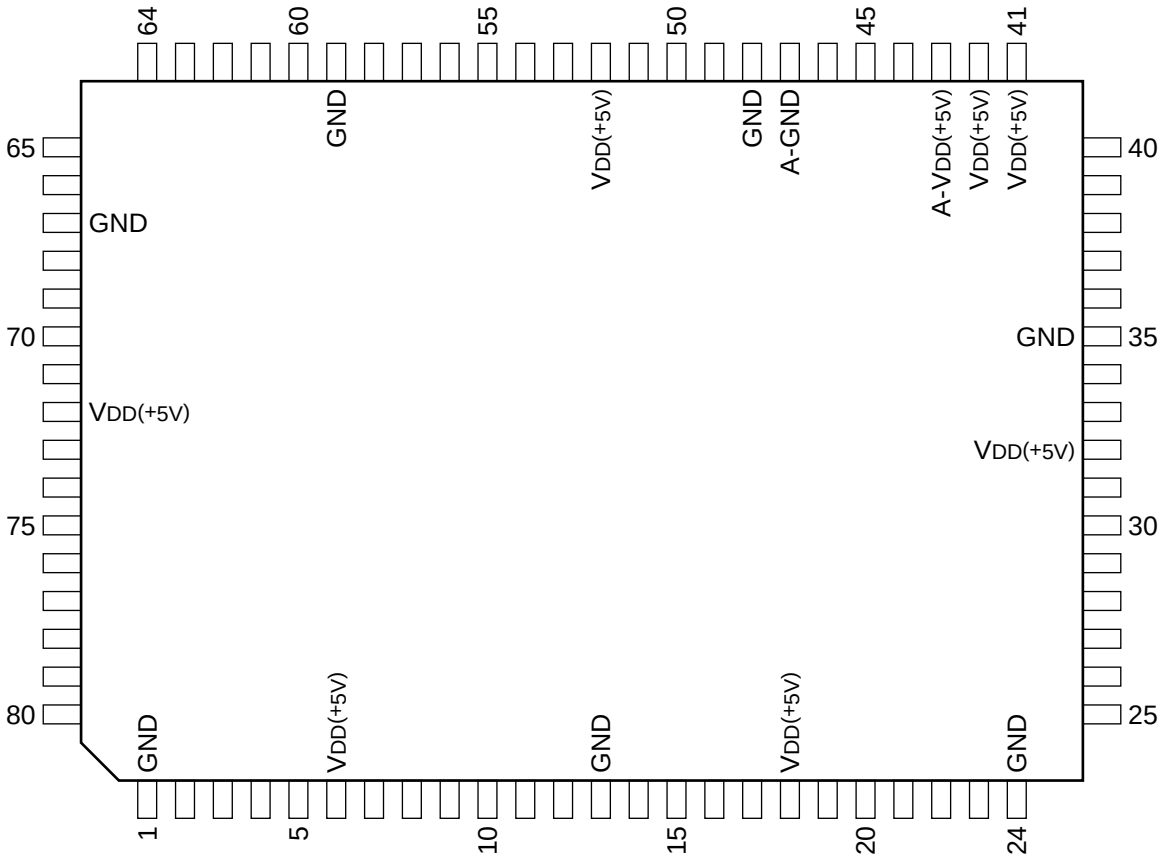
C-MOS ADVANCED VIDEO DISPLAY PROCESSER

-TOP VIEW-

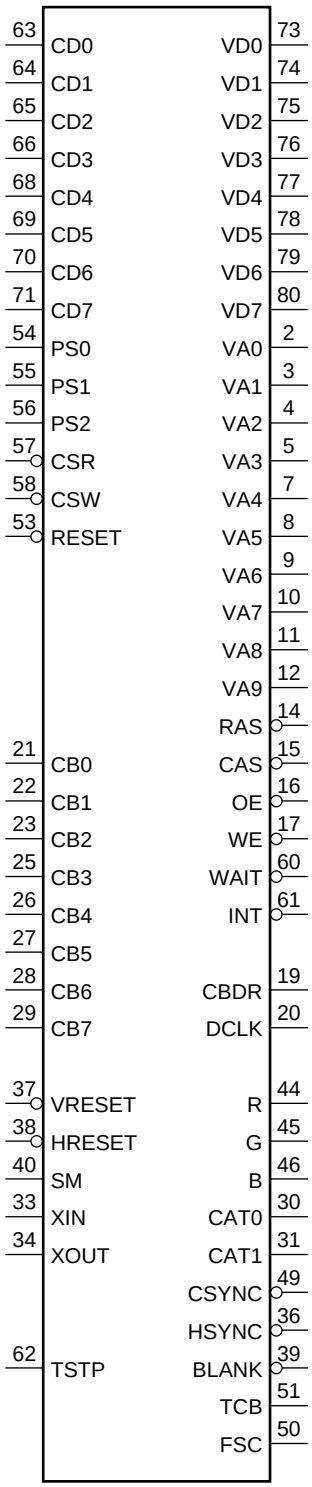


A-VDD, A-GND : FOR ANALOG(R, G, B)

VDD, GND : FOR DIGITAL

(A-VDD,VDD = +5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	–	GND	21	I/O	CB0	41	–	VDD	61	O	$\overline{INT}$
2	O	VA0	22	I/O	CB1	42	–	VDD	62	I	TSTP
3	O	VA1	23	I/O	CB2	43	–	A-VDD	63	I/O	CD0
4	O	VA2	24	–	GND	44	O	R	64	I/O	CD1
5	O	VA3	25	I/O	CB3	45	O	G	65	I/O	CD2
6	–	VDD	26	I/O	CB4	46	O	B	66	I/O	CD3
7	O	VA4	27	I/O	CB5	47	–	A-GND	67	–	GND
8	O	VA5	28	I/O	CB6	48	–	GND	68	I/O	CD4
9	O	VA6	29	I/O	CB7	49	O	$\overline{CSYNC}$	69	I/O	CD5
10	O	VA7	30	O	CAT0	50	O	FSC	70	I/O	CD6
11	O	VA8	31	O	CAT1	51	O	TCB	71	I/O	CD7
12	O	VA9	32	–	VDD	52	–	VDD	72	–	VDD
13	–	GND	33	I	XIN	53	I	$\overline{RESET}$	73	I/O	VD0
14	O	$\overline{RAS}$	34	O	XOUT	54	I	PS0	74	I/O	VD1
15	O	$\overline{CAS}$	35	–	GND	55	I	PS1	75	I/O	VD2
16	O	$\overline{OE}$	36	O	$\overline{HSYNC}$	56	I	PS2	76	I/O	VD3
17	O	$\overline{WE}$	37	I	$\overline{VRESET}$	57	I	$\overline{CSR}$	77	I/O	VD4
18	–	VDD	38	I	$\overline{HRESET}$	58	I	$\overline{CSW}$	78	I/O	VD5
19	O	CBDR	39	O	$\overline{BLANK}$	59	–	GND	79	I/O	VD6
20	O	DCLK	40	I	SM	60	O	$\overline{WAIT}$	80	I/O	VD7



INPUT

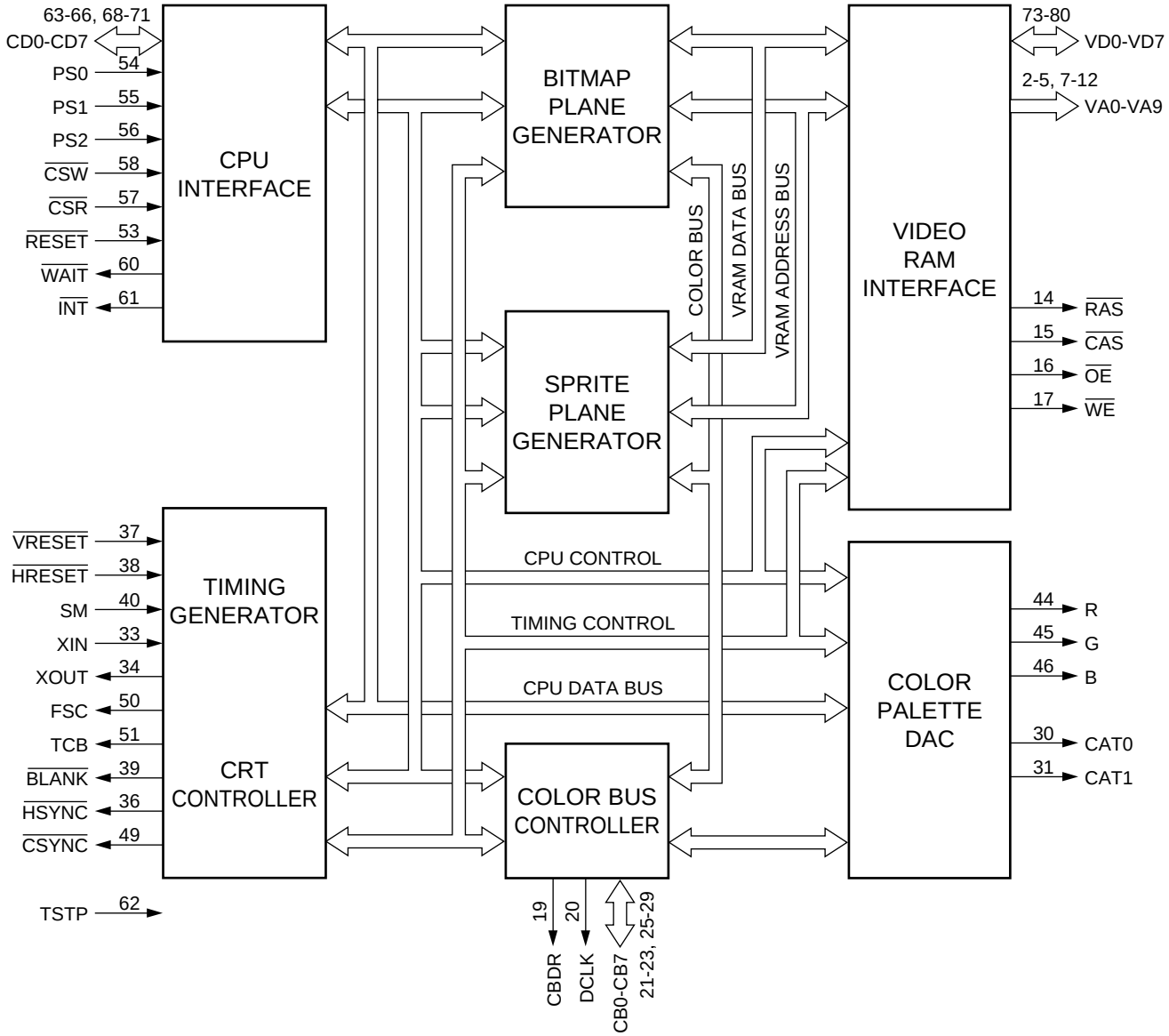
$\overline{\text{CSR}}$	;	DATA READ STROBE
$\overline{\text{CSW}}$	;	DATA WRITE STROBE
$\overline{\text{HRESET}}$	;	HORIZONTAL TIMING RESET
PS0-PS2	;	APPOINT NUMBER INPUT/OUTPUT PORT
$\overline{\text{RESET}}$	;	POWER ON RESET
SM	;	SCAM MODE SELECT (L : PAL/H : NTSC)
TSTP	;	TEST FOR INTERNAL CIRCUIT
$\overline{\text{VRESET}}$	;	VERTICAL TIMING RESET
XIN	;	CLOCK IN

OUTPUT

B	;	ANALOG LINEAR B
$\overline{\text{BLANK}}$	;	BLANKING
$\overline{\text{CAS}}$	;	DRAM COLUMN ADDRESS STROBE FOR VIDEO RAM
CAT0,CAT1	;	COLOR CODE ATTRIBUTE TIMING
CBDR	;	CHARACTOR COLOR CODE SELECT (L : CB0-CB7 INPUTS/H : CB0-CB7 OUTPUTS)
$\overline{\text{CSYNC}}$	;	COMPLEX SYNC OR VERTICAL SYNC
DCLK	;	DOT CLOCK
FSC	;	SUB-CARRIER CLOCK FOR NTSC VIDEO ENCODER
G	;	ANALOG LINEAR G
$\overline{\text{HSYNC}}$	;	HORIZONTAL SYNC
$\overline{\text{INT}}$	;	INTERRUPT REQUEST
$\overline{\text{OE}}$	;	DRAM DATA OUTPUT ENABLE FOR VIDEO RAM
R	;	ANALOG LINEAR R
$\overline{\text{RAS}}$	;	DRAM ROW ADDRESS STROBE FOR VIDEO RAM
TCB	;	COLOR BURST INSERT TIMING
VA0-VA9	;	ADDRESS BUS FOR VIDEO RAM
$\overline{\text{WAIT}}$	;	WAIT
$\overline{\text{WE}}$	;	DRAM WRITE ENABLE FOR VIDEO RAM
XOUT	;	CLOCK OUT

INPUT/OUTPUT

CB0-CB7	;	CHARACTOR COLOR CODE
CD0-CD7	;	8-BIT DATA BUS FOR CPU
VD0-VD7	;	8-BIT DATA BUS FOR VIDEO RAM


63-66, 68-71
CD0-CD7
PS0
54
PS1
55
PS2
56
CSW
58
CSR
57
RESET
53
WAIT
60
INT
61
CPU INTERFACE
BITMAP PLANE GENERATOR
SPRITE PLANE GENERATOR
COLOR BUS
VRAM DATA BUS
VRAM ADDRESS BUS
VIDEO RAM INTERFACE
73-80
VD0-VD7
2-5, 7-12
VA0-VA9
14
RAS
15
CAS
16
OE
17
WE
VRESET
37
HRESET
38
SM
40
XIN
33
XOUT
34
FSC
50
TCB
51
BLANK
39
HSYNC
36
CSYNC
49
TSTP
62
TIMING GENERATOR
CRT CONTROLLER
CPU CONTROL
TIMING CONTROL
CPU DATA BUS
COLOR BUS CONTROLLER
COLOR PALETTE DAC
44
R
45
G
46
B
30
CAT0
31
CAT1
19
CBDR
20
DCLK
CB0-CB7
21-23, 25-29