E3 (34.368 MBPS) Integrated Line Receiver

GENERAL DESCRIPTION

The XR-T7295E E3 Integrated Line Receiver is a fully integrated receive interface that terminates a bipolar E3 (34.368 MBPS) signal transmitted over coaxial cable. This device can be used with the XR-T7296 Integrated Line Transmitter (See Figure 10).

The device provides the functions of receive equalization (optional), automatic-gain control (AGC), clock-recovery and data retiming, loss-of-signal and loss-of-frequency-lock detection. The digital system interface is dual-rail, with received positive and negative 1s appearing as unipolar digital signals on separate output leads. The on-chip equalizer is designed for cable losses of 0 to 15dB. The receive input has a variable input sensitivity control, providing three different sensitivity settings. High input sensitivity allows for significant amounts of flat loss or for use with input signals at the monitor level. Figure 1 shows the block diagram of the device.

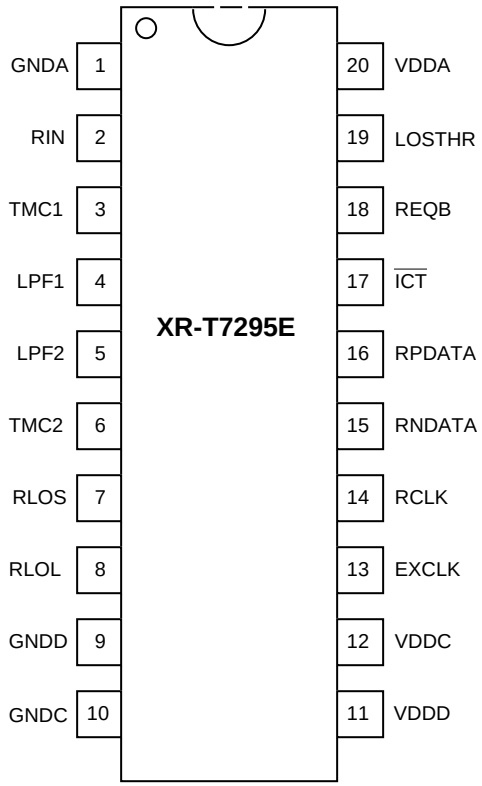
The XR-T7295E device is manufactured by using linear CMOS technology. The XR-T7295E is available in either a 20-pin plastic DIP or 20-pin plastic SOJ package for surface mounting. A pin compatible version is available for DS3 or STS-1 applications. Please refer to the XR-T7295 datasheet.

FEATURES

Fully integrated receive interface for E3 signals
Integrated equalization (optional) and timing recovery
Loss-of-signal and loss-of-lock alarms
Variable input sensitivity control
5V power supply
Compliant with G.703, G.775 and G.824 specifications

APPLICATIONS

Interface to E3 networks
CSU/DSU equipment
PCM test equipment
Fiber optic terminals
Multiplexers



PIN ASSIGNMENT

Note: Pin assignment is for DIP and SOJ packages

ORDERING INFORMATION

Part Number	Packages	Operating Temperature
XR-T7295-1EIP	PDIP	-40°C to+85°C
XR-T7295-1EIW	SOJ	-40°C to+85°C

ABSOLUTE MAXIMUM RATINGS

Power Supply	-0.5V to +6.5V
Storage Temperature	-40°C to +125°
Voltage at any Pin	-0.5V to VDD +0.5V
Power Dissipation	700mW
Maximum allowable Voltages (RIN) with respect tp GND	-0.5V to +5V

EXAR Corporation • 48720 Kato Road, Fremont, CA 94538 • (510)668-7000 • (510)668-7017 fax

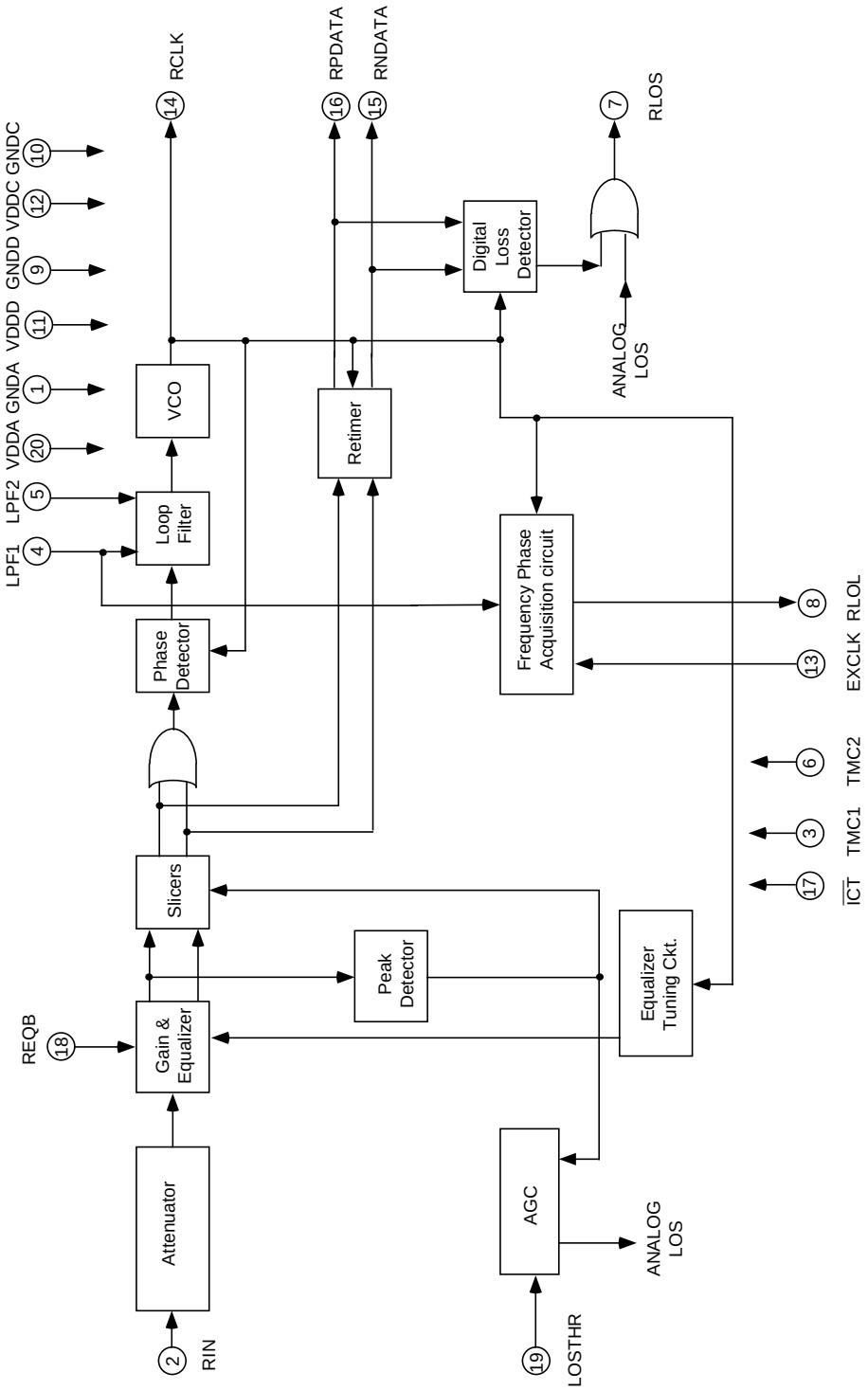


Figure 1. Block Diagram

PIN DESCRIPTION

PIN#	SYMBOL	TYPE	DESCRIPTION
1	GNDA	–	**Analog Ground.**
2	RIN	I	**Receive Input.** Unbalanced analog receive input.
3,6	TMC1-TMC2	I	**Test Mode Control 1 and 2**. Internal test modes are enabled within the device by using TMC1 and TMC2. Users must tie these pins to the ground plane.
4,5	LPF1-LPF2	I	**PLL Filter 1 and 2.** An external capacitor (0.1µF ± 20%) is connected between these pins (See Figure 3).
7	RLOS	O	**Receive Loss-of-Signal.** This pin is set high on loss of signal at the receive input.
8	RLOL	O	**Receive PLL Loss-of-Lock.** This pin is set high on loss of PLL frequency lock.
9	GNDD	–	**Digital Ground for PLL Clock.** Ground lead for all circuitry running synchronously with PLL clock.
10	GNDC	–	**Digital Ground for EXCLK.** Ground lead for all circuitry running synchronously with EXCLK.
11	VDDD	–	**5V Digital Supply (±10%) for PLL Clock.** Power for all circuitry running synchronously with PLL clock.
12	VDDC	–	**5V Digital Supply (±10%) for EXCLK.** Power for all circuitry running synchronously with EXCLK.
13	EXCLK	I	**External Reference Clock.** A valid E3 (34.368MHz ± 100ppm) clock must be provided at this input. The duty cycle of EXCLK, referenced to VDD/2 levels, must be 40%-60%.
14	RCLK	O	**Receive Clock.** Recovered clock signal to the terminal equipment.
15	RNDATA	O	**Receive Negative Data**. Negative pulse data output to the terminal equipment.
16	RPDATA	O	**Receive Positive Data.** Positive pulse data output to the terminal equipment
17	$\overline{\text{ICT}}$	I	**Output In-Circuit Test Control** (Active-Low). If $\overline{\text{ICT}}$ is forced low, all digital output pins (RCLK, RPDATA, RNDATA, RLOS, RLOL) are placed in a high-Impedance state to allow for in-circuit testing.
18	REQB	I	**Receive Equalization Bypass.** A high on this pin bypasses the internal equalizer. A low places the equalizer in the data path.
19	LOSTHR	I	**Loss-of-Signal Threshold Control.** The voltage forced on this pin controls the input loss-of-signal threshold. Three settings are provided by forcing GND, VDD/2, or VDD at LOSTHR.
20	VDDA	–	**5 V Analog Supply (±10%).**

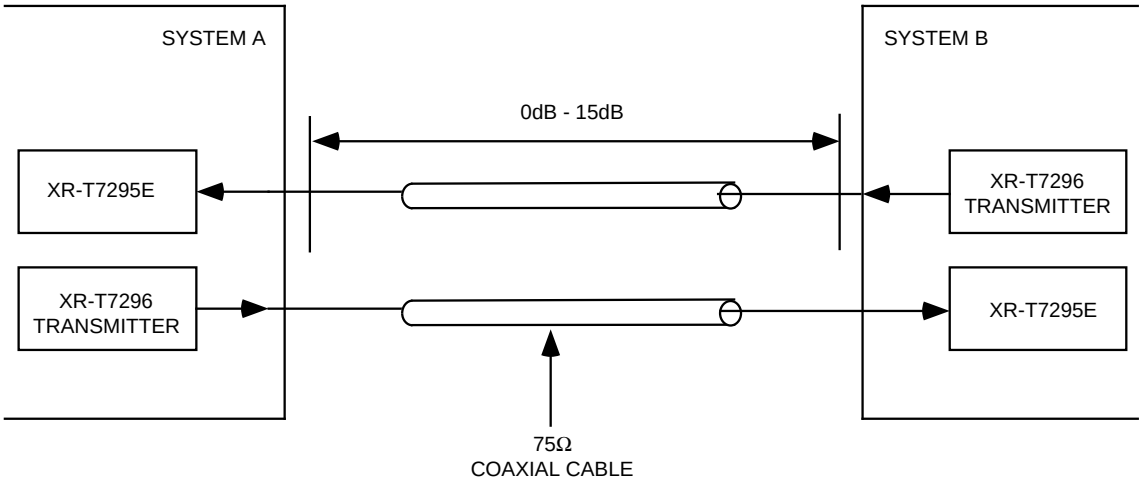


Figure 2. Application Diagram

SYSTEM DESCRIPTION

Receive Path Configurations

The diagram in Figure 2 shows a typical system application for the T7295E device. In the receive signal path (see Figure 1), the internal equalizer can be included by setting REQB = 0 or bypassed by setting REQB = 1. The equalizer bypass option allows easy interfacing of the T7295E device into systems already containing external equalizers. Figure 3 illustrates the receive path options for two separate cases.

In case 1, the signal from the coaxial cable feeds directly into the RIN input. In this mode, the user should set REQB = 0, engaging the equalizer in the data path if the cable loss is greater than 6dB. If the cable loss is less than 6dB, the equalizer is bypassed by setting REQB = 1.

In case 2, an external line and equalizer network precedes the T7295E device. In this mode, the signal at RIN is already equalized, and the on-chip equalizer should be bypassed by setting REQB1 = 1. In both case 1 and case 2, the signal at RIN must meet the amplitude limits described in Table 1.

The recommended receive termination is also shown in Figure 3. The 75Ω resistor terminates the coaxial cable with its characteristic impedance. In Figure 3 case 2, if the fixed equalizer includes the line termination, the 75Ω resistor is not required. The signal is ac coupled through the 0.01µF capacitor to RIN. The dc bias at RIN is generated internally. The input capacitance at the RIN pin is typically 2.8pF (SOJ package) and 3.6pF (DIP package).

Pulse Mask at the 34.368 MBPS Interface

Table 2 shows the pulse specifications at the transmitter output port and Figure 4 shows the pulse mask requirement for E3 as recommended in G.703.

REQB	LOSTHR	Minimum Signal		UNIT[3]
		SOJ[2]	DIP	
0	0	80	115	mV pk
	VDD/2	60	85	mV pk
	VDD	40	60	mV pk
1	0	80	115	mV pk
	VDD/2	80	115	mV pk
	VDD	80	115	mV pk

Table 1. Receive Input Signal Amplitude Requirements[1]

1 Maximum input amplitude under all conditions is 1.1 Vpk
2 The SOJ device performance is enhanced by decreased package parasitics.
3 Although system designers typically use power in dBm to describe input levels, the T7295E responds to peak input signal amplitude. Therefore, the T7295E input signal limits are given in mV pk.

Line Termination and Input Capacitance

The recommended receive termination is shown in Figure 3. The 75Ω resistor terminates the coaxial cable with its characteristic impedance. The 0.01µF capacitor to RIN couples the signal into the receive input without disturbing the internally generated dc bias level present on RIN. The input capacitance at the RIN pin is 2.8 pF (SOJ package) and 3.6 pF (DIP package).

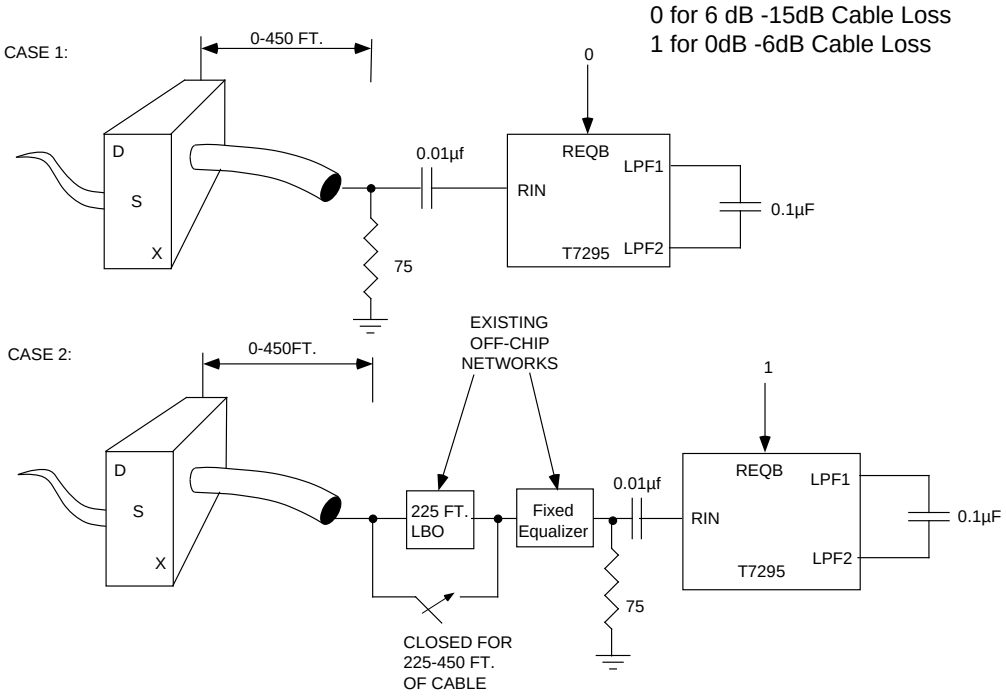


Figure 3. Receiver Configurations

External Loop Filter Capacitor

Figure 3 shows the connection to an external 0.1 µF capacitor at the LPF1/LPF2 pins. This capacitor is part of the PLL filter. A non-polarized, low-leakage capacitor should be used. A ceramic capacitor with the value 0.1 µF ± 20% is acceptable.

TIMING RECOVERY

Output Jitter

The total jitter appearing on the RCLK output during normal operation consists of two components. First, some jitter appears on RCLK because of jitter on the incoming signal. (The next section discusses the jitter transfer characteristic, which describes the relationship between input and output jitter.) Second, noise sources within the XR-T7295E device or noise sources that are coupled into the device through the power supplies create jitter on RCLK. The magnitude of this internally generated jitter is a function of the PLL bandwidth, which in turn is a function of the input 1s density. For higher 1s densities, the amount of generated jitter decreases. Generated jitter also depends on the quality of the power supply bypassing networks used. Figure 8 shows the suggested bypassing network, and Table 3 lists the typical generated jitter performance achievable with this network.

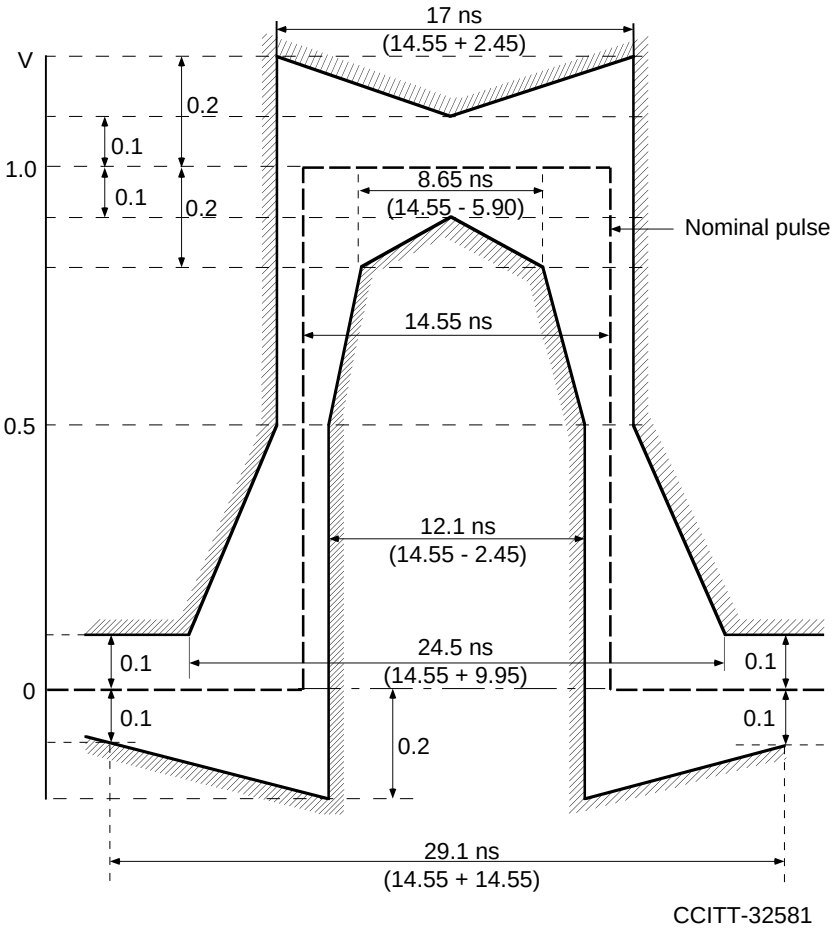


Figure 4. Pulse Mask at the 34.368 Mbit/s Interface

PARAMETER	VALUE
Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see Figure 4) , irrespective of the sign
Pair(s) in each direction	One coaxial pair
Test load impedance	75 ohms resistive
Nominal peak voltage of a mark (pulse)	1.0V
Peak voltage of a space (no pulse)	0V ± 0.1V
Nominal pulse width	14.55ns
Ratio of the amplitudes of positive and negative pulses at the center of a pulse interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05

Table 2. E3 Pulse Specification at the Transmitter Output Port

Jitter Transfer Characteristic

The jitter transfer characteristic indicates the fraction of input jitter that reaches the RCLK output as a function of input jitter frequency. Table 3 shows important jitter transfer characteristics parameters. Figure 6 also shows a typical characteristic, with the operating conditions as described in Table 3. Although standard documents do not specify jitter transfer characteristic requirements, the XR-T7295E device information is provided here to assist in evaluation of the device.

PARAMETER	TYP	MAX	UNIT
Generated Jitter*			
All-1s patter	1.0	-	ns peak-to-peak
Repetitive 1000 pattern	1.5	-	ns peak-to-peak
Jitter Transfer Characteristic••			
Peaking	0.05	0.1	dB
f 3dB	115	-	kHz

** Repetitive input data pattern at nominal E3 level with VDD = 5V TA = 25°C.*

•• Repetitive 1000 input at nominal E3 level with VDD = 5V, TA = 25°C.

Table 3. Generated Jitter and Jitter Transfer Characteristics

Jitter Accommodation

Under all allowable operating conditions, the jitter accommodation of the XR-T7295E device exceeds the limits for error-free operation (BER < $1E^{-9}$). The typical (V_{DD} = 5V, T = 25°C, E3 nominal signal level) jitter accommodation of the device is shown in Figure 6.

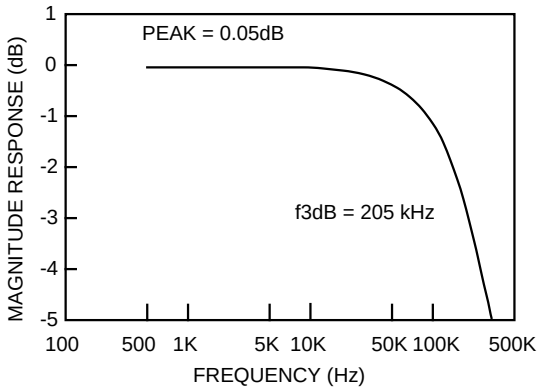


Figure 5. Typical PLL Jitter Transfer Characteristic

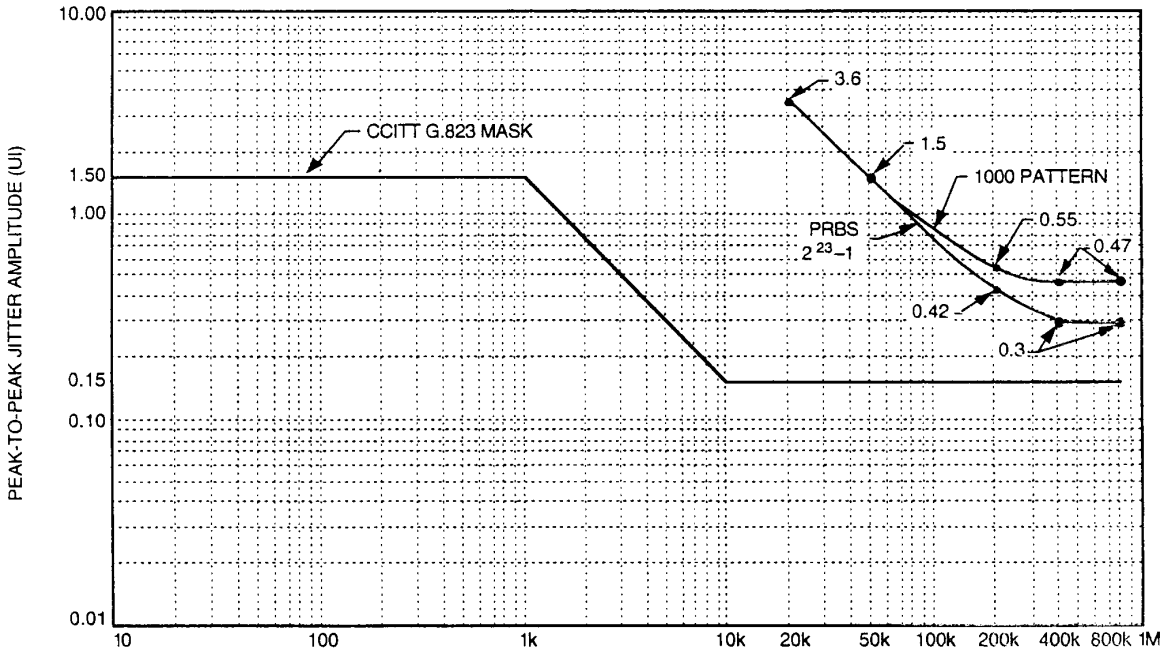


Figure 6. Lower Limit of Maximum Tolerable input jitter at 34.368 Mbit/s

False-Lock Immunity

False-lock is defined as the condition where a PLL recovered clock obtains stable phase-lock at a frequency not equal to the incoming data rate. The XR-T7295E device uses a combination frequency/phase-lock architecture to prevent false-lock. An on-chip frequency comparator continuously compares the EXCLK reference to the PLL clock. If the frequency difference between the EXCLK and PLL clock exceeds approximately ± 0.5% of EXCLK, correction circuitry acts to force re-acquisition of the proper frequency and phase.

Acquisition Time

If a valid input signals is assumed to be already present at RIN, the maximum time between the application of device power and error-free operation is 20 ms. If power has already been applied, the interval between the application of valid data and error-free operation is 4 ms.

Loss-of-Lock Indication

As stated above, the PLL acquisition aid circuitry monitors the PLL clock frequency relative to the EXCLK frequency.

The acquisition circuit also monitors the retimed data to detect possible phase-lock which is 180° out of a normal phase alignment. The RLOL alarm is activated if either or both of the following conditions exist:

- the difference between the PLL clock and the EXCLK frequency exceeds approximately ± 0.5%.
- the retimed data is 180° out of normal phase alignment.

A high RLOL output indicates that the acquisition circuit is working to bring the PLL into proper frequency lock. RLOL remains high until frequency lock has occurred; however, the minimum RLOL pulse width is 32 clock cycles.

DATA RATE	REQB	LOSTHR	THRESHOLD MIN.	THRESHOLD MAX.	UNIT
E3 34.368 MBPS	0	0	60	220	mV pk
		VDD/2	40	145	mV pk
		VDD	25	90	mV pk
	1	0	45	175	mV pk
		VDD/2	30	115	mV pk
		VDD	20	70	mV pk

Table 4. Analog Loss-of-Signal Thresholds

Notes: The RLOS alarm is an indication of the presence of an input signal, not a bit error rate indication. Table 1 gives the minimum input amplitude needed for error-free operation (BER<1E-9). Independent of the RLOS state, the device will attempt to recover correct timing and data.
The RLOS low-to-high transition typically occurs 1dB below the high-to-low transition.

Loss-of-Signal Detection

Figure 1 shows that analog and digital methods of loss-of-signal (LOS) detection are combined to create the RLOS alarm output. RLOS is set if either the analog or digital detection circuitry indicates LOS has occurred.

Analog Detection

The analog LOS detector monitors the peak input signal amplitude. RLOS makes a high-to-low transition (input signal regained) when the input signal amplitude exceeds the loss-of signal threshold defined in Table 4. The RLOS low-to-high transition (input signal loss) occurs at a level typically 1.0 dB below the high-to-low transition level. The hysteresis prevents RLOS chattering. Once set, the RLOS alarm remains high for at least 32 clock cycles, allow ing for system detection of a LOS condition without the use of an external alarm latch.

To allow for varying levels of noise and crosstalk in different applications, three loss-of-signal threshold settings are available using the LOSTHR pin.

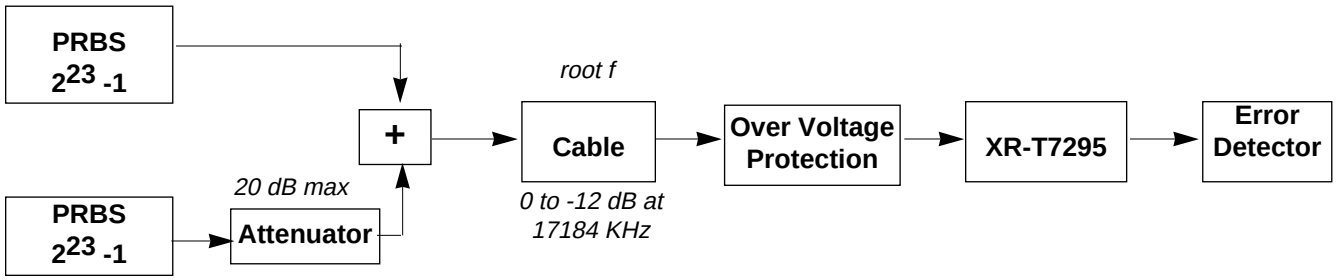


Figure 7. Test set-up for Interference Immunity Requirements

Setting LOSTHR = VDD provides the lowest loss-of-signal threshold; LOSTHR = VDD /2 (can be produced using two 50kΩ ±10% resistor as a voltage divider between VDDD and GNDD) provides an intermediate threshold. LOSTHR = GND provides the highest threshold. The LOSTHR pin must be set to its desired value at power up and must not be changed during operation.

Digital Detection

In addition to the signal amplitude monitoring of the analog LOS detector, the digital LOS detector monitors the recovered data 1s density. The RLOS alarm goes high if 160 ± 32 or more consecutive 0s occur in the receive data stream. The alarm goes low when at least eight 1s occur in a string of 32 consecutive bits. This hysteresis minimizes RLOS chattering and guarantees a minimum RLOS pulse width of 32 clock cycles.

Note: That RLOS chatter can still occur. When REQB = 1, input signal levels above the analog LOS threshold can still be low enough to result in a high bit error rate. The resultant data stream (containing errors) can temporarily activate the digital LOS detector, and RLOS chatter can occur. Therefore, RLOS should not be used as a bit error rate monitor. RLOS chatter can also occur when RLOL is activated (high).

Phase Hits

In response to a 180° phase hit in the input data, the T7295E returns to error-free operation in less than 2ms. During the reacquisition time, RLOS may temporarily be indicated.

Recovered Clock and Data Timing

Table 7 and Figure 9 summarize the timing relationships between the high-speed logic signals RCLK, RPDATA, and RNDATA. All duty cycle and timing relationships are referenced to VDD/2 threshold level. RPDATA and RNDATA change on the rising edge of RCLK and are valid during the falling edge of RCLK. A positive pulse at RIN creates and high level on RPDATA and a low level on RNDATA. A negative pulse creates a high level on RNDATA and a low level on RPDATA, and a received zero produces low levels on both RPDATA and RNDATA.

PARAMETER	MIN	TYP	MAX	UNIT
Attenuator	-20			dB

Table 5. Interference Requirement

Interference Immunity

The XR-T7295E complies with the interference test detailed in the Figure 7 and Table 5. The two data generators are non-synchronous.

In-Circuit Test Capability

When pulled low, the $\overline{ICT}$ pin forces all digital output buffers (RCLK, RPDATA, RNDATA, RLOS, RLOL pins) to be placed in a high output impedance state. This feature allows in-circuit testing to be done on neighboring devices without concern for XR-T7295E device buffer damage. When forced high, the $\overline{ICT}$ pin does not affect device operation. An internal pull-up device (nominally 50 kΩ) is provided on this pin; therefore, users can leave this pin open for normal operation. This is the only pin for which internal pull-up/pull-down is provided.

RECOMMENDED OPERATING CONDITIONS

T_A = -40°C to +85°C, VDD = 5V ± 10%

Electrical Characteristics

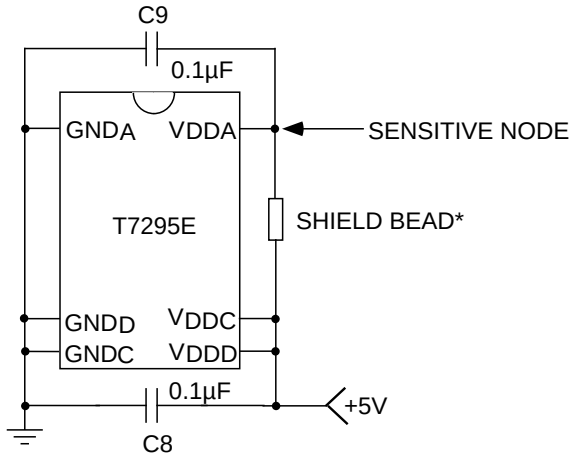
Typical values are for VDD=5.0V, 25°C, and random data. Maximum values are for VDD=5.5V at 85°C all 1s data.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Current	IDD				
REQB = 0		-	82	106	mA
REQB = 1		-	79	103	mA

BOARD LAYOUT CONSIDERATIONS

Power Supply Bypassing

Figure 8 illustrates the recommended power supply bypassing network. A 0.1 µF capacitor bypasses the digital supplies. The analog supply VDDA is bypassed by using a 0.1 µF capacitor and a shield bead that removes significant amounts of high-frequency noise generated by the system and by the device logic. Good quality, high-frequency (low lead inductance) capacitors should be used. Finally, it is most important that all ground connections be made to a low-impedance ground plane.



**Recommended shield beads are the Fair-Rite 2643000101 or the Fair-Rite 2743019446 (surface mount).*

Figure 8. Recommended Power Supply Bypassing Network

Receive Input

The connections to the receive input pin, RIN, must be carefully considered. Noise-coupling must be minimized along the path from the signal entering the board to the input pin. Any noise coupled into the XR-T7295E input directly degrades the signal-to-noise ratio of the input signal.

PLL Filter Capacitor

The PLL filter capacitor between pins LPF1 and LPF2 must be placed as close to the chip as possible. The LPF1 and LPF2 pins are adjacent, allowing for short lead lengths with no crossover's to the external capacitor. Noise-coupling into the LPF1 and LPF2 pins may degrade PLL performance.

HANDLING PRECAUTIONS

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting.

COMPLIANCE SPECIFICATIONS

Compliance with *CCITT Recommendations G.703,* G.775 *and G.824,* 1988.

LOGIC INTERFACE CHARACTERISTICS -40°C ≤TA ≤+85°C, VDD = 5V±10%

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Input Voltage					
Low	VIL	-	GNDD	0.5	V
High	VIH		VDDD -0.5	VDDD	V
Output Voltage					
Low	VOL	-5.0mA	GNDD	0.4	V
High	VOH	5.0mA	VDDD -0.5	VDDD	V
Input Capacitance	CI	-		10	pF
Load Capacitance	CL	--		10	pF
Input Leakage	IL	-0.5 to VDD + 0.5V (all input pins except 2 and 17)	-10	+10	µA
		0 V (pin 17)	0.02	0.5	mA
		VDD (pin 2)	10	100	µA
		GND (Pin 2)	-50	-5	µA

Table 6. Logic Interface Characteristic

TIMING CHARACTERISTICS All timing characteristics are measured with 10pF loading, -40°C ≤TA ≤+85°C, VDD = 5V±10%

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
tRCH1RCH2	Clock Rise Time (10% - 90%)	-	-	3.5	ns
tRCL2RCL1	Clock Fall Time (10% - 90%)	-	-	2.5	ns
tRDVRCL	Receive Data Set-up Time	5.5	-	-	ns
tRCLRDX	Receive Data Hold Time	8.5	-	-	ns
tRCHRDV	Receive Propagation Delay (See note 1)	0.6	-	3.7	ns
-	Clock Duty Cycle	45	50	55	%

Note 1: *The total delay from RIN tot he digital outputs RPDATA and RNDATA is three RCLK clocks.*

Table 7. System Interface Timing Characteristics (See Figure 9)

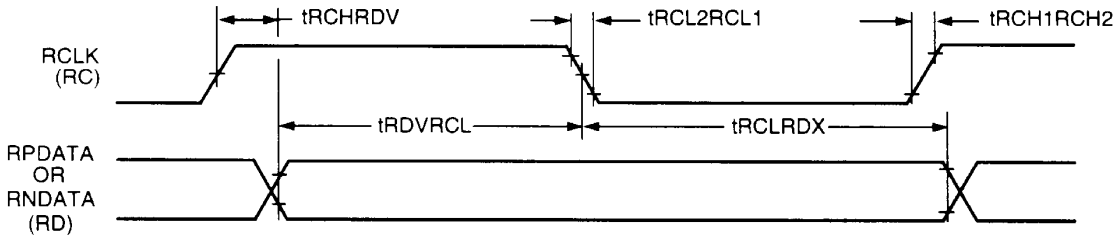


Figure 9. Timing Diagram for System Interface

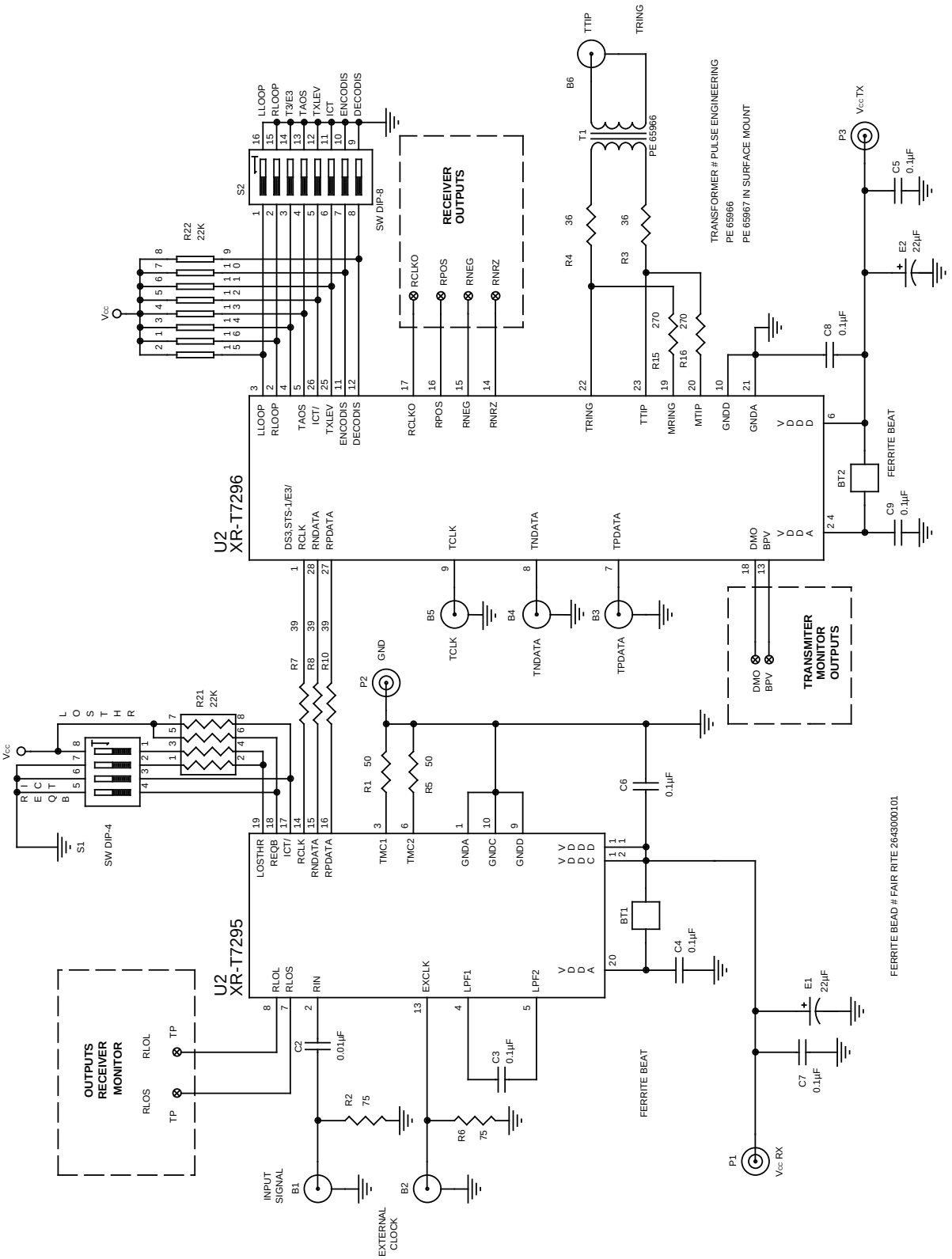


Figure 10. Evaluation System Schematic

NOTES

NOTES