...the analog plus company™

XR-T66L100 DEMO BOARD

USER MANUAL

Rev. 1.00

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TABLE OF CONTENTS

1.00 INTRODUCTION TO CALLER ID

The Caller ID feature is an on-hook capability which provides the user with information about the caller before actually answering the call. The information displayed is a data message sent from the central office to the CPE using simplex VDI-1 (Voice band Digital Interface) during the silent interval and after the first 20Hz ringing burst. The data contains the date (month and day), time (hour and minutes), and calling party number information in one of three forms:

a) 2 to 10 digit extension
b) privacy indication for those calling parties which do not want their number displayed
c) out-of-area indication if the calling number can not be recovered for an on-screen display

VDI-1 is specified in terms of three architectural layers (physical, datalink and presentation layers). The XR-T66L100 is primarily concerned with the physical layer interface requirements, which refers to the electrical and procedural characteristics that the CO uses to physically connect to the CPE. It is concerned solely with transmitting a stream of bits, without regard to meaning or structure. The data link layer provides the procedural characteristics that allow the CO to transfer complete units of information to the CPE and the presentation layer defines the general content and syntax needed to transmit recognizable information.

2.00 XR-T66L100ES DEMOBOARD

The XR-T66L100ES demoboard is intended to facilitate and speed up the evaluation procedure of the XR-T66L100 device. The demoboard requires a single 5V power supply connected to VCC and GND and a test ring signal and/or FSK signal generator connected to TIP and RING. The XR-T66L100 device is a pin compatible version of its 5V predecessor, the XR-T66100. The XR-T66L100ES demoboard is actually a modified XR-T66100ES board which allows for 3.3V operation. A voltage regulator was added to the board to provide 2.97V to the XR-T66L100 device. This voltage, factory set via an added potentiometer, is the lower limit of the V_{CC} tolerance spec (3.3V +/- 10%) in the data sheet. Supply voltage to the XR-T66L100 may be manually adjusted via the pot over a range of 2.45V to 3.8V. The addition of the regulator allows continued operation of the MAX204 RS-232 transceiver IC at +5V.

Resistor and capacitor value changes were made in the network interface circuitry between the Tip and Ring pins of the XR-T66L100 and the RJ-11 jacks. The change results in 1dB of attenuation and will allow evaluation of the device with a signal strength of -37dB (-36dB at the jacks).

Specific changes to the XR-T66100ES board are:
(Reference Figure 15 on page 23).

1) addition of R100, R101, R102, C100, LM317.
2) value change of R6 and R7 from 10K to 1K, value change of C1 and C2 from 4.7nF, 400V to 22nF, 250V.
3) N1 removed with the addition of LM317.

3.00 MESSAGE FORMAT

Caller ID information is sent to the CPE in the silent interval after the first ringing phase. The central office waits half a second after the ringing before starting transmission of the data, and completes the transmission half a second prior to the next ringing signal.

FSK data is sent to the CPE as a single or multiple message format (see Figure 2 & 3). All caller ID messages are preceded by a 250msec channel seizure sequence (01010101 pattern). This signal is sent at the beginning of each message to alert the CPE of the coming information. This is then followed by a 150msec of ones (1200Hz), intended to aid in “conditioning” the receiver for data. The message begins with the message type in one byte sequence (see Figure 2). After that, a message length or data word count value of 9 through 18 specifies the number of data words that are going to be transmitted following this word. This number does not include the check sum word which follows the last data word.

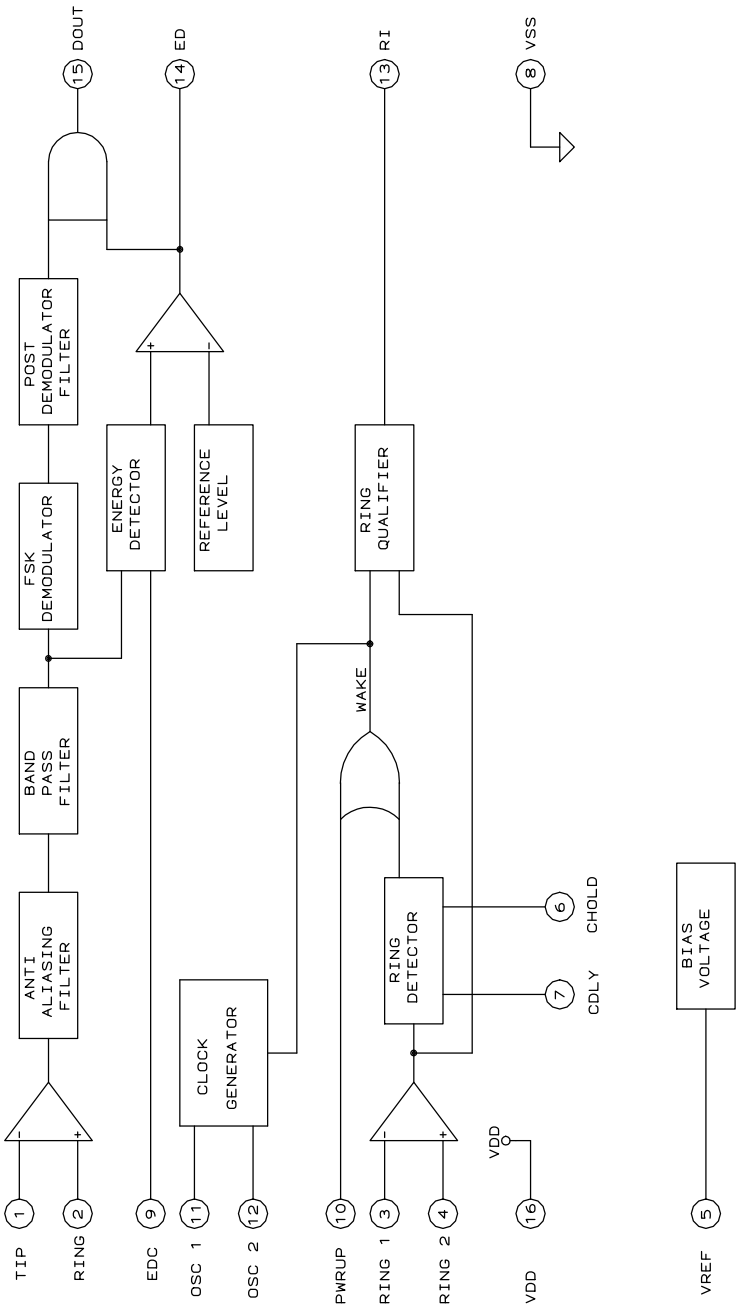

Figure 1. Functional Block Diagram

WORD #	Signification	Binary Contents 7 6 5 4 3 2 1 0	Description	Dec. Value	Hex Value	Mod. 256 in Hex
1	Msg. Type	0 0 0 0 0 1 0 0	CND *(See Note 1)*	04	04	04
2	Length	0 0 0 1 0 0 1 0	18	18	12	16
3	Month	0 0 1 1 0 0 0 0	0	48	30	46
4		0 0 1 1 0 1 0 0	4	52	34	7A
5	Day	0 0 1 1 0 0 1 0	2	50	32	AC
6		0 0 1 1 1 0 0 0	8	56	38	E4
7	Hour	0 0 1 1 0 0 0 1	1	49	31	15
8		0 0 1 1 0 0 1 1	3	51	33	48
9	Minutes	0 0 1 1 0 0 1 0	2	50	32	7A
10		0 0 1 1 0 0 0 0	0	48	30	AA
11	Calling	0 0 1 1 0 1 0 0	4	52	34	DE
12	Number	0 0 1 1 0 0 0 0	0	48	30	OE
13		0 0 1 1 1 0 0 0	8	56	38	46
14		0 0 1 1 0 1 0 0	4	52	34	7A
15		0 0 1 1 0 0 1 1	3	51	33	AD
16		0 0 1 1 0 1 0 0	4	52	34	E1
17		0 0 1 1 0 1 1 0	6	54	36	17
18		0 0 1 1 0 1 0 0	4	52	34	4B
19		0 0 1 1 0 0 0 0	0	48	30	7B
20		0 0 1 1 0 0 0 0	0	48	30	AB
21	Checksum	0 1 0 1 0 1 0 1	Checksum *(See Note 2)*	85	55	55

Note 1: *CND = Calling Number Delivery*
Note 2: *Calculated Checksum + Received Checksum = 0 AB + 55 = 0 Mod 256*

Table 1. Example of Caller Identification Coding

Caller ID information bits are grouped into 8-bit characters preceded by a start bit (logical 0) and followed by a stop bit (logical 1). Data words are sent as ASCII characters without parity. The first eight words of data contain date (month and day) and local time (hour and minutes) two characters each. Word 11 through 20 carries the calling party information. The calling party information can be a 2 to 10 digit number or an ASCII alpha character indicating “P” for privacy or “O” for out of area. The last byte is a check sum word which is used by the CPE to insure the integrity of the received data. The check sum word consists of 2’s complement of the modulo-256 sum of all the words transmitted from the CO including the message type, message length and data words. The CPE then derives the sum and adds this to the check sum. Any result other than zero indicates that the information was not received correctly. (see Table 1)

Multiple data message formats include additional parameter information. Each parameter is a series of data words specifying parameter type, parameter length and parameter data as described in Figure 3.

4.00 XR-T66L100 DESCRIPTION

Input Section

On the receive side, the received signal coming from TIP and RING first goes through a differential to single ended op-amp with a 3dB roll-off frequency around 32kHz and an input impedance of 100kΩ. After the differential op-amp, the signal goes through a Sallen - Key antialiasing filter which reinforces the low-pass characteristics of the differential op-amp and minimizes the aliasing effects. This allows the main filter to be clocked at a lower frequency with resulting smaller capacitor ratios. This filter is intended to band limit the receive energy and improve the signal to noise ratio of the receiver.

The next section is a band-pass filter composed of a fifth order high-pass followed by a third order low-pass filter. The low-pass and high-pass cuttoff frequencies are 150Hz and 3.5kHz respectively (see Figure 4).

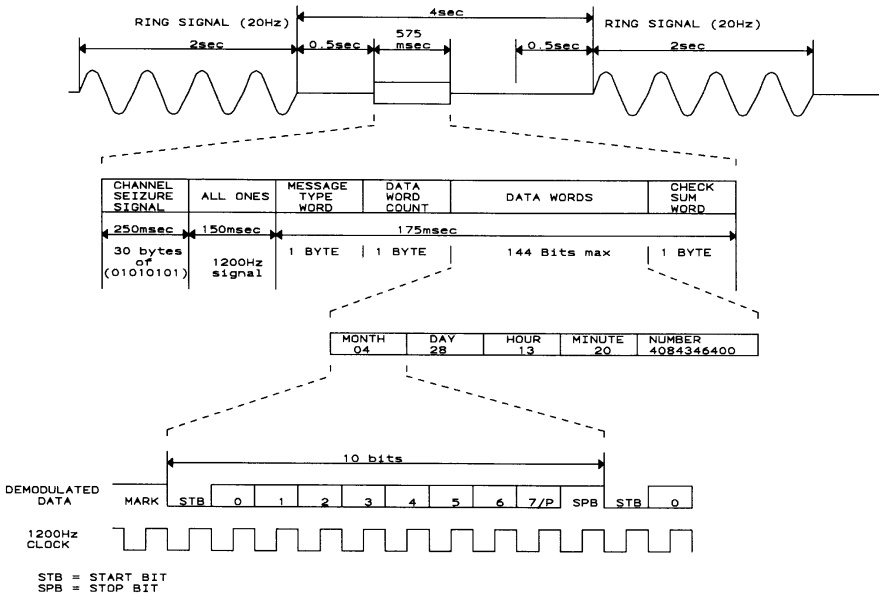

Figure 2. Single Data Message Format

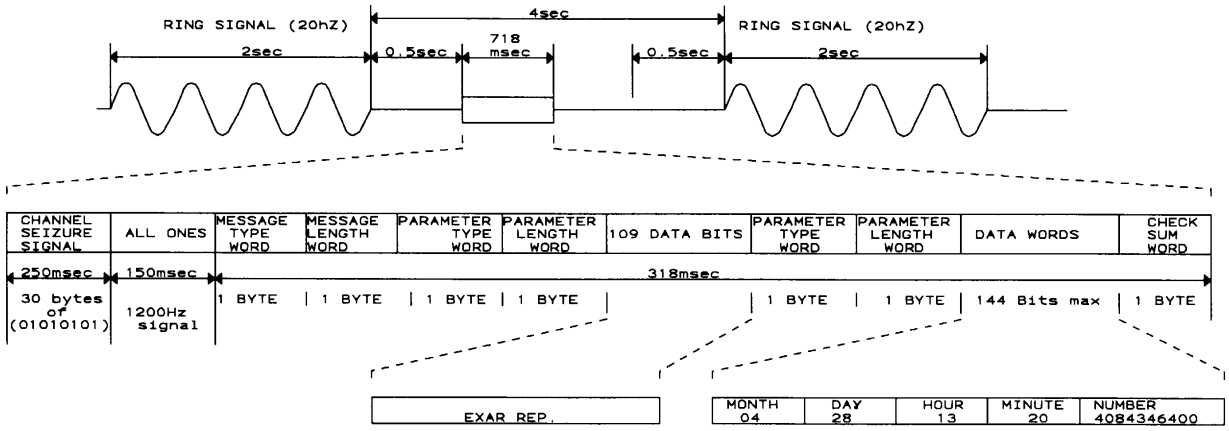

Figure 3. Multiple Data Mesage Format

After the bandpass filter, the signal is fed to a smoothing filter which attenuates the sampling frequency by 20dB and produces a smooth and filtered FSK output, which is fed to the demodulator and energy detector. The purpose of the receive filtering is to reject out of band noise so that the filtered signal can be demodulated` with resulting low bit error rate. All filters were also designed to minimize group delay and distortion between mark and space frequencies.

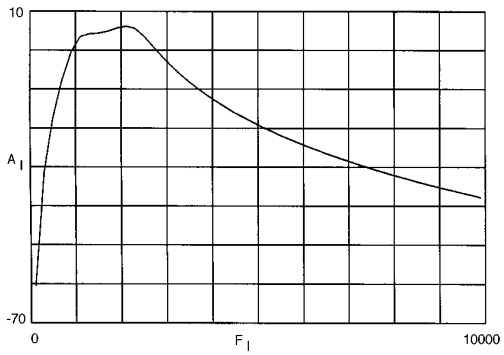

Figure 4. Bandpass Filter Response

The next section is the demodulator which is the most important part of the receiver. The filtered input signal from the band-pass filter is fed into a programmable pulsewidth converter whose function is to generate 2 sequential pulses at 4 times the center frequency of the received signal. This converter is reset on each edge of the amplitude limited signal. After this, the signal is fed through a base-band filter stage to filter out the x4 frequency component while passing the base-band information. A slicer is then used to recover the digital information.

The demodulation of the FSK signals are done according to Bell 202A specifications which are:

Link Type:	Simplex
Modulation Scheme:	Phase Coherent Frequency Shift Keying
Logical 1 (Mark)	1200+/-12Hz
Logical 0 (Space)	2200+/-22Hz
Transmission rate:	1200 bits per second
Data:	Serial, Binary, Asynchronous
Transmission Level:	-13,5+/-1dbm into 900Ohm

or V.23 specifications which are:

Link Type:	Simplex
Modulation:	FSK
Mark (logic 1)	1300 Hz ± 1.5%
Space (logic 0)	2100 Hz ± 1.5%
Received signal level for space	The received signal levels may differ by up to 6 dB for mark and space.
Transmission Rate:	1200 baud ± 1%

A raised-cosine post-demodulation filter connected to the output of the FSK demodulator filters out all frequencies above the demodulated baud rate frequency and thus insuring a low bit error rate.

Working in parallel with the FSK demodulator is an energy detector which is used to evaluate the energy within the pass-band and indicate whether the signals have the correct frequency and amplitude contents. The energy detector consists of three major sections: the rectifier, the integrator and the comparator. The rectifier samples the signal out of the bandpass filter and either passes it through or inverts it, depending on the signal polarity. The integrator generates a peak voltage representative of the energy within the pass-band. The output of the integrator is then compared with an internally generated reference voltage (slightly higher than VREF), and the result is then passed through a delay buffer to one of the inputs of an “and” gate (see Figure 1). This gate is used in conjunction with the demodulated output and thus makes sure that the data output is correct and valid. The response time of the energy detector is set to 5msec.

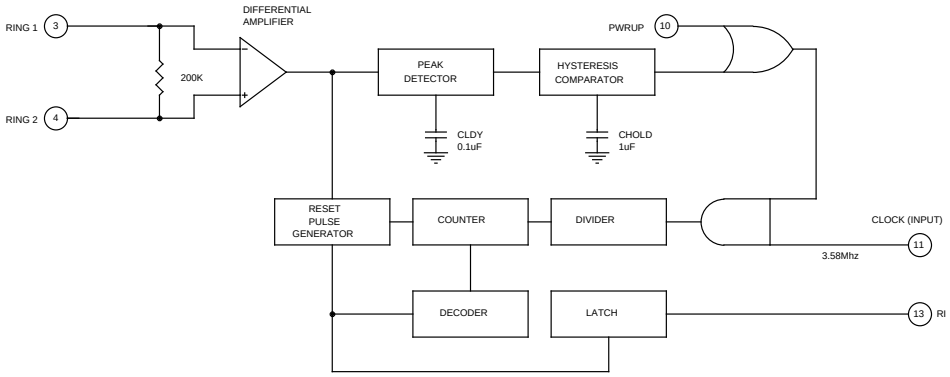

Figure 5. Ring Detect Logic

Ring Detector and Qualifier

The ring indicator circuit is an integral part of Caller ID circuit and includes a clock generator, a ring detector and a ring qualifier with a special power-up feature. The XR-T66L100 monitors the line during the on-hook condition, detects the ringing signal and informs the microcontroller of its presence with the RI output pin once the ring signal has been qualified for amplitude, delay and frequency.

The input to ring detector is a differential to single ended op-amp with high frequency roll-off characteristics in order to minimize high frequency interference. The single ended output signal is used to peak charge an external capacitor (CHOLD) which detects the energy within 1 sec of the ring signal. The peak voltage is then compared to a reference voltage (around 2.9V). The output of this comparator indicates that there is enough consecutive pulses on the ring signal and then drives an external capacitor (CDLY) with a fast charge and slow discharge time constant. The CDLY discharge time constant determines the amount of time the chip will be kept active in order to successfully recover the FSK information sent by the CO. The XR-T66L100 uses the ring signal or the power-up pin (PWR-UP) to wake up and be fully operational.

Once the ring signal has been qualified for amplitude and delay, it is qualified for frequency content before the Ring Indicator output pin is toggled. With the oscillator active, the crystal frequency is divided by 1024 and used to drive an 8 bit counter. The counter output is decoded for 51 and 233 pulses indicating the boundaries for 15Hz and 68Hz. The decoder outputs are latched and sent to a flip-flop so that only those frequencies which fall within the 15Hz to 68Hz band will generate a valid ring indicator signal output.

5.00 APPLICATION CIRCUIT (See Figure 14)
CDLY (Pin 7)

The Ring Detector response time specified by Bellcore is 0.2 sec to 2.2 sec. The XR-T66L100 response time is adjustable through the CDLY (pin 7) capacitor/resistor combination. With a 0.1uF capacitor, the response time is approximately 600msec, and this includes 3 valid ring periods from the Ring Qualifier. It is possible to reduce the response time by reducing the CDLY capacitor; however, there is a minimum response time determined by the 3 ring periods. These can be calculated as 0.2sec for 16Hz and 0.044sec for 68Hz. Internal to pin 6 is a leakage path of approximately 10MOhm (It is possible to shunt the C9 capacitor with an external resistor for applications that need a faster discharge time constant).

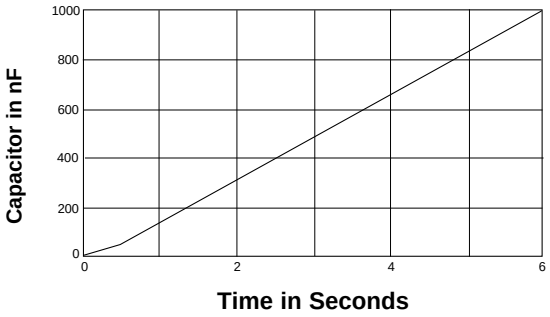

Figure 6. CDLY Response Time

Note: *For applications which do not require the Ring Detector logic, the XR-T66L100 can be powered up externally with a pull-up PNP transistor and made fully operational and ready to receive FSK data after 15msec. This may be advantageous for applications requiring low power down current since the XR-T66L100 will not be activated until the external ring voltage is detected.*

6.00 CHOLD (PIN 6)

The CHOLD capacitor determines the time it takes for the oscillator signal to die off. Internally there is a built in discharge path of approximately 10MOhm. The discharge time can be approximated as:

τ = 10MOhm * C10

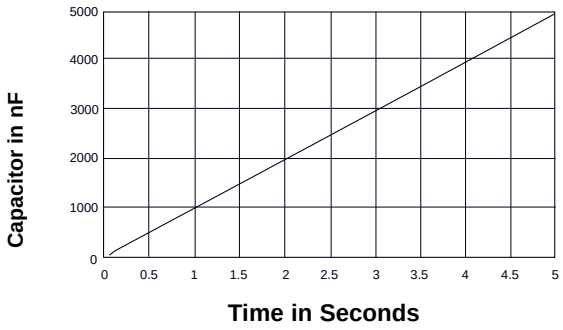

Figure 7. CHOLD Response Time

7.00 OSC1 & OSC2 (pins 11 & 12)

The Oscillator (pin 11 & 12) can be excited by crystal or ceramic resonator with a resonating frequency of 3.58MHz. The crystal should be a parallel resonant crystal such as commonly used for color burst applications. The capacitors used to adjust and load the resonator (C7 and C8) are commonly 20pF but may vary depending on the manufactures specifications.

8.00 TIP/RING (pins 1 & 2)

The input section connects to TIP and RING through C1 and C2 which are typically high voltage capacitors in order to achieve the high voltage isolation required by the network. The minimum voltage requirements are different from country to country and depends on the safety regulations imposed by the safety agencies of that country.

To design the line interface between the DAA (Data Access Arrangement), and to the inputs TIP, RING, RING1 and RING2, three compromises have to be considered, termination impedance when the Caller Identification System is on hook, recovering the data while the system is still on hook and detecting the ring signal.

Termination Impedance

The termination impedance should be very high. This is due to the fact that the central office will monitor the DC current into the line to determine if the customer premise equipment is off hook. The AC impedance needs to be high as well so that the ringing signal is not loaded, thereby allowing other equipment on the same line to see the ringing signal.

Table 2 shows the EIA/FCC requirements for impedance. Figure 8 shows the equivalent circuit seen from the central office.

Function	Frequency	State	Volt	Standard	Limits (Ohms)
DC Res.	N/A	Quiescent	<100V DC	EIA-470	>70 M
AC Imp.	<200Hz	Quiescent	<10V RMS	EIA-470	>7 K
AC Imp.	687-1633Hz	Quiescent	<3 V RMS	EIA-470	>100 K
AC Imp.	15.3-68 Hz	Active	40-150 VRMS	FCC-68	>8 K

Table. 2

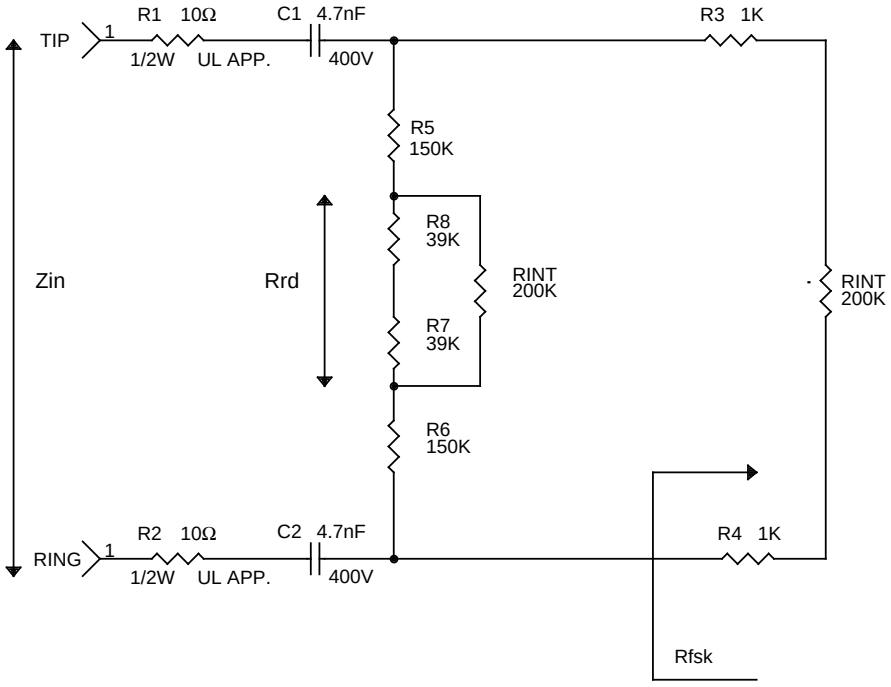

Figure 8. Impedance Equivalent Circuit

The equations to calculate the impedance are as follows:

$$R_{fsk} = R_3 + R_{int} + R_4$$

$$R_{rd} = \frac{(R_7 + R_8) \bullet R_{int}}{(R_7 + R_8 + R_{int})}$$

$$X_{in} = \frac{1}{\omega \bullet C_1} + \frac{1}{\omega \bullet C_2}$$

$$R_{in} = R_1 + R_2 + \left(\frac{R_{fsk} \bullet (R_5 + R_{rd} + R_6)}{(R_{fsk} + R_5 + R_6 + R_{rd})} \right)$$

$$|Z_{IN}| = \sqrt{(X_{in})^2 + (R_{in})^2}$$

Figure 9 (a) and (b), show this impedance (using the components of application schematic) plotted over frequency.

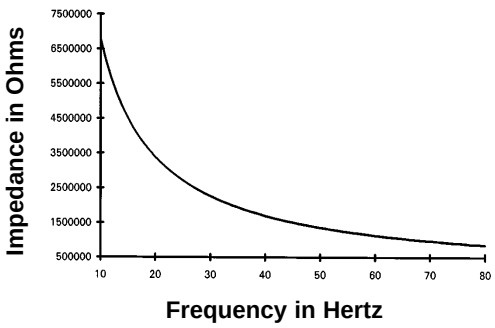

Figure 9 (a). Impedance vs Frequency

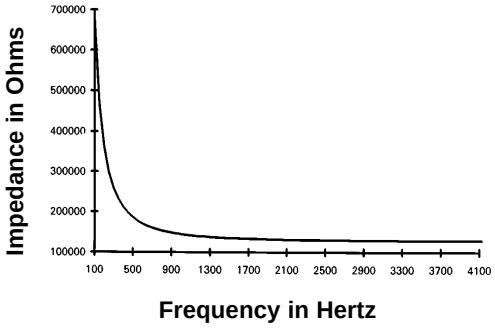

Figure 9 (b). Impedance vs Frequency

Recovery of the FSK or Data Stream

The challenge here is to build the interface circuitry with the minimum attenuation of the signal but keep the input impedance as high as possible.

The equation to calculate the attenuation in decibel is as follows:

$$R_{fsk} = R_3 + R_{int} + R_4$$

$$R_{rd} = \frac{(R_7 + R_8) \bullet R_{int}}{(R_7 + R_8 + R_{int})}$$

$$X_{in} = \frac{1}{\omega \bullet C_1} + \frac{1}{\omega \bullet C_2}$$

$$R_{in} = R_1 + R_2 + \left(\frac{R_{fsk} \bullet (R_5 + R_{rd} + R_6)}{(R_{fsk} + R_5 + R_6 + R_{rd})} \right)$$

$$|Z_{IN}| = \sqrt{(X_{in})^2 + (R_{in})^2}$$

$$A_{ttn\text{ - }V_{rel}} = 20 \bullet \text{LOG } 10 \left(\frac{R_{rel}}{Z_{in}} \right)$$

$$A_{ttn\text{ - }V_{rel}\text{ - }V_{in}} = 20 \bullet \text{LOG } 10 \left(\frac{R_{int}}{R_{fsk}} \right)$$

Total FSK Attenuation = $A_{ttn\text{ - }V_{rel}} + A_{ttn\text{ - }V_{rel}\text{ - }V_{in}}$

Figure 10 shows the equivalent circuit and Figure 11 shows the plotted attenuation using the components of the typical application circuit shown in Figure 14.

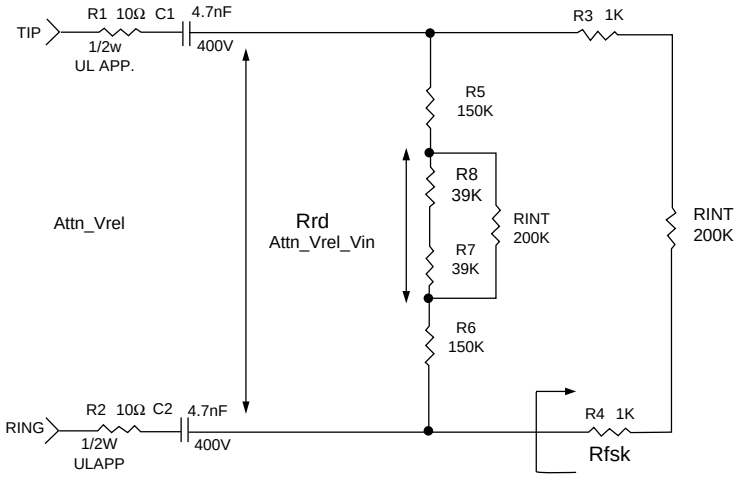

Figure 10. Equivalent Circuit for FSK Input

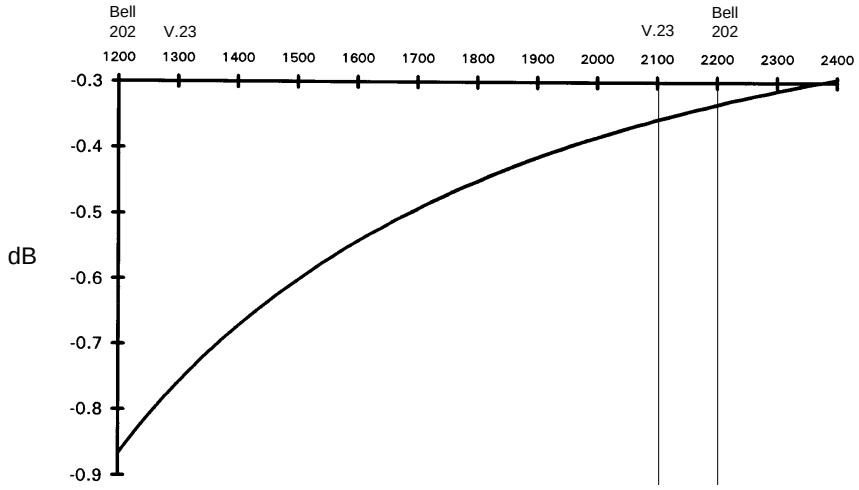

Figure 11. Plot of Attenuation in Decibel Versus Frequency

Ringing Signal Detection:

The minimum guaranteed input ringing signal is 65 V_{rms}. To detect the ringing signal, the DAA has to attenuate this signal to the minimum input level at the XR-T66L100 (Ring 1, Ring 2) which is 0.6 volt peak.

The equation to calculate the attenuation in decibel is as follows:

$$R_{fsk} = R_3 + R_{int} + R_4$$

$$R_{rd} = \frac{(R_7 + R_8) \bullet R_{int}}{(R_7 + R_8 + R_{int})}$$

$$X_{in} = \frac{1}{\omega \bullet C_1} + \frac{1}{\omega \bullet C_2}$$

$$R_{in} = R_1 + R_2 + \left(\frac{R_{fsk} \bullet (R_5 + R_{rd} + R_6)}{(R_{fsk} + R_5 + R_6 + R_{rd})} \right)$$

$$|Z_{IN}| = \sqrt{(X_{in})^2 + (R_{in})^2}$$

$$V_{in} = 65\ V_{rms} \bullet \sqrt{2 \bullet 2}$$

$$V_{rel} = \left(\frac{R_{rel}}{Z_{in}} \right) * V_{in}$$

$$V_{min-in} = \left(\frac{Rrd}{R_{rd} + R_5 + R_6} \right) \bullet V_{rel}$$

Figure 12 shows the equivalent circuit and Figure 13 shows the attenuation over frequency using the components of the typical application circuit shown in Figure 14.

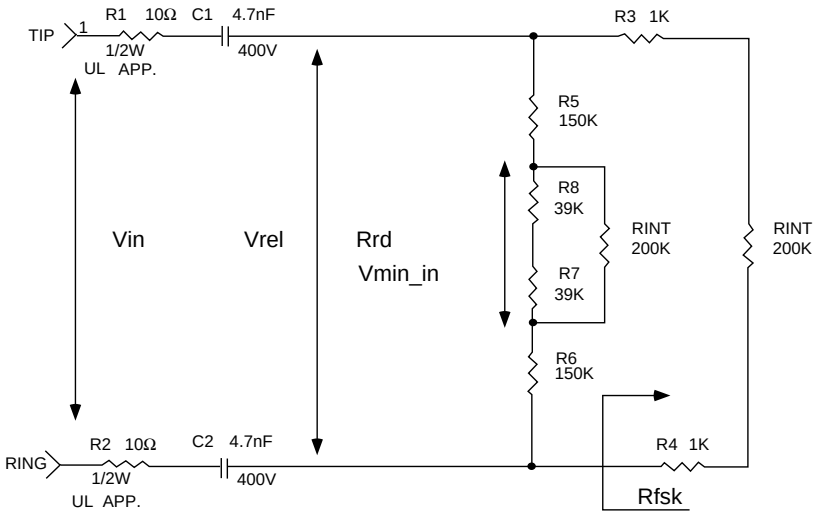

Figure 12. Equivalent Schematic for Ring Detect

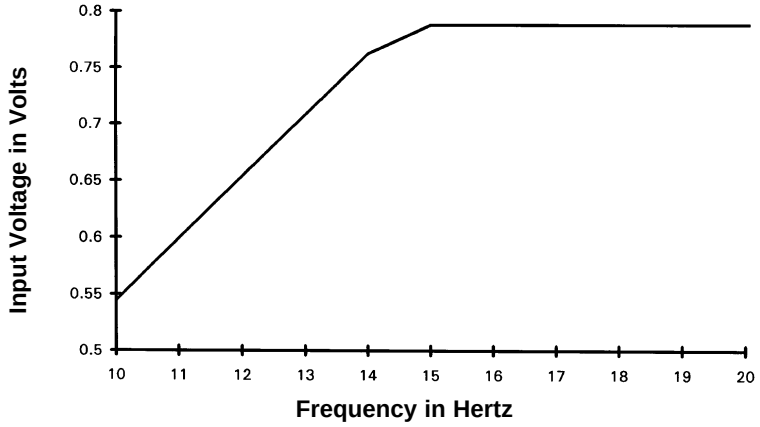

Figure 13. Ring Signal Attenuation Versus Frequency

9.00 EDC (pin 9)

The energy detector evaluates the energy within the pass-band of the band-pass filter and indicates whether the signals have the correct amplitudes and frequency contents. The response time for EDC output is typical 5msec from the time that a valid signal is present at the receive inputs. A capacitor of 0.1µF minimum is recommended to filter out the ripple on the EDC output signal.

Demoboard Schematic

The application circuit shown in Figure 15 requires more external components as opposed to the basic application circuit, but it has several advantages such as:

- Small isolation capacitors (470pF / 3KV). Small ceramic high voltage capacitors are the most economical solution for high voltage isolation.

- Higher input sensitivity (-35db). This is achieved by adding a 680 KΩ pull-up resistor to the EDC capacitor.

- Zero power down current. The minimal powerdown current of this IC is typically 15µA. To further reduce the current consumption of this device (as needed for battery powered applications), the device may need to be shut-off completely. This application circuit uses an opto-isolator in order to achieve the necessary isolation requirements and to generate a reli able noise free ring waveform. This ring signal is fed to the RING2 input for further qualification before a valid Ring Indicator signal is activated by the XR-T66L100 and used to interrupt the microprocessor.

Another function of the ring waveform is to power-up the device momentarily until the microprocessor decides to keep the device activated and ready to receive the incoming FSK data.

10.00 DEMOBOARD SETTINGS:

Loopback test (no ring signal input)

Connect the phone line and RS232 connector to the appropriate connectors of the caller ID simulator.

Set J1 and J2 to “MICRO” settings

Set J3 to DCE setting

Auto Power-up Mode (needs ring signal to wake up)

Connect the phone line from the simulator to the XR-T66L100 demoboard. Apply +3V to 5V to VCC.

Note: *Power down current should be 0mA.*

Set J1 and J2 to “SELF”

The demoboard will wake up when receiving a valid ring signal and decode the FSK signals. The data signals can be observed on the DOUT pin.

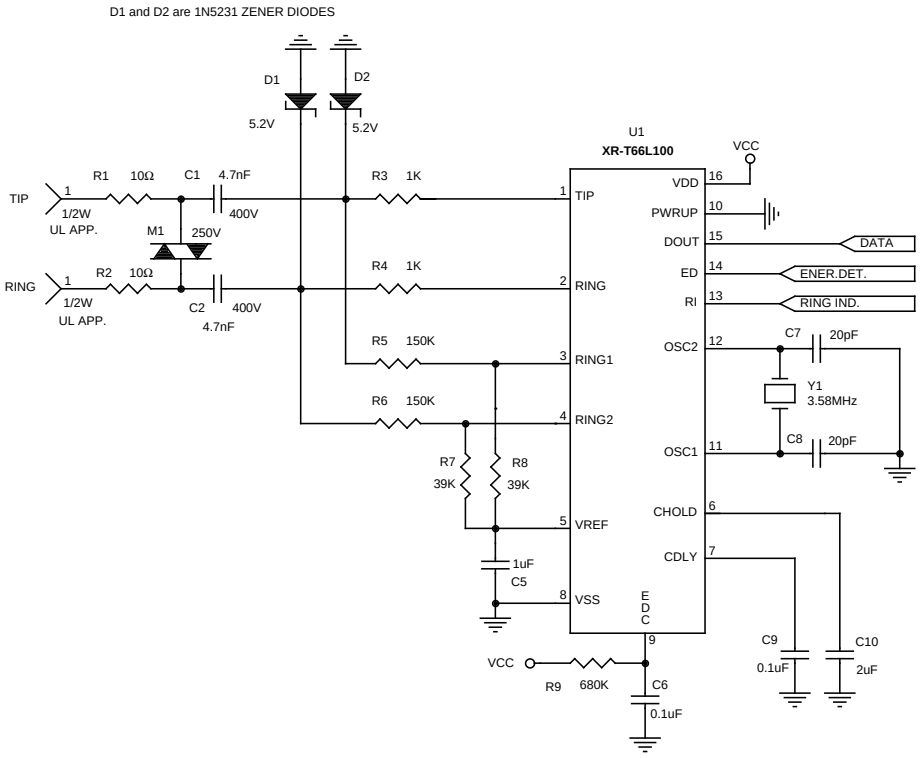

Figure 14. Typical Application

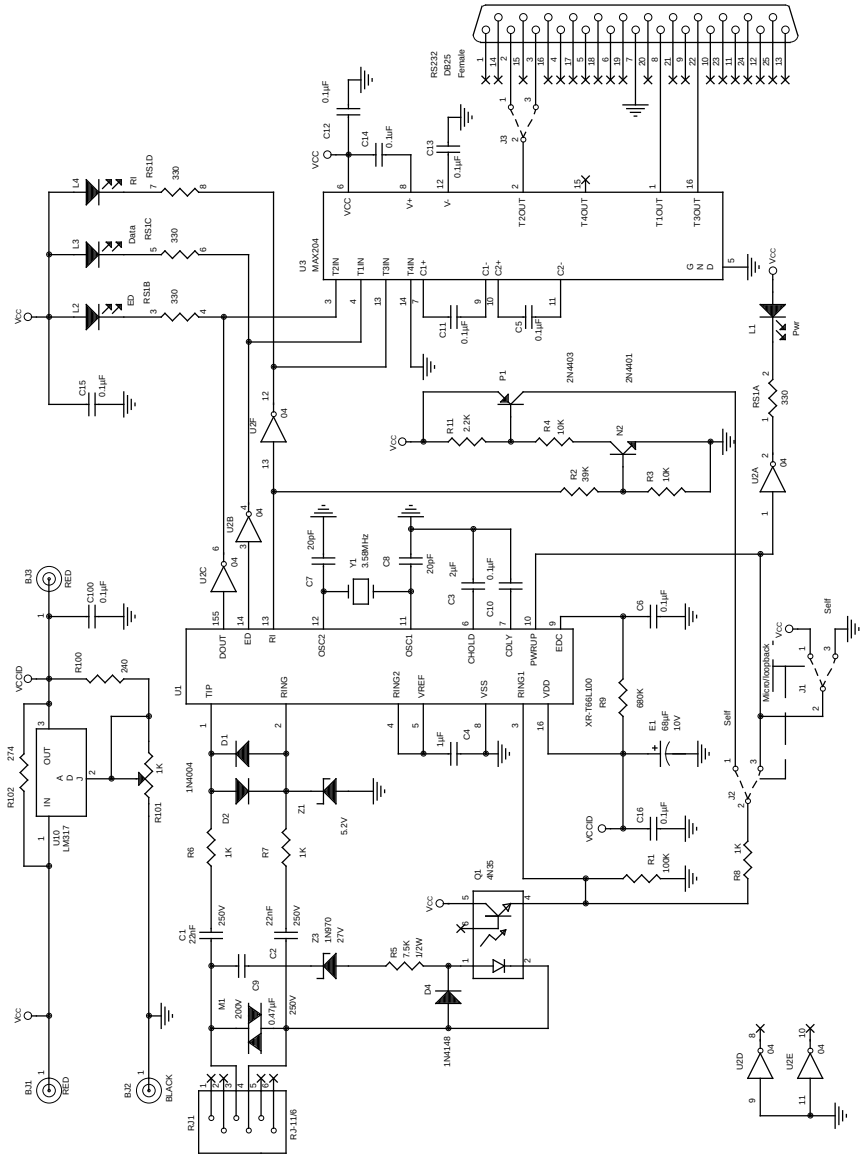

Figure 15. Demoboard Schematic

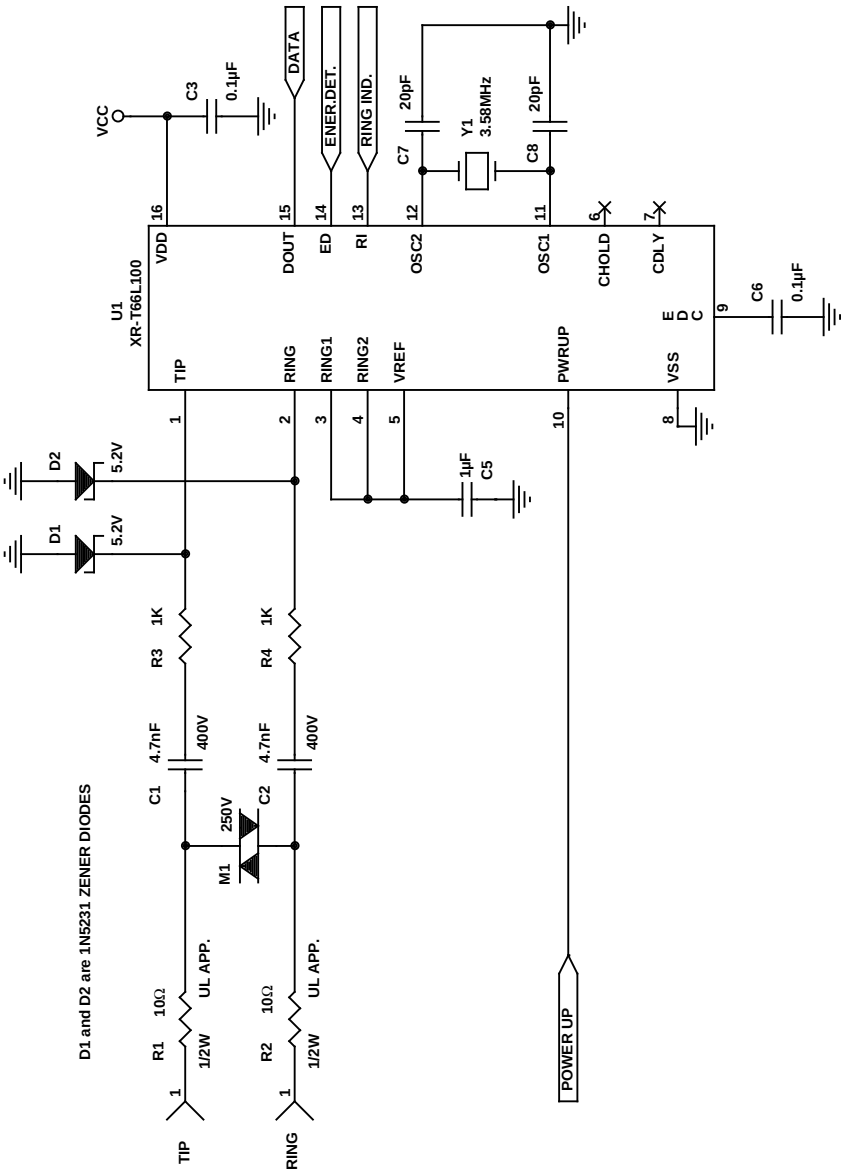

Figure 16. Typical Application without Ring Detect

Notes

Notes

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