XR-T5794

Quad E-1 Line Interface Unit

...the analog plus company™

October 1996-4

FEATURES

- Meets CCITT G.703 Pulse Mask Template for 2.048 Mbps (E1) Rates
- Transmitter and Receiver Interfaces Can Be:
  - Single Ended, 75Ω Capacitive or Transformer Coupled
  - Balanced, 100 or 120Ω Transformer Coupled
- Minimum Return Loss is 20 dB (Receive) and 18 dB (Transmit), Exceeds G.703 and ETSI 300 166 Specifications
- Bipolar Outputs Can Be Disabled Individually (High Z Outputs)
- System Interface is TTL Compatible on Digital Input and TTL/CMOS Compatible On Digital Output Pins
- Individual Channel Loss of Signal Detection, Local and Remote Digital Loopback
- Fifth Driver For Monitoring and Testing
- Low Power, CMOS Technology
- Over-temperature Protection

APPLICATIONS

- Multi-Line E1 Interface Cards
- E1 Network Equipment
  - Multiplexers
  - Cross Connects
  - Switching Systems
- Fault Tolerant Systems

GENERAL DESCRIPTION

The XR-T5794 is an optimized line interface unit, built using low power CMOS technology. The device contains four independent E1 channels for primary rate, PCM applications up to 2.048 Mbps. Each channel performs the driver and receiver functions necessary to convert bipolar signals to TTL/CMOS compatible logic levels and vice versa. The device supports single ended or balanced line interfaces on each channel, thereby providing the user an option of reducing system cost and board space by replacing the transformer with a capacitor.

Each of the four drivers can be independently disabled, allowing maximum flexibility in system power management. Output pulses are fully CCITT G.703 compliant. Moreover, the return loss is at least 18 dB over a frequency range of 51 kHz to 3.072 MHz.

The slicing circuit in the receive path is able to tolerate a maximum of 12 dB of cable loss with a minimum input sensitivity of 600 mV over the operating temperature range. Return loss on the receive interfaces is minimum 20 dB from 51 kHz to 3.072 MHz.

Local and remote loop backs can be performed on any of the four channels. A separate loss of signal (LOS) detection circuitry and a LOS pin is provided for each input. A fifth transmitter has been provided to support dedicated monitoring and testing purposes on any of the eight bipolar paths. For designers not requiring the fifth (monitor) driver, EXAR offers the XR-T5793, a pin compatible version of the XR-T5794.

The XR-T5794 is targeted for multi-line E1 line card applications where real estate, low power consumption and back-up redundancy are critical. Also, the device may be used in T1 applications (1.544 Mbps) which do not require meeting the DSX-1 cross connect pulse template.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-T5794IJ	68 Lead PLCC	-40°C to +85°C
XR-T5794IV	80 Lead SQFP (14x14x1.4 mm)	-40°C to +85°C

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ (510) 668-7017

BLOCK DIAGRAM

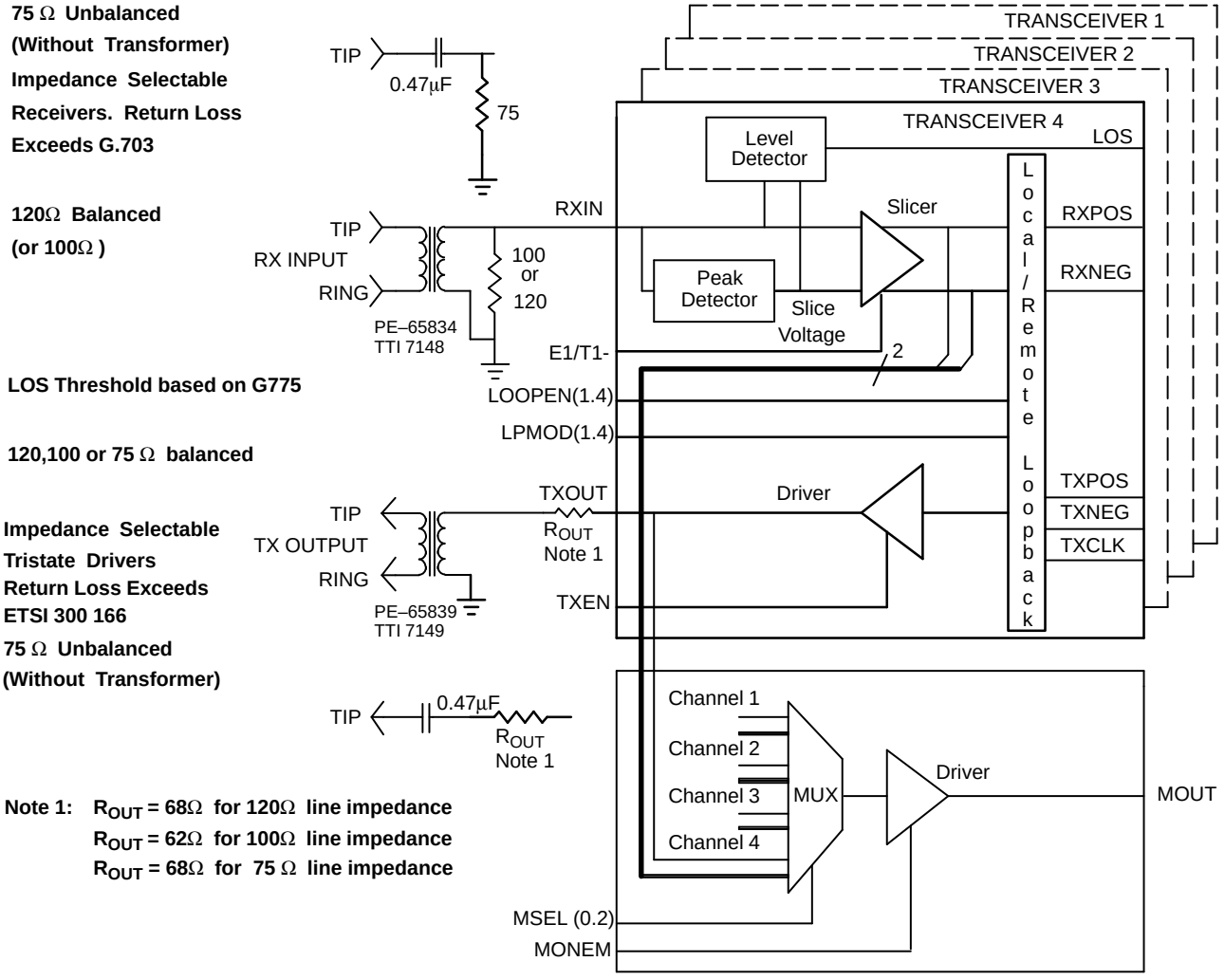
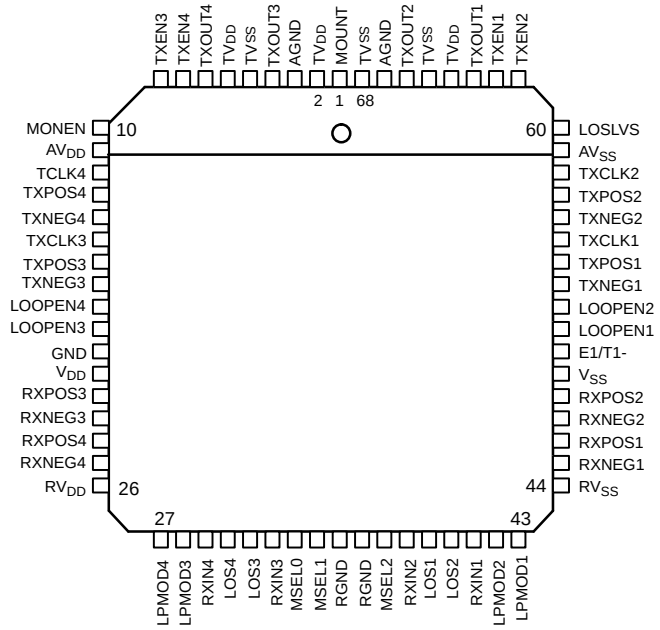
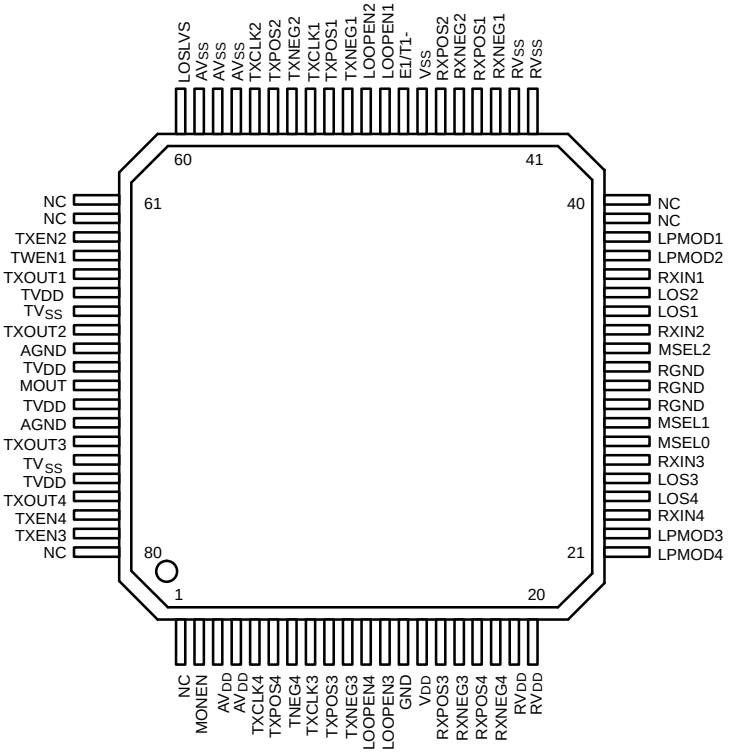


Figure 1. Block Diagram

PIN CONFIGURATION



68 Lead PLCC



80 Lead SQFP (14 x 14 x 1.4 mm)

PIN DESCRIPTION

PLCC Pin #	SQFP Pin #	Symbol	Type	Description
1	71	MOUT	O	**Signal monitor output.** If MONEN=1, this output tracks the selected signal. Hi-Z otherwise. The channel selection is done using MONSEL[2..0] inputs.
2	72	TV_{DD}	V_{DD}	**Transmit V_{DD}.** +5 V (±5%).
3	73	AGND	GND	**Analog Ground.**
4	74	TXOUT3	O	**Transmitter 3 output.** Transmitter 3 bipolar output connected to coupling capacitor or pulse transformer by a resistor.
5	75	TV_{SS}	V_{SS}	**Transmit V_{SS}.** -5 V (± 5%).
6	76	TV_{DD}	V_{DD}	**Transmit V_{DD}.** +5 V (±5%).
7	77	TXOUT4	O	**Transmitter 4 output.** Transmitter 4 bipolar output connected to coupling capacitor or pulse transformer by a resistor.
8	78	TXEN4	I	**Transmitter 4 output enable.** If driven high the transmitter 4 output drivers are enabled. Hi-Z otherwise.
9	79	TXEN3	I	**Transmitter 3 output enable.** If driven high the transmitter 3 output drivers are enabled. Hi-Z otherwise.
10	2	MONEN	I	**Monitor / test output enable.** If driven high the output driver of the MOUT output is enabled. Hi-Z otherwise.
11	3,4	AV_{DD}	V_{DD}	**Analog V_{DD}.**
12	5	TXCLK4	I	**Transmitter 4 clock input.** Apply logic one when RZ signals are supplied to data inputs.
13	6	TXPOS4	I	**Transmitter 4 positive data in.** Positive data input in NRZ or RZ format for transmitter 4.
14	7	TXNEG4	I	**Transmitter 4 negative data in.** Negative data input in NRZ or RZ format for transmitter 4.
15	8	TXCLK3	I	**Transmitter 3 clock input.** Apply logic one when RZ signals are supplied to data inputs.
16	9	TXPOS3	I	**Transmitter 3 positive data in.** Positive data input in NRZ or RZ format for transmitter 3.
17	10	TXNEG3	I	**Transmitter 3 negative data in.** Negative data input in NRZ or RZ format for transmitter 3.
18	11	LOOP-EN4	I	**Loop enable 4.** If driven high the specified loop type will be enabled for channel 4. Otherwise normal operation will continue.
19	12	LOOP-EN3	I	**Loop enable 3.** If driven high the specified loop type will be enabled for channel 3. Otherwise normal operation will continue.
20	13	GND	GND	**Digital Ground.**
21	14	V_{DD}	V_{DD}	**Digital V_{DD}.** +5 V (±5%).
22	15	RXPOS3	O	**Receiver 3 positive data out.** Positive data output in NRZ or RZ format for receiver 3.
23	16	RXNEG3	O	**Receiver 3 negative data out.** Negative data output in NRZ or RZ format for receiver 3.
24	17	RXPOS4	O	**Receiver 4 positive data out.** Positive data output in NRZ or RZ format for receiver 4.

PIN DESCRIPTION (CONT'D)

PLCC Pin #	SQFP Pin #	Symbol	Type	Description
25	18	RXNEG4	O	**Receiver 4 negative data out.** Negative data output in NRZ or RZ format for receiver 4.
26	19,20	RV_{DD}	V_{DD}	**Receive V_{DD}.** +5 V (±5%).
27	21	LPMOD4	I	**Loop mode 4.** If driven high the loop back mode of channel 4 will be set to remote loop. Otherwise the loop back mode will remain at local loop. The actual loopback will be activated when the LOOPEN4 is asserted.
28	22	LPMOD3	I	**Loop mode 3.** If driven high the loop back mode of channel 3 will be set to remote loop. Otherwise the loop back mode will remain at local loop. The actual loop back will be activated when the LOOPEN3 is asserted.
29	23	RXIN4	I	**Receiver 4 input.** Receiver 4 bipolar input connected to coupling capacitor or pulse transformer.
30	24	LOS4	O	**Receiver 4 loss of signal.** Asserted during LOS condition. Clear otherwise.
31	25	LOS3	O	**Receiver 3 loss of signal**. Asserted during LOS condition. Clear otherwise.
32	26	RXIN3	I	**Receiver 3 input.** Receiver 3 bipolar input connected to coupling capacitor or pulse transformer.
33	27	MSEL0	I	**Monitor channel select 0.** Select line, used to select a channel for monitoring using the MOUT pin based on the following assignment: MSEL2 MSEL1 MSEL0 SELECTS 0 0 0 Line 1 Receive 0 0 1 Line 2 Receive 0 1 0 Line 3 Receive 0 1 1 Line 4 Receive 1 0 0 Line 1 Transmit 1 0 1 Line 2 Transmit 1 1 0 Line 3 Transmit 1 1 1 Line 4 Transmit ***Note*** *The monitoring is only done on the NRZ data output signals from the receiver or from the transmitter line side.*
34	28	MSEL1	I	**Monitor channel select 1.** See table above.
35	29	RGND	GND	**Receive Ground.**
36	31	RGND	GND	**Receive Ground.**
37	32	MSEL2	I	**Monitor channel select 2.** See table above.
38	33	RXIN2	I	**Receiver 2 input**. Receiver 2 bipolar input connected to coupling capacitor or pulse transformer.
39	34	LOS1	O	**Receiver 1 loss of signal.** Asserted during LOS condition. Clear otherwise.
40	35	LOS2	O	**Receiver 2 loss of signal**. Asserted during LOS condition. Clear otherwise.
41	36	RXIN1	I	**Receiver 1 input**. Receiver 1 bipolar input connected to coupling capacitor or pulse transformer.
42	37	LPMOD2	I	**Loop mode 2.** If driven high the loop back mode of channel 2 will be set to remote loop. Otherwise the loop back mode will remain at local loop. The actual loopback will be activated when the LOOPEN2 is asserted.

PIN DESCRIPTION (CONT'D)

PLCC Pin #	SQFP Pin #	Symbol	Type	Description
43	38	LPMOD1	I	**Loop mode 1.** Iif driven high the loop back mode of channel 1 will be set to remote loop. Otherwise the loop back mode will remain at local loop. The actual loop back will be activated when the LOOPEN1 is asserted.
44	41,42	RV_{SS}	V_{SS}	**Receive V_{SS}.** -5 V (±5%).
45	43	RXNEG1	O	**Receiver 1 negative data out.** Negative data output in NRZ or RZ format for receiver 1.
46	44	RXPOS1	O	**Receiver 1 positive data out.** Positive data output in NRZ or RZ format for receiver 1.
47	45	RXNEG2	O	**Receiver 2 negative data out**. Negative data output in NRZ or RZ format for receiver 2.
48	46	RXPOS2	O	**Receiver 2 positive data out.** Positive data output in NRZ or RZ format for receiver 2.
49	47	V_{SS}	V_{SS}	**Digital V_{SS}.** -5 V (± 5%).
50	48	E1/T1-	I	**E1/T1- selection.** Apply logic one to select the receive data threshold appropriate for E1 operation. Connect to ground to select the T1 data threshold.
51	49	LOOP-EN1	I	**Loop enable 1.** If driven high the specified loop back mode will be enabled for channel 1. Otherwise normal operation will continue.
52	50	LOOP-EN2	I	**Loop enable 2.** If driven high the specified loop back mode will be enabled for channel 2. Otherwise normal operation will continue.
53	51	TXNEG1	I	**Transmitter 1 negative data in.** Negative data input in NRZ or RZ format for transmitter 1.
54	52	TXPOS1	I	**Transmitter 1 positive data in.** Positive data input in NRZ or RZ format for transmitter 1.
55	53	TXCLK1	I	**Transmitter 1 clock input.** Apply logic one when RZ signals are supplied to data inputs.
56	54	TXNEG2	I	**Transmitter 2 negative data in.** Negative data input in NRZ or RZ format for transmitter 2.
57	55	TXPOS2	I	**Transmitter 2 positive data in.** Positive data input in NRZ or RZ format for transmitter 2.
58	56	TXCLK2	I	**Transmitter 2 clock input.** Apply logic one when RZ signals are supplied to data inputs.
59	57,58,59	AV_{SS}	V_{SS}	**Analog V_{SS}.**
60	60	LOSLVS	I	**Loss of signal voltage select.** Apply logic one to select LOS voltage level appropriate for 120Ω balanced receiver operation. Connect to ground to choose LOS voltage for 75Ω unbalanced operation.
61	63	TXEN2	I	**Transmitter 2 output enable.** If asserted the transmitter 2 output drivers are enabled. High-Z otherwise.
62	64	TXEN1	I	**Transmitter 1 output enable.** If asserted the transmitter 1 output drivers are enabled. High-Z otherwise.
63	65	TXOUT1	O	**Transmitter 1 output.** Transmitter 1 bipolar output connected to coupling capacitor or pulse transformer through a resistor.
64	66	TV_{DD}	V_{DD}	**Transmit V_{DD}.** +5 V (±5%).
65	67	TV_{SS}	V_{SS}	**Transmit V_{SS}.** +5 V (±5%).

PIN DESCRIPTION (CONT'D)

PLCC Pin #	SQFP Pin #	Symbol	Type	Description
66	68	TXOUT2	O	**Transmitter 2 output.** Transmitter 2 bipolar output connected to coupling capacitor or pulse transformer through a resistor.
67	69	AGND	GND	**Analog Ground.**
68	70	TV_{SS}	V_{SS}	**Transmit V_{DD}.** +5 V (±5%).
-	30	RGND	GND	**Receive Ground.**
-	1,39,40, 61,62,80	NC	-	**Not Connected.**

RETURN LOSS REQUIREMENTS

Transmit Interface	75Ω		100Ω		120Ω		Units
	Min.	Typ.	Min.	Typ.	Min.	Typ.	
51kHz to 102 kHz	18	22	18	22	18	22	dB
102 kHz to 2.048 MHz	18	22	18	22	18	22	dB
2.048 MHz to 3.072 MHz	18	22	18	22	18	22	dB

Receive Interface	75Ω		100Ω		120Ω		Units
	Min.	Typ.	Min.	Typ.	Min.	Typ.	
51kHz to 102 kHz	20	30	20	30	20	30	dB
102 kHz to 2.048 MHz	20	30	20	30	20	30	dB
2.048 MHz to 3.072 MHz	20	30	20	30	20	30	dB

Note

The return loss has been measured on the evaluation board coupled via a capacitor and terminated with 75Ω impedance.

Table 1. Return Loss Requirements (Resistor Tolerance: 1% On Transmit Side, 2% On Receive Side)

DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = -40 to **25** to 85°C, all V_{DD}s = **5V** ± 5%, all V_{SS}s = **-5V** ± 5%, all GNDs = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DC Parameters						
V_{DD}s	DC Supply Positive	4.75	**5.00**	5.25	V	
V_{SS}s	DC Supply Negative	-4.75	**-5.00**	-5.25	V	
Inputs						
V_{IH}	High Level Input	**2.0**			V	
V_{IL}	Low Level Input			**0.8**	V	
I_{PDC}	Input Pull Down Current			**40**	µA	
Outputs						
V_{OH}	High Level Output	3.5			V	I_{OH} = -10µA
V_{OH}	High Level Output	**2.4**			V	I_{OH} = -40µA
V_{OL}	Low Level Output			**0.4**	V	I_{OL} = 1.6mA
Receiver Specifications						
R_{XP}	Receiver Sensitivity	0.6		4.2	Vp	
R_{XCL}	Allowed Cable Loss (0dB=2.4V)	0 0	10 10	12 12	dB dB	1.024 MHz (E1) 772 kHz (T1)
R_{XIWT}	Interference Margin (E1)	16			dB	With 6dB Cable Loss
R_{XTI}	Receiver Slicing Level (T1)[1]	**60**	65	**70**	%	Peak Voltage %
R_{XEI}	Receiver Slicing Level (E1)[1]	**45**	50	**55**	%	Peak Voltage %
R_{XLOS}	Receiver LOS Threshold		0.2	**0.3**	V	
R_{IN}	Input Resistance	2.5			KΩ	Up to 3.072 MHz
Power Specifications (Without Monitor Channel)						
P_D	Power Dissipation		400	**680**	mW	
P_D	Power Dissipation		250	280	mW	All drivers in High-Z
P_C	Power Consumption 75Ω[2]		500	833	mW	All 1's transmit & receive
P_C	Power Consumption 100Ω[2]		475	860	mW	All 1's transmit & receive
P_C	Power Consumption 120Ω[2]		450	830	mW	All 1's transmit & receive
PV_{DD}	Power Supply Requirement			Pc/2+5 mW	mW	
PV_{SS}	Power Supply Requirement			Pc/2-5 mW	mW	

Notes

- Bold face parameters are covered by production test and guaranteed over operating temperature range.

[1] Selected by E1/T1

[2] Power consumption = power dissipation + power to the cable.

AC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = -40 to **25** to 85°C, all V_{DD}s = **5V** ± 5%, all V_{SS}s = **-5V** ± 5%, all GNDs = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{TXOUT}	Output Pulse Amplitude (75Ω)	**2.13**	2.37	**2.60**	V	
V_{TXOUT}	Output Pulse Amplitude (120Ω)	2.70	3.0	3.30	V	
V_{TXOUT}	Output Pulse Amplitude (100Ω)	2.3	3.0	3.7	V	
T_{XPW}	Pulse Width (2.048 MHz)	**224**	244	**264**	nS	Determined by T_X clock
T_{XPW}	Pulse Width (1.544 MHz)	274	324	374	nS	Determined by T_X clock
	Pos/Neg Pulse Imbalance	-5		5	%	
T_1	TXCLK Clock Period (E1)		488		nS	
T_2	TXCLK Clock Period (T1)		648		nS	
T_3	TXCLK Duty Cycle	48	50	52	%	
T_4	Data Setup Time, TDATA to TCLK	**50**			nS	
T_5	Data Hold Time, TCLK to TDATA	**50**			nS	
tr	Clock Rise Time			30	nS	
tf	Clock Fall Time			30	nS	
T_6	Receive Data High (E1)	**219**	244	**269**	nS	0 dB cable loss
T_7	Data Propagation Delay			**100**	nS	

Note
*- **Bold face parameters are covered by production test and guaranteed over operating temperature range.***

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Supply Voltage . . . . . ±7V

Turns Ratio	Line Impedance	R_{LOAD}
1:1	75Ω	75Ω
1:1	120Ω	120Ω
1:1	100Ω	100Ω

Table 2. Input Transformer Requirements

Turns Ratio	Line Impedance	R_{LOAD}
1:1	75Ω	68Ω
1:1.265	120Ω	68Ω
1:1.265	100Ω	62Ω

Table 3. Output Transformer Requirements

Magnetic Supplier Information:

Pulse
Telecom Product Group
P.O. Box 12235
San Diego, CA 92112
Tel. (619) 674-8100
Fax. (691) 674-8262

Transpower Technologies, Inc.
24 Highway 28, Suite 202
Crystal Bay, NV 89402–0187
Tel. (702) 831–0140
Fax. (702) 831–3521

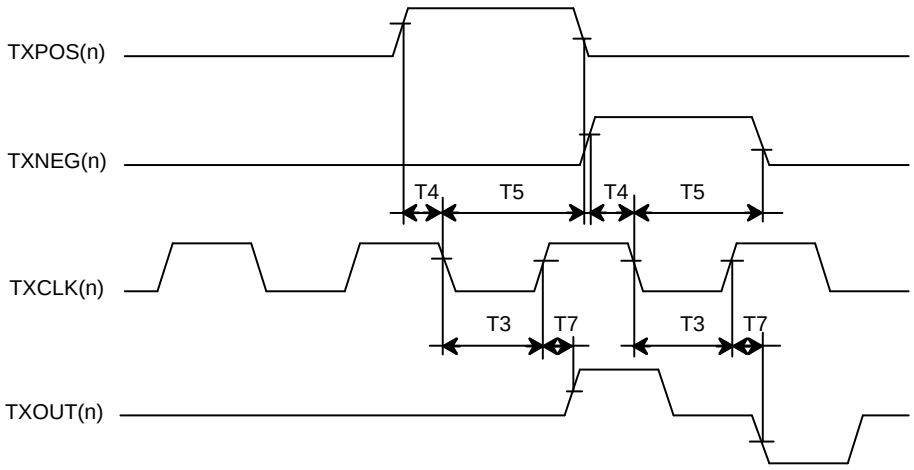


Figure 2. Transmit Timing Diagram

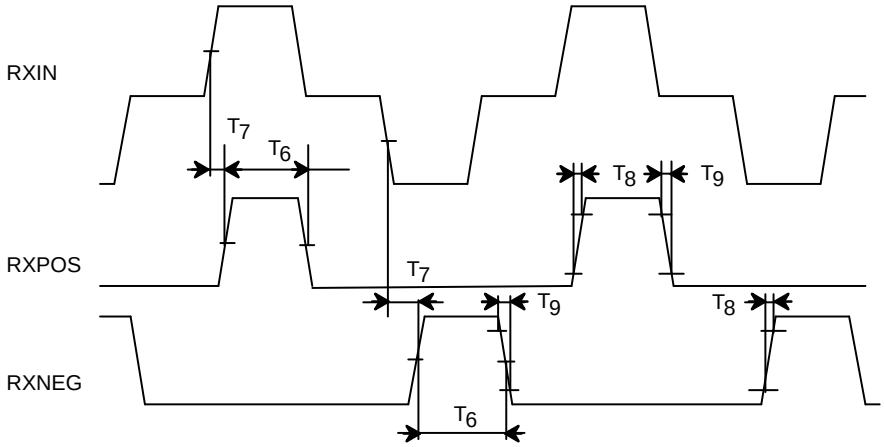


Figure 3. Receive Timing Diagram

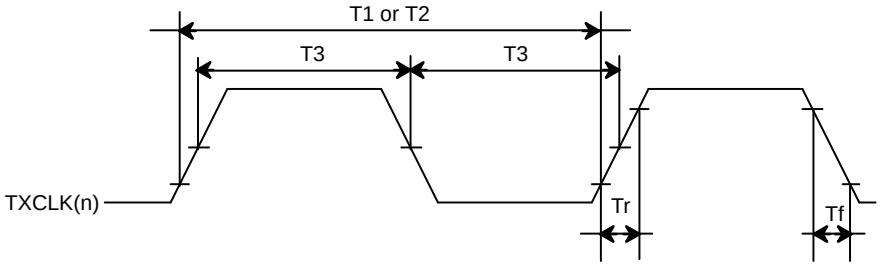


Figure 4. Transmit Clock Timing

SYSTEM DESCRIPTION

This device is a quad E1 transceiver which provides electrical interface for 2.048 Mbps applications. Its unique architecture includes four receiver circuits that convert CCITT G.703 compliant bipolar signals to TTL compatible logic levels. Likewise, in the other direction, four transmitters translate TTL compatible logic levels to G.703 compatible bipolar signals. A fifth transmitter circuit is used as a monitor output. One of the four AMI receiver inputs or transmitter outputs can be selected (via MONSEL[2..0] lines) to be monitored. The MOUT output can be disabled using the MONEN signal.

This device supports two different types of loopback functions. Each of four channels can be independently looped either in local or remote sides digitally. The remote loopback is performed between the receiver input and transmitter output. To activate the remote loopback on channel n, LOOPENn and LPMODn inputs are driven high. Local loopback on channel n, can be established similarly by driving LOOPENn high and clearing LPMODn inputs. More than one channel can be tested simultaneously.

RECEIVERS

Each of the four identical E1 line receivers will accept bipolar signals meeting the CCITT G.703 pulse mask requirements. Each input stage consists of a slicing circuitry which samples the incoming pulses at a fixed percentage of the signals maximum amplitude. The slicing voltage level is generated using a precision peak detector. The receiver section can tolerate up to 12 dB of line loss (measured at 1.024 MHz).

A loss of signal (LOS) is detected on any inputs by input fail circuitry. There is an independent LOS pin dedicated for each of the receivers. The LOS detection is based on signal energy instead of number of zeros.

A balanced signal (100 or 120Ω) must be coupled by a transformer. An unbalanced signal (75Ω) may be coupled via a capacitor or transformer coupled.

TRANSMITTERS

This device contains five identical CCITT G.703 compliant transmitters which meet the return loss requirements. Each transmitter is a single-ended voltage driver. External resistors are used to maintain an accurate source impedance that has a high return loss to the transformer or the capacitor. Each of the drivers can be individually disabled, this is required in fault tolerant applications where redundancy is a requirement. During power-down mode of operation the bipolar outputs can be disabled.

To protect the data integrity during a brownout, the output pulse amplitudes are reduced by a factor of 25% if the supply drops below an internally set limit.

Transmission is possible either with or without a clock. If a clock is used, the transmit input data must consist of full-width NRZ pulses, and the transmitter output pulse width is determined by the duty cycle of the clock. If the transmit clock is tied high, the transmitter output pulses are determined by the input data pulse width. In this mode, RZ data must be supplied to the device.

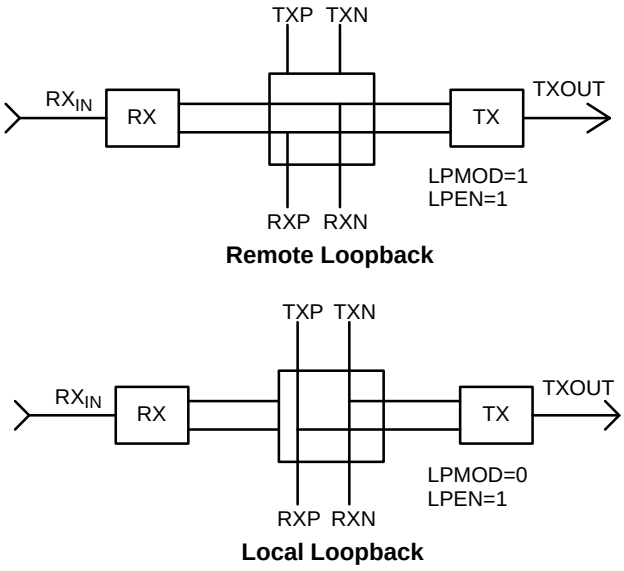


Figure 5. Loopback Configurations

Output Transformer Selection

The 1:1.265 ratio output transformer is recommended for the XR-T5794 because this ratio gives the best possible transmitter output return loss for 120Ω balanced E1 service. However, other transformers may provide an adequate return loss for many applications. The two characteristics that determine series build-out resistor requirements are:

- Driver output impedance is less than 5Ω.
- V_S, which is the driver open circuit output voltage, is 4.5 Volts peak.

The following method may be used to determine transformer suitability for a given use.

1. List the application requirements.

   Transformer Ratio = 1:n
   Vo = Peak Output Pulse Amplitude
   R_L= Load Resistance

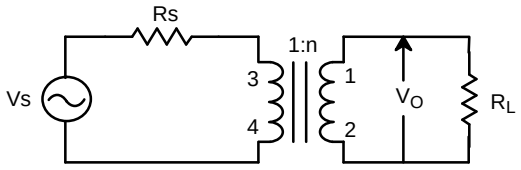


Figure 6. Equivalent Impedance Schematic

2. Calculate equivalent output voltage and load resistance without the transformer.

$$Req = \frac{R_L}{n^2} \qquad Veq = \frac{V_o}{n}$$

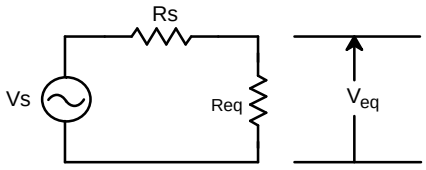


Figure 7. Equivalent Simplified Schematic

3. Calculate the source resistance, R_S.

$$Rs = Req\left(\frac{Vs}{Veq} - 1\right)$$

4. Now calculate the theoretical return loss.

$$Return\ Loss = 20\ log\left(\frac{Req + Rs}{Req - Rs}\right)$$

The calculation given below uses the recommended 1:1.265 ratio transformer as an example:
Transformer Ratio= 1 :1.265
V_O = 3.0 V Peak
R_L = 120 Ω

$$Req = \frac{R_L}{n^2} = \frac{120}{1.6} = 75\Omega$$

$$Veq = \frac{V_o}{n} = \frac{3.0}{1.265} = 2.37\ V$$

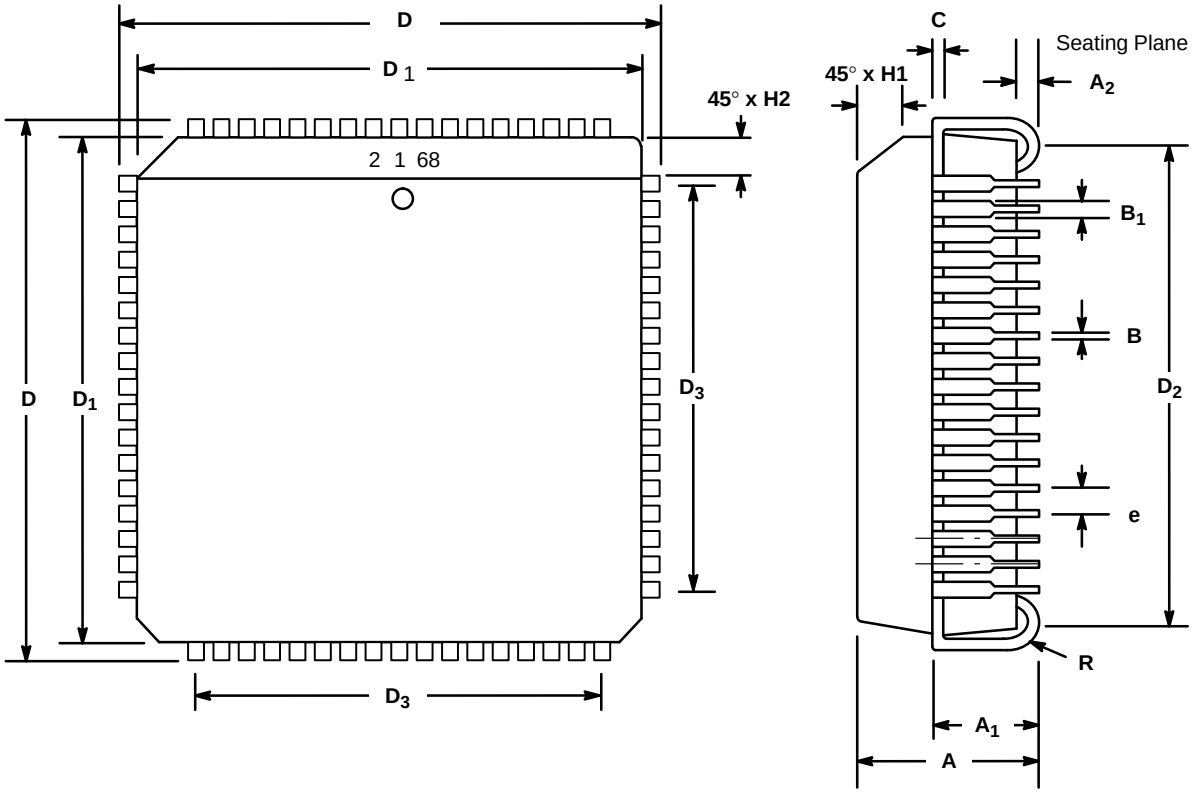
$$Rs = Req\left(\frac{Vs}{Veq} - 1\right) = 75\left(\frac{4.5}{2.37} - 1\right) = 67.4\Omega$$

(Datasheet specifies standard value of 68Ω)
Calculate the theoretical return loss to determine if the transformer is acceptable.

$$Return\ Loss = 20\ log\left(\frac{75 + 67.4}{75 - 67.4}\right) = 25.5\ dB$$

68 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)

Rev. 1.00

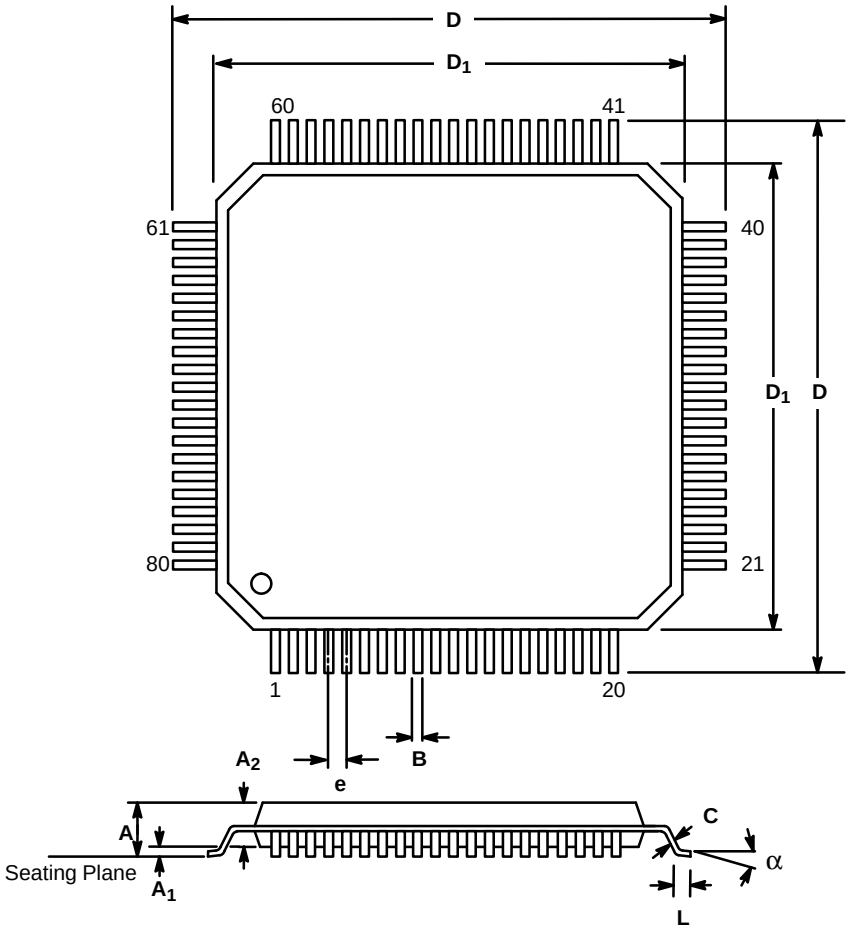


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.200	4.19	5.08
A_1	0.090	0.130	2.29	3.30
A_2	0.020	---.	0.51	---
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.985	0.995	25.02	25.27
D_1	0.950	0.958	24.13	24.33
D_2	0.890	0.930	22.61	23.62
D_3	0.800 typ.		20.32 typ.	
e	0.050 BSC		1.27 BSC	
H1	0.042	0.056	1.07	1.42
H2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

Note: The control dimension is the inch column

80 LEAD SHRINK QUAD FLAT PACK (14 x 14 x 1.4 mm, SQFP)

Rev. 1.00



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.005	0.009	0.13	0.23
C	0.004	0.008	0.09	0.20
D	0.622	0.638	15.80	16.20
D_1	0.547	0.555	13.90	14.10
e	0.0256 BSC		0.65 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Datasheet October 1996