March 1996-1

Quad E-1 Line Interface Unit

GENERAL DESCRIPTION

The XR-T5793 is an optimized line interface unit, built in low power CMOS technology, containing four independent E1 channels for primary rate, PCM applications up to 2.048 Mbps. Each channel performs the driver and receiver functions necessary to convert bipolar signals to TTL/CMOS compatible logic levels and vice versa. The device supports single ended or balanced line interfaces on each channel, thereby providing the user an option of reducing system cost and board space by replacing the transformer with a capacitor.

Each of the four drivers can be independently disabled, allowing maximum flexibility in system power management. Output pulses are fully CCITT G.703 compliant. Moreover, the return loss is at least 18 dB over a frequency range of 51 KHz to 3.072 MHz.

The slicing circuit in the receive path is able to tolerate a maximum of 12 dB of cable loss with a minimum input sensitivity of 600 mV over the operating temperature range. Return loss on the receive interfaces is minimum 20 dB from 51 KHz to 3.072 MHz.

Local and remote loopbacks can be performed on any of the four channels. A separate loss of signal (LOS) detection circuitry and a LOS pin is provided for each input.

The XR-T5793 is targeted for multi-line E1 line card applications where real estate and low power consumption are critical. Also, the device may be used in T1 applications (1.544 Mbps) which do not require meeting the DSX-1 cross connect pulse template. The XR-T5793 is pin compatible with the XR-T5794, which supports a fifth channel. The fifth channel is for redundancy and dedicated monitoring on any of the eight bipolar paths.

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5793IJ	68 Pin PLCC	-40°C to +85°C
XR-T5793IV	80 Pin SQFP	-40°C to +85°C

FEATURES

Meets CCITT G.703 pulse mask template for 2.048 Mbps (E1) rates

Transmitter and receiver interfaces can be:

- Single ended, 75 Ohm capacitive or transformer coupled
- Balanced, 100 or 120 Ohm transformer coupled

Minimum return loss is 20 dB (receive) and 18 dB (transmit), exceeds G.703 and ETSI 300 166 specifications

Bipolar outputs can be disabled individually (High Z outputs)

System interface is TTL compatible on digital input and TTL/CMOS compatible on digital output pins

Individual channel loss of signal detection, local and remote digital loopback

Low power, CMOS technology

Over-temperature protection

APPLICATION

Multi-line E1 interface cards

E1 network equipment
- Multiplexers
- Cross connects
- Switching systems

Fault tolerant systems

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Supply Voltage	+/-7V

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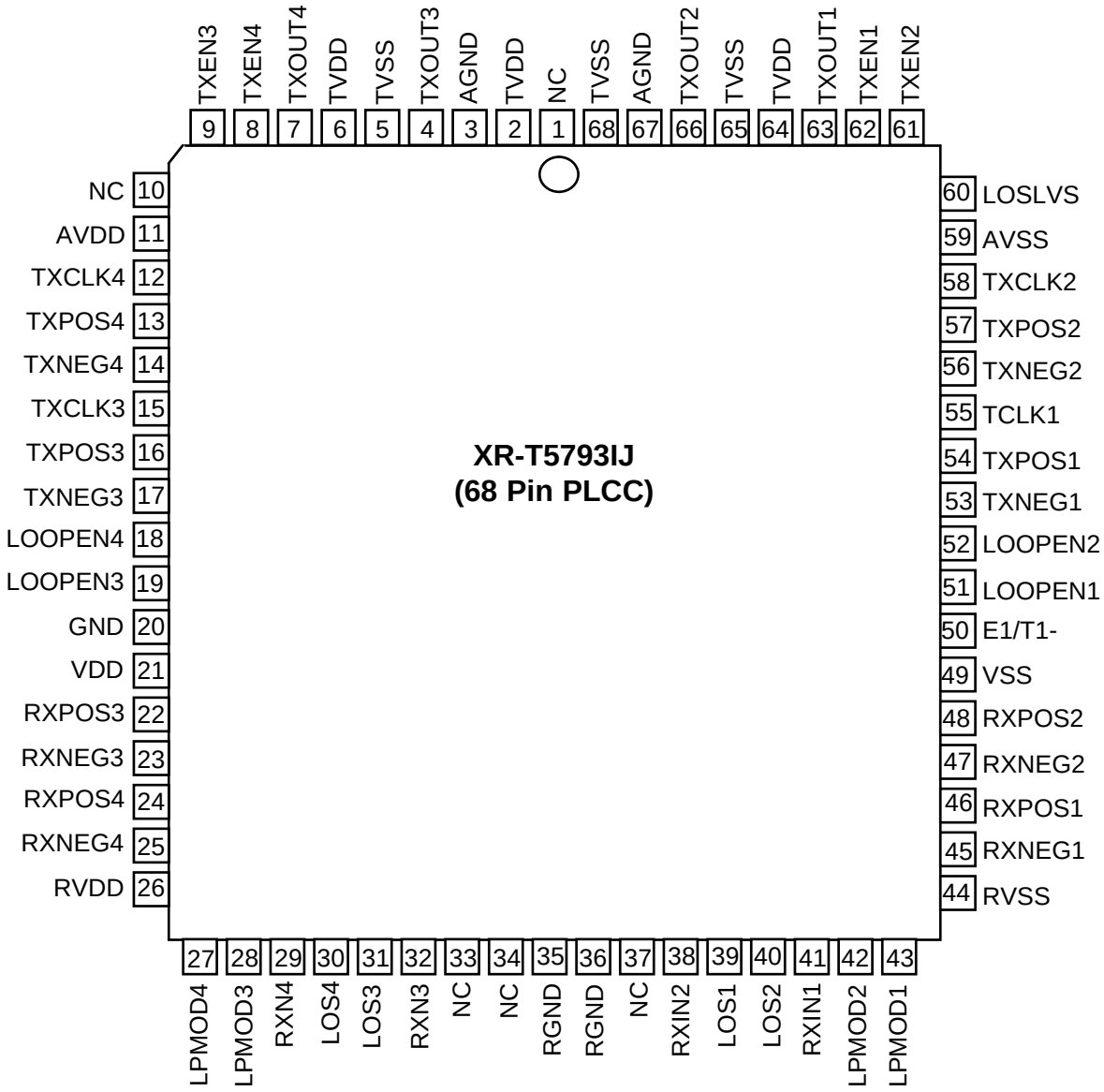
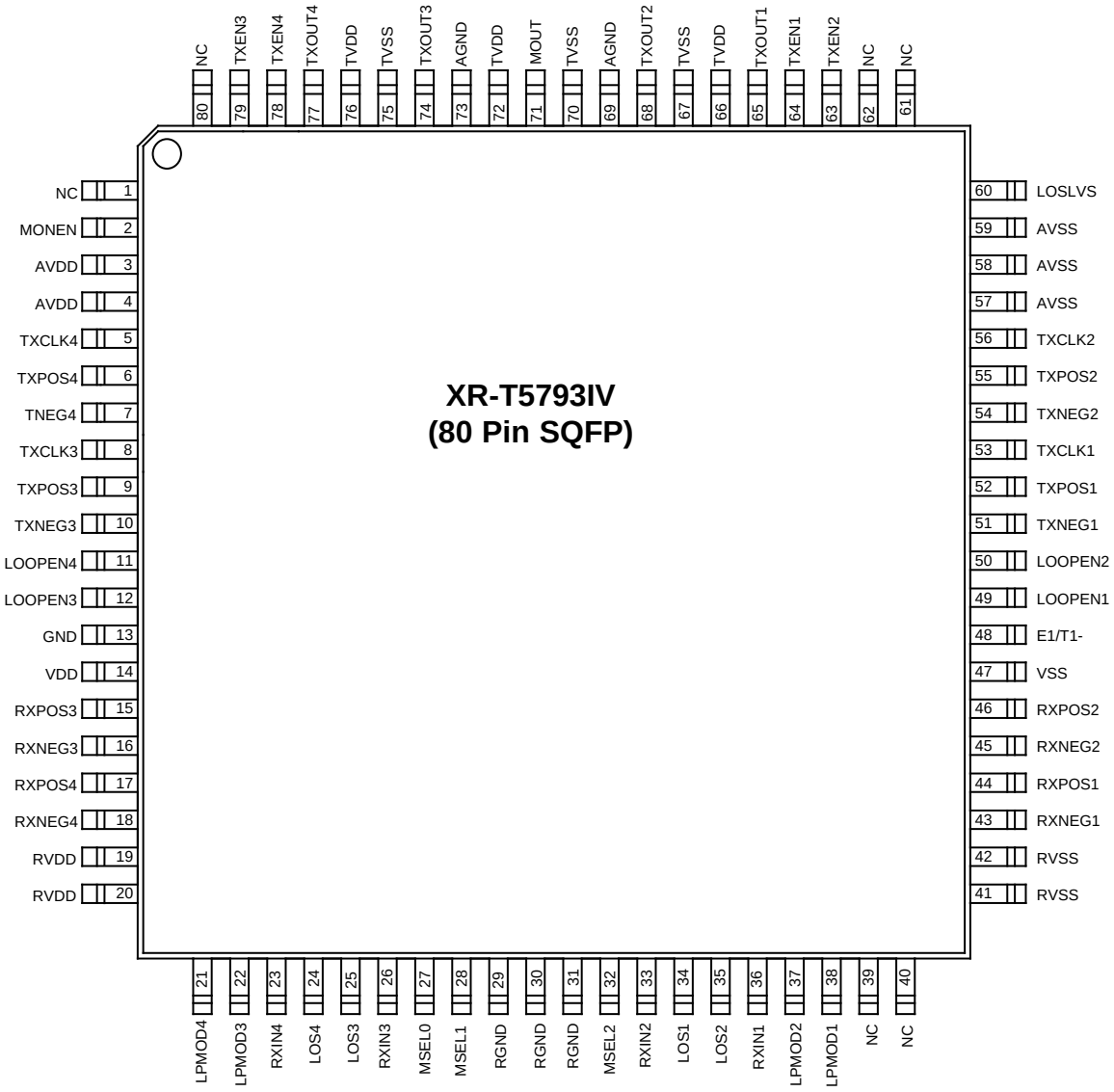

TXEN3 9
TXEN4 8
TXOUT4 7
TVDD 6
TVSS 5
TXOUT3 4
AGND 3
TVDD 2
NC 1
TVSS 68
AGND 67
TXOUT2 66
TVSS 65
TVDD 64
TXOUT1 63
TXEN1 62
TXEN2 61
NC 10
AVDD 11
TXCLK4 12
TXPOS4 13
TXNEG4 14
TXCLK3 15
TXPOS3 16
TXNEG3 17
LOOPEN4 18
LOOPEN3 19
GND 20
VDD 21
RXPOS3 22
RXNEG3 23
RXPOS4 24
RXNEG4 25
RVDD 26
60 LOSLVS
59 AVSS
58 TXCLK2
57 TXPOS2
56 TXNEG2
55 TCLK1
54 TXPOS1
53 TXNEG1
52 LOOPEN2
51 LOOPEN1
50 E1/T1-
49 VSS
48 RXPOS2
47 RXNEG2
46 RXPOS1
45 RXNEG1
44 RVSS
27 LPMOD4
28 LPMOD3
29 RXN4
30 LOS4
31 LOS3
32 RXN3
33 NC
34 NC
35 RGND
36 RGND
37 NC
38 RXIN2
39 LOS1
40 LOS2
41 RXIN1
42 LPMOD2
43 LPMOD1
XR-T5793IJ
(68 Pin PLCC)

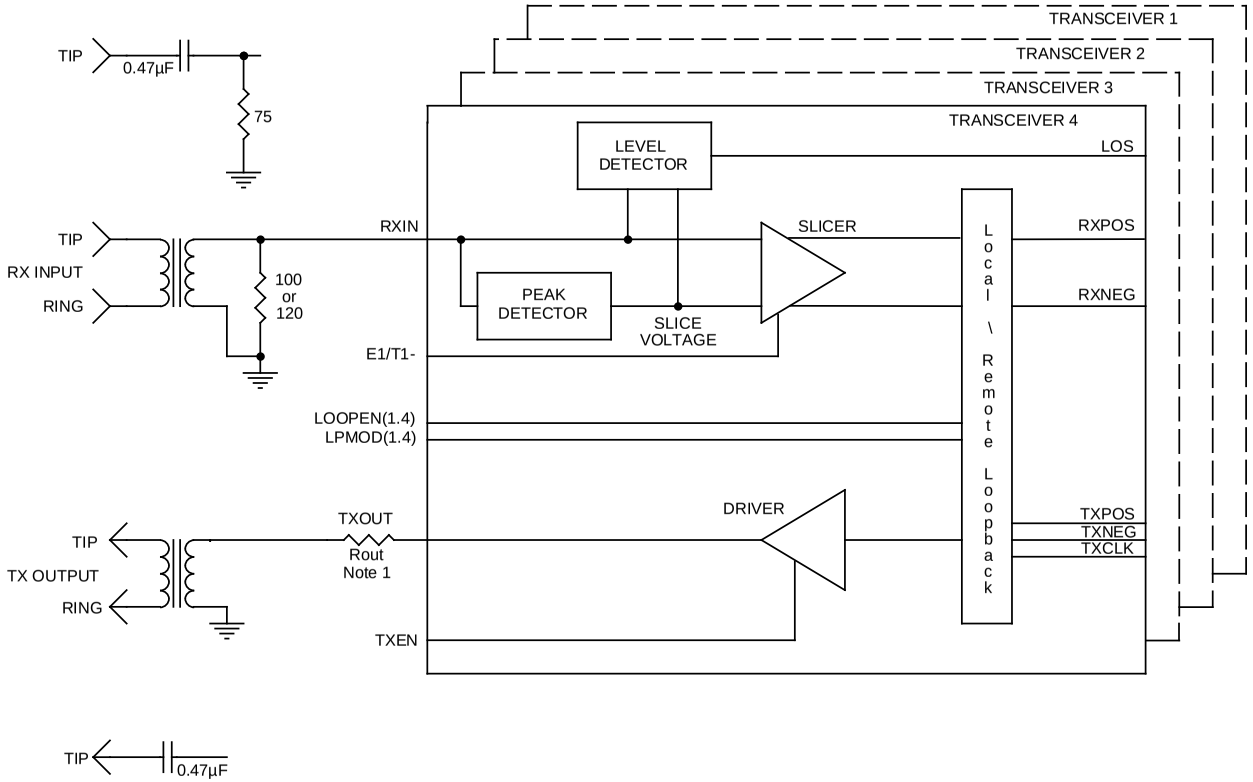

XR-T5793IV
(80 Pin SQFP)
1 NC
2 MONEN
3 AVDD
4 AVDD
5 TXCLK4
6 TXPOS4
7 TNEG4
8 TXCLK3
9 TXPOS3
10 TXNEG3
11 LOOPEN4
12 LOOPEN3
13 GND
14 VDD
15 RXPOS3
16 RXNEG3
17 RXPOS4
18 RXNEG4
19 RVDD
20 RVDD
21 LPMOD4
22 LPMOD3
23 RXIN4
24 LOS4
25 LOS3
26 RXIN3
27 MSEL0
28 MSEL1
29 RGND
30 RGND
31 RGND
32 MSEL2
33 RXIN2
34 LOS1
35 LOS2
36 RXIN1
37 LPMOD2
38 LPMOD1
39 NC
40 NC
41 RVSS
42 RVSS
43 RXNEG1
44 RXPOS1
45 RXNEG2
46 RXPOS2
47 VSS
48 E1/T1-
49 LOOPEN1
50 LOOPEN2
51 TXNEG1
52 TXPOS1
53 TXCLK1
54 TXNEG2
55 TXPOS2
56 TXCLK2
57 AVSS
58 AVSS
59 AVSS
60 LOSLVS
61 NC
62 NC
63 TXEN2
64 TXEN1
65 TXOUT1
66 TVDD
67 TVSS
68 TXOUT2
69 AGND
70 TVSS
71 MOUT
72 TVDD
73 AGND
74 TXOUT3
75 TVSS
76 TVDD
77 TXOUT4
78 TXEN4
79 TXEN3
80 NC

75 Ohm unbalanced
(Without Transformer)
Impedance selectable
receivers. Return loss
exceeds G.703
120 Ohm balanced
(or 100 Ohm)

LOS Threshold based on G775

120,100 or 75 Ohm balanced

Impedance selectable
Tristate Drivers
Return Loss exceeds
ETSI 300 166
75 Ohm unbalanced
(Without Transformer)



Note 1: Rout = 68 Ohm for 120 Ohm line impedance
Rout = 62 Ohm for 100 Ohm line impedance
Rout = 68 Ohm for 75 Ohm line impedance

Figure 1. XR-T5793 Block Diagram

SYSTEM DESCRIPTION

This device is a quad E1 transceiver which provides electrical interface for 2.048 Mbps applications. Its unique architecture includes four receiver circuits that convert CCITT G.703 compliant bipolar signals to TTL compatible logic levels. Likewise, in the other direction, four transmitters translate TTL compatible logic levels to G.703 compatible bipolar signals.

This device supports two different types of loopback functions. Each of four channels can be independently looped either in local or remote sides digitally. The remote loopback is performed between the receiver input and transmitter output. To activate the remote loopback on channel n, LOOPENn and LPMODn inputs are driven high. Local loopback on channel n, can be established similarly by driving LOOPENn high and clearing LPMODn inputs. More than one channel can be tested simultaneously.

RECEIVERS

Each of the four identical E1 line receivers will accept bipolar signals meeting the CCITT G.703 pulse mask requirements. Each input stage consists of a slicing circuitry which samples the incoming pulses at a fixed percentage of the signals maximum amplitude. The slicing voltage level is generated using a precision peak detector. The receiver section can tolerate up to 12 dB of line loss (measured at 1.024 MHz).

A loss of signal (LOS) is detected on any inputs by input fail circuitry. There is an independent LOS pin dedicated for each of the receivers. The LOS detection is based on signal energy instead of number of zeros.

A balanced signal (100 or 120 Ohms) must be coupled by a transformer. An unbalanced signal (75 Ohm) may be coupled via capacitor or a transformer.

TRANSMITTERS

This device contains four identical CCITT G.703 compliant transmitters which meet the return loss requirements. Each transmitter is a single-ended voltage driver. External resistors are used to maintain an accurate source impedance that has a high return loss to the transformer or the capacitor. Each of the drivers can be individually disabled, this is required in fault tolerant applications where redundancy is a requirement. During power-down mode of operation the bipolar outputs can be disabled.

To protect the data integrity during a brownout, the output pulse amplitudes are reduced by a factor of 25% if the supply drops below an internally set limit.

Transmission is possible either with or without a clock. If a clock is used, the transmit input data must consist of full-width NRZ pulses, and the transmitter output pulse width is determined by the duty cycle of the clock. If the transmit clock is tied high, the transmitter output pulses are determined by the input data pulse width. In this mode, RZ data must be supplied to the device.

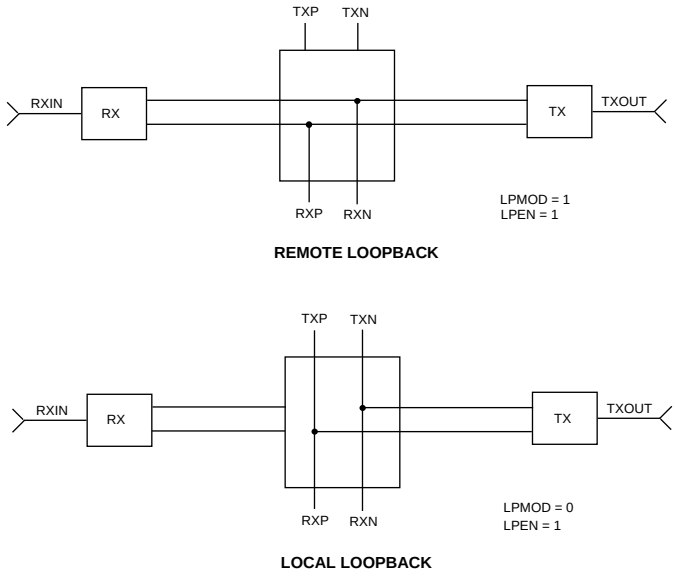


Figure 2. Loopback Configurations

Output Transformer Selection

The 1:1.265 ratio output transformer is recommended for the XR-T5793 because this ratio gives the best possible transmitter output return loss for 120 Ohm balanced E1 service. However, other transformers may provide an adequate return loss for many applications. The two characteristics that determine series build-out resistor requirements are:

- Driver output impedance is less than 5 Ohms.
- V_S, which is the driver open circuit output voltage, is 4.5 Volts peak.

The following method may be used to determine transformer suitability for a given use.

1. List the application requirements.

   Transformer ratio = 1:n
   V_O = Peak output pulse amplitude
   R_L = Load resistance

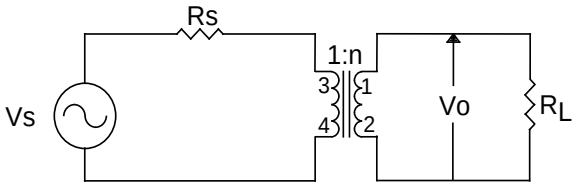


Figure 3. Equivalent Impedance Schematic

2. Calculate equivalent output voltage and load resis tance without the transformer.

$$R_{eq} = \frac{R_L}{n^2}$$

$$V_{eq} = \frac{V_o}{n}$$

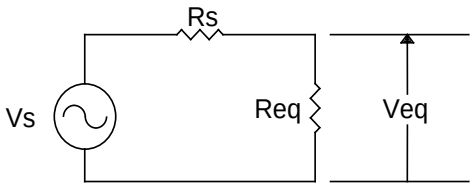


Figure 4.. Equivalent Simplified Schematic

3. Calculate the source resistance, R_S.

$$R_s = R_{eq}\left(\frac{V_s}{V_{eq}} - 1\right)$$

4. Now calculate the theoretical return loss.

$$\text{Return Loss} = 20\log\left(\frac{R_{eq} + R_s}{R_{eq} - R_s}\right)$$

The calculation given below uses the recommended 1:1.265 ratio transformer as an example:

Transformer Ratio = 1:1.265
V_O = 3.0 Volts Peak
R_L = 120 Ohms

$$R_{eq} = \frac{R_L}{n^2} = \frac{120}{1.6} = 75\Omega$$

$$V_{eq} = \frac{V_o}{n} = \frac{3.0}{1.265} = 2.37V$$

$$R_s = R_{eq}\left(\frac{V_s}{V_{eq}} - 1\right) = 75\left(\frac{4.5}{2.37} - 1\right) = 67.4\Omega$$

(Datasheet specifies standard value of 68Ω)
Calculate the theoretical return loss to determine if the transformer is acceptable.

$$\text{Return Loss} = 20\log\left(\frac{75 + 67.4}{75 - 67.4}\right) = 25.5dB$$

PIN DESCRIPTION

PLCC Pin #	SQFP PIN #	SYMBOL	TYPE	DESCRIPTION
1	71	NC	-	**NOT CONNECTED**
2	72	TVDD	VDD	**TRANSMIT VDD -** +5 V (+/-5%).
3	73	AGND	GND	**ANALOG GROUND**
4	74	TXOUT3	O	**TRANSMITTER 3 OUTPUT-** Transmitter 3 bipolar output connected to coupling capacitor or pulse transformer by a resistor.
5	75	TVSS	VSS	**TRANSMIT VSS -** -5 V (+/- 5%).
6	76	TVDD	VDD	**TRANSMIT VDD -** +5 V (+/-5%).
7	77	TXOUT4	O	**TRANSMITTER 4 OUTPUT-** Transmitter 4 bipolar output connected to coupling capacitor or pulse transformer by a resistor.
8	78	TXEN4	I	**TRANSMITTER 4 OUTPUT ENABLE -** If driven high the transmitter 4 output drivers are enabled. Hi-Z otherwise.
9	79	TXEN3	I	**TRANSMITTER 3 OUTPUT ENABLE -** If driven high the transmit ter 3 output drivers are enabled. Hi-Z otherwise.
10	2	NC	-	**NOT CONNECTED**
11	3,4	AVDD	VDD	**ANALOG VDD**
12	5	TXCLK4	I	**TRANSMITTER 4 CLOCK INPUT -** Apply logic one when RZ signals are supplied to data inputs.
13	6	TXPOS4	I	**TRANSMITTER 4 POSITIVE DATA IN -** Positive data input in NRZ or RZ format for transmitter 4.
14	7	TXNEG4	I	**TRANSMITTER 4 NEGATIVE DATA IN -** Negative data input in NRZ or RZ format for transmitter 4.
15	8	TXCLK3	I	**TRANSMITTER 3 CLOCK INPUT -** Apply logic one when RZ signals are supplied to data inputs.

PIN DESCRIPTION (Cont.)

PLCC Pin #	SQFP PIN #	SYMBOL	TYPE	DESCRIPTION
16	9	TXPOS3	I	**TRANSMITTER 3 POSITIVE DATA IN -** Positive data input in NRZ or RZ format for transmitter 3.
17	10	TXNEG3	I	**TRANSMITTER 3 NEGATIVE DATA IN -** Negative data input in NRZ or RZ format for transmitter 3.
18	11	LOOPEN4	I	**LOOP ENABLE 4 -** If driven high the specified loop type will be enabled for channel 4. Otherwise normal operation will continue.
19	12	LOOPEN3	I	**LOOP ENABLE 3 -** If driven high the specified loop type will be enabled for channel 3. Otherwise normal operation will continue.
20	13	GND	GND	**DIGITAL GROUND**
21	14	VDD	VDD	**DIGITAL VDD -** +5 V (+/-5%).
22	15	RXPOS3	O	**RECEIVER 3 POSITIVE DATA OUT -** Positive data output in NRZ or RZ format for receiver 3.
23	16	RXNEG3	O	**RECEIVER 3 NEGATIVE DATA OUT -** Negative data output in NRZ or RZ format for receiver 3.
24	17	RXPOS4	O	**RECEIVER 4 POSITIVE DATA OUT**- Positive data output in NRZ or RZ format for receiver 4.
25	18	RXNEG4	O	**RECEIVER 4 NEGATIVE DATA OUT -** Negative data output in NRZ or RZ format for receiver 4.
26	19,20	RVDD	VDD	**RECEIVE VDD -** +5 V (+/-5%).
27	21	LPMOD4	I	**LOOP MODE 4 -** If driven high the loopback mode of channel 4 will be set to remote loop. Otherwise the loopback mode will remain at local loop. The actual loopback will be activated when the LOOPEN4 is asserted.
28	22	LPMOD3	I	**LOOP MODE 3 -** If driven high the loopback mode of channel 3 will be set to remote loop. Otherwise the loopback mode will remain at local loop. The actual loopback will be activated when the LOOPEN3 is asserted.
29	23	RXIN4	I	**RECEIVER 4 INPUT-** Receiver 4 bipolar input connected to coupling capacitor or pulse transformer.

PIN DESCRIPTION (Cont.)

PLCC Pin #	SQFP PIN #	SYMBOL	TYPE	DESCRIPTION
30	24	LOS4	O	**RECEIVER 4 LOSS OF SIGNAL -** Asserted during LOS condition. Clear otherwise.
31	25	LOS3	O	**RECEIVER 3 LOSS OF SIGNAL -** Asserted during LOS condition. Clear otherwise.
32	26	RXIN3	I	**RECEIVER 3 INPUT-** Receiver 3 bipolar input connected to coupling capacitor or pulse transformer.
33	27	NC	-	**NOT CONNECTED**
34	28	NC	-	**NOT CONNECTED**
35	29	RGND	GND	**RECEIVE GROUND**
36	31	RGND	GND	**RECEIVE GROUND**
37	32	NC	-	**NOT CONNECTED**
38	33	RXIN2	I	**RECEIVER 2 INPUT -** Receiver 2 bipolar input connected to coupling capacitor or pulse transformer.
39	34	LOS1	O	**RECEIVER 1 LOSS OF SIGNAL -** Asserted during LOS condition. Clear otherwise.
40	35	LOS2	O	**RECEIVER 2 LOSS OF SIGNAL -** Asserted during LOS condition. Clear otherwise.
41	36	RXIN1	I	**RECEIVER 1 INPUT-** Receiver 1 bipolar input connected to coupling capacitor or pulse transformer.
42	37	LPMOD2	I	**LOOP MODE 2 -** If driven high the loopback mode of channel 2 will be set to remote loop. Otherwise the loopback mode will remain at local loop. The actual loopback will be activated when the LOOPEN2 is asserted.
43	38	LPMOD1	I	**LOOP MODE 1 -** If driven high the loopback mode of channel 1 will be set to remote loop. Otherwise the loopback mode will remain at local loop. The actual loopback will be activated when the LOOPEN1 is asserted.
44	41,42	RVSS	VSS	**RECEIVE VSS -** -5 V (+/-5%).

PIN DESCRIPTION (Cont.)

PLCC Pin #	SQFP PIN #	SYMBOL	TYPE	DESCRIPTION
45	43	RXNEG1	O	**RECEIVER 1 NEGATIVE DATA OUT -** Negative data output in NRZ or RZ format for receiver 1.
46	44	RXPOS1	O	**RECEIVER 1 POSITIVE DATA OUT -** Positive data output in NRZ or RZ format for receiver 1.
47	45	RXNEG2	O	**RECEIVER 2 NEGATIVE DATA OUT -** Negative data output in NRZ or RZ format for receiver 2.
48	46	RXPOS2	O	**RECEIVER 2 POSITIVE DATA OUT** - Positive data output in NRZ or RZ format for receiver 2.
49	47	VSS	VSS	**DIGITAL VSS -** -5 V (+/- 5%).
50	48	E1/T1-	I	**E1/T1- SELECTION -** Apply logic one to select the receive data threshold appropriate for E1 operation. Connect to ground to select the T1 data threshold.
51	49	LOOPEN1	I	**LOOP ENABLE 1 -** If driven high the specified loopback mode will be enabled for channel 1. Otherwise normal operation will continue.
52	50	LOOPEN2	I	**LOOP ENABLE 2 -** If driven high the specified loopback mode will be enabled for channel 2. Otherwise normal operation will continue.
53	51	TXNEG1	I	**TRANSMITTER 1 NEGATIVE DATA IN -** Negative data input in NRZ or RZ format for transmitter 1.
54	52	TXPOS1	I	**TRANSMITTER 1 POSITIVE DATA IN -** Positive data input in NRZ or RZ format for transmitter 1.
55	53	TXCLK1	I	**TRANSMITTER 1 CLOCK INPUT -** Apply logic one when RZ signals are supplied to data inputs.
56	54	TXNEG2	I	**TRANSMITTER 2 NEGATIVE DATA IN -** Negative data input in NRZ or RZ format for transmitter 2.
57	55	TXPOS2	I	**TRANSMITTER 2 POSITIVE DATA IN -** Positive data input in NRZ or RZ format for transmitter 2.
58	56	TXCLK2	I	**TRANSMITTER 2 CLOCK INPUT -** Apply logic one when RZ signals are supplied to data inputs.

PIN DESCRIPTION (Cont.)

PLCC Pin #	SQFP PIN #	SYMBOL	TYPE	DESCRIPTION
59	57,58,59	AVSS	VSS	**ANALOG VSS**
60	60	LOSLVS	I	**LOSS OF SIGNAL VOLTAGE SELECT -** Apply logic one to select LOS voltage level appropriate for 120 Ohm balanced receiver operation. Connect to ground to choose LOS voltage for 75 Ohm unbalanced operation.
61	63	TXEN2	I	**TRANSMITTER 2 OUTPUT ENABLE -** If asserted the transmitter 2 output drivers are enabled. High-Z otherwise.
62	64	TXEN1	I	**TRANSMITTER 1 OUTPUT ENABLE -** If asserted the transmitter 1 output drivers are enabled. High-Z otherwise.
63	65	TXOUT1	O	**TRANSMITTER 1 OUTPUT -** Transmitter 1 bipolar output connected to coupling capacitor or pulse transformer through a resistor.
64	66	TVDD	VDD	**TRANSMIT VDD -** +5 V (+/-5%).
65	67	TVSS	VSS	**TRANSMIT VSS -** +5 V (+/-5%).
66	68	TXOUT2	O	**TRANSMITTER 2 OUTPUT-** Transmitter 2 bipolar output connected to coupling capacitor or pulse transformer through a resistor.
67	69	AGND	GND	**ANALOG GROUND**
68	70	TVSS	VSS	**TRANSMIT VDD -** +5 V (+/-5%).
-	30	RGND	GND	**RECEIVE GROUND**
-	1,39,40, 61,62,80	NC	-	**NOT CONNECTED**

Table 1: Return Loss Requirements (resistor tolerance: 1% on transmit side, 2% on receive side)

TRANSMIT INTERFACE	75	Ohm	100	Ohm	120	Ohm	
	MIN	TYP	MIN	TYP	MIN	TYP	UNITS
51KHz TO 102 KHz	18	22	18	22	18	22	dB
102 KHz TO 2.048 MHz	18	22	18	22	18	22	dB
2.048 MHz TO 3.072 MHz	18	22	18	22	18	22	dB

RECEIVE INTERFACE	75	Ohm	100	Ohm	120	Ohm	
	MIN	TYP	MIN	TYP	MIN	TYP	UNITS
51KHz TO 102 KHz	20	30	20	30	20	30	dB
102 KHz TO 2.048 MHz	20	30	20	30	20	30	dB
2.048 MHz TO 3.072 MHz	20	30	20	30	20	30	dB

Note: *The return loss has been measured on the evaluation board coupled via a capacitor and terminated with 75 Ohm impedance.*

ELECTRICAL CHARACTERISTICS

Test Conditions: TA = -40 to **25** to 85°C, all VDDs = **5V** +/- 5%, all VSSs = **-5V** +/-5%, all GNDs = 0V

DC PARAMETERS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
VDDs	DC supply positive	4.75	**5.00**	5.25	V	
VSSs	DC supply negative	-4.75	**-5.00**	-5.25	V	

INPUTS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
VIH	High level input	**2.0**			V	
VIL	Low level input			**0.8**	V	
Ipdc	Input pull down current			**40**	µA	

OUTPUTS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
VOH	High level output	3.5			V	IOH = -10µA
VOH	High level output	**2.4**			V	IOH = -40µA
VOL	Low level output			**0.4**	V	IOL = 1.6mA

RECEIVER SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
R_{XP}	Receiver sensitivity	0.6		4.2	Vp	
R_{XCL}	Allowed cable loss	0	10	12	dB	1.024 MHz (E1)
	(0dB=2.4V)	0	10	12	dB	772 KHz (T1)
R_{XIWT}	Interference margin (E1)	16			dB	with 6dB cable loss
Rxti	Receiver slicing level (T1) (Note 1)	**60**	65	**70**	%	Peak Voltage %
Rxei	Receiver slicing level (E1) (Note 1)	**45**	50	**55**	%	Peak Voltage %
Rxlos	Receiver LOS threshold		0.2	**0.3**	V	
R_{in}	Input resistance	2.5			kΩ	Up to 3.072 MHz

Note 1: *Selected by E1/T1-*
Note 2: *Bold face parameters are covered by production test and guaranteed over operating temperature range.*

POWER SPECIFICATIONS (without monitor channel)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
Pd	Power dissipation		400	**680**	mW	
Pd	Power dissipation		250	280	mW	All drivers in High-Z
Pc	Power Consumption 75 Ohm (Note 1)		500	833	mW	All 1's transmit & receive
Pc	Power Consumption 100 Ohm (Note 1)		475	860	mW	All 1's transmit & receive
Pc	Power Consumption 120 Ohm (Note 1)		450	830	mW	All 1's transmit & receive
P_{VDD}	Power supply requirement			Pc/2+5mW	mW	
P_{VSS}	Power supply requirement			Pc/2-5mW	mW	

Note 1: *Power consumption = power dissipation + power to the cable.*
Note 2: *Bold face parameters are covered by production test and guaranteed over operating temperature range.*

INPUT TRANSFORMER REQUIREMENTS

TURNS RATIO	LINE IMPEDANCE	R_{LOAD}
1:1	75 Ohms	75 Ohms
1:1	120 Ohms	120 Ohms
1:1	100 Ohms	100 Ohms

OUTPUT TRANSFORMER REQUIREMENTS

TURNS RATIO	LINE IMPEDANCE	R_{OUT}
1:1	75 Ohms	68 Ohms
1:1.265	120 Ohms	68 Ohms
1:1.265	100 Ohms	62 Ohms

Magnetic Supplier Information:

Pulse
Telecom Product Group
P.O. Box 12235
San Diego, CA 92112
Tel. (619)674-8100
Fax. (619)674-8262

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ELECTRICAL CHARACTERISTICS (Continued)

Test Conditions: TA = -40 to **25** to 85°C, all VDDs = **5V** +/- 5%, all VSSs = **-5V** +/-5%, all GNDs = 0V

AC PARAMETERS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{TXOUT}	Output pulse amplitude (75 Ohm)	**2.13**	2.37	**2.60**	V	
V_{TXOUT}	Output pulse amplitude (120 Ohm)	2.70	3.0	3.30	V	
V_{TXOUT}	Output pulse amplitude (100 Ohm)	2.3	3.0	3.7	V	
T_{XPW}	Pulse width (2.048 MHz)	**224**	244	**264**	nS	Determined by TX clock
T_{XPW}	Pulse width (1.544 MHz)	274	324	374	nS	Determined by TX clock
	Pos/neg pulse imbalance	-5%		+5%	%	
T_1	TXCLK clock period (E1)		488		nS	
T_2	TXCLK clock period (T1)		648		nS	
T_3	TXCLK duty cycle	48	50	52	%	
T_4	Data setup time, TDATA to TCLK	**50**			nS	
T_5	Data hold time, TCLK to TDATA	**50**			nS	
Tr	Clock rise time			30	nS	
Tf	Clock fall time			30	nS	
T_6	Receive data high (E1)	**219**	244	**269**	nS	0 dB cable loss
T_7	Data propagation delay			**100**	nS	
T_8	Receive Rise Time			**50**	ns	
T_9	Receive Fall Time			**50**	ns	

Note: *Bold face parameters are covered by production test and guaranteed over operating temperature range.*

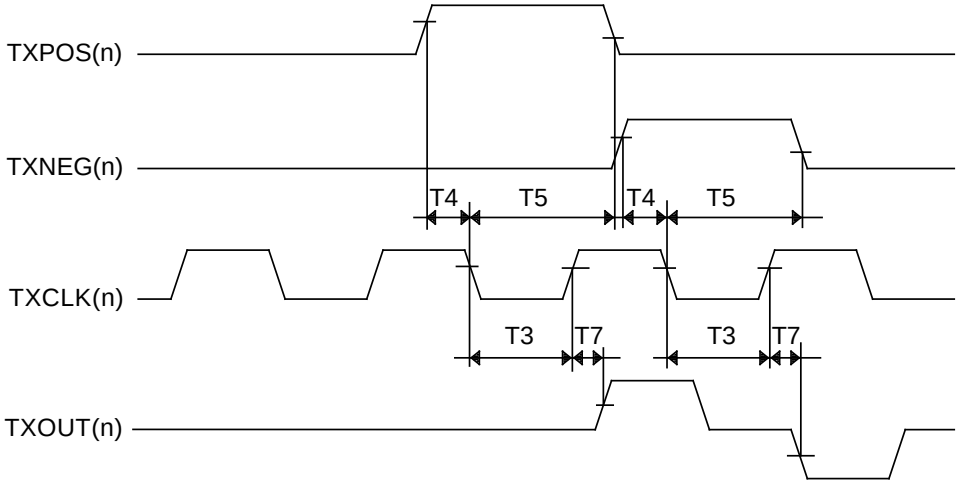


Figure 5. Transmit Timing Diagram

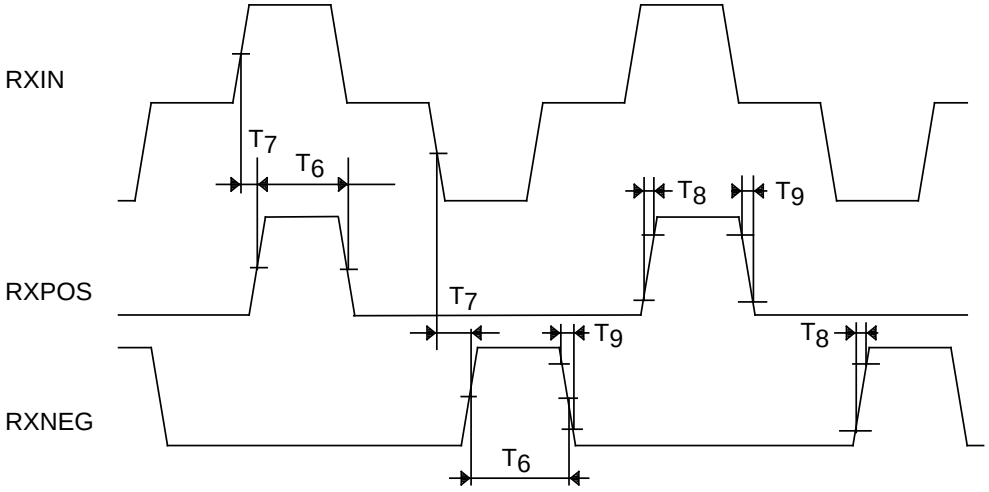


Figure 6. Receive Timing Diagram

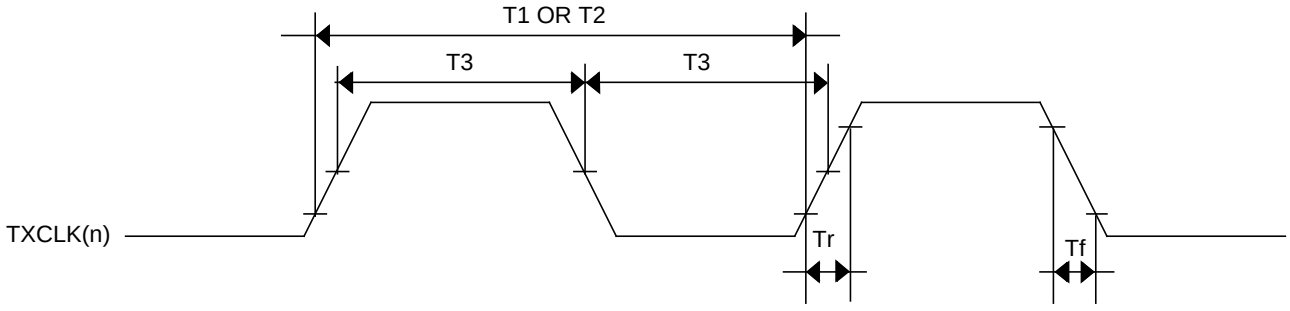
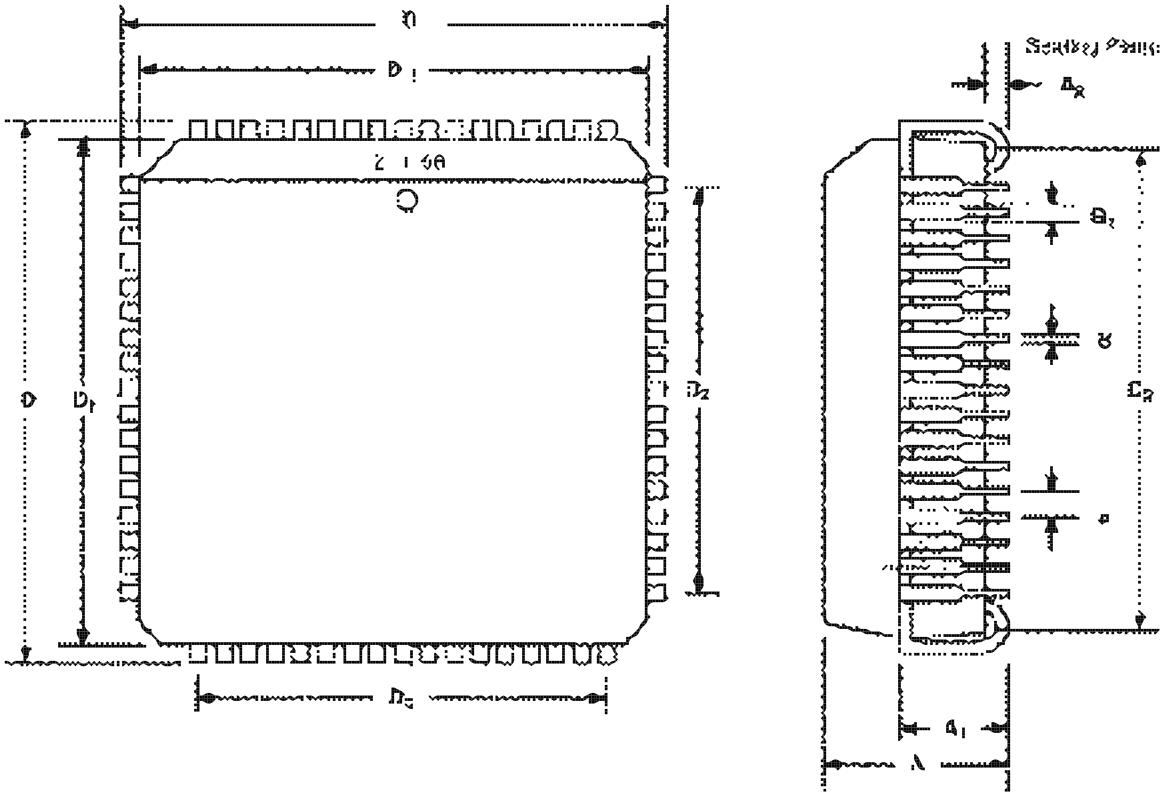


Figure 7. Transmit Clock Timing

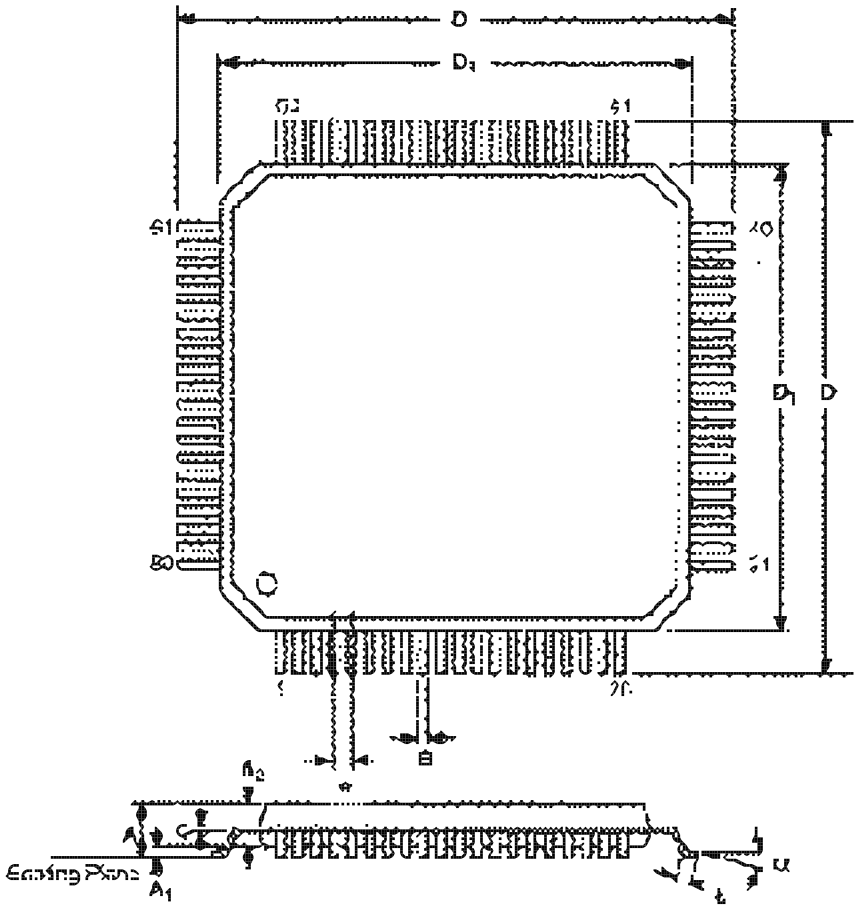
JEDEC 68 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.200	4.19	5.08
A_1	0.090	0.120	2.29	3.04
A_2	0.020 min		0.51 min	
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
D	0.985	0.995	25.02	25.27
D_1	0.950	0.958	24.13	24.33
D_2	0.890	0.930	22.61	23.62
e	0.050 typ		1.27 typ	
g	0.050 BSC		1.27 BSC	

Note: *Package has been manufactured to comply with specifications listed under millimeters column.*

80 LEAD SHRINK QUAD FLAT PACK
(14 x14 x 1.4 MM, SQFP)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.063	1.35	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.005	0.009	0.13	0.23
C	0.004	0.008	0.09	0.20
D	0.622	0.638	15.80	16.20
D1	0.547	0.555	13.90	14.10
e	0.026 BSC		0.65 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: *Package has been manufactured to comply with specifications listed under millimeters column.*

NOTICE

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