March 1996-2

E-1 Line Interface Unit

GENERAL DESCRIPTION

The XR-T5791 is an optimized line interface unit, built using low power CMOS technology. This device contains an E1 channel for primary rate, PCM applications up to 2.048 Mbps. It performs the driver and receiver functions necessary to convert bipolar signals to TTL/CMOS compatible logic levels and vice versa. The device supports single ended or balanced line interfaces, thereby providing the user an option of reducing system cost and board space by replacing the transformer with a capacitor.

The driver can be disabled, allowing maximum flexibility in system power management. The output pulse is fully CCITT G.703 compliant. Moreover, the return loss is at least 18 dB over a frequency range of 51 KHz to 3.072 MHz.

The slicing circuit in the receive path is able to tolerate a maximum of 12 dB of cable loss with a minimum input sensitivity of 600 mV over the operating temperature range. Return loss on the receive interface is minimum 20 dB from 51 KHz to 3.072 MHz.

Local and remote loopbacks can be performed. A loss of signal (LOS) detection circuitry and a LOS pin is provided.

The XR-T5791 is targeted toward single channel line interface cards. Also, the device is designed to be used with EXAR's quad channel LIU, the XR-T5794 or the XR-T5793, for multi channel cards where there are odd number of channels or the number of channels is not a multiple of four. Furthermore, the device may be used in T1 applications (1.544 Mbps) which do not require meeting the DSX-1 cross connect pulse template.

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5791ID	18 Pin SOIC	-40°C to +85°C
XR-T5791IP	18 Pin PDIP	-40°C to +85°C

FEATURES

Meets CCITT G.703 pulse mask template for 2.048 Mbps (E1) rates

Transmitter and receiver interfaces can be:

- Single ended, 75 Ohm capacitive or transformer coupled
- Balanced, 100 or 120 Ohm transformer coupled

Minimum return loss is 20 dB (receive) and 18 dB (transmit), exceeds G.703 and ETSI 300 166 specifications

Bipolar output can be disabled (High Z output)

System interface is TTL compatible on digital input and TTL/CMOS compatible on digital output pins

Loss of signal detection

Local and remote digital loopback

Low power, CMOS technology

Over-temperature protection

APPLICATION

E1 line interface cards

E1 network equipment
- Multiplexers
- Cross connects
- Switching systems

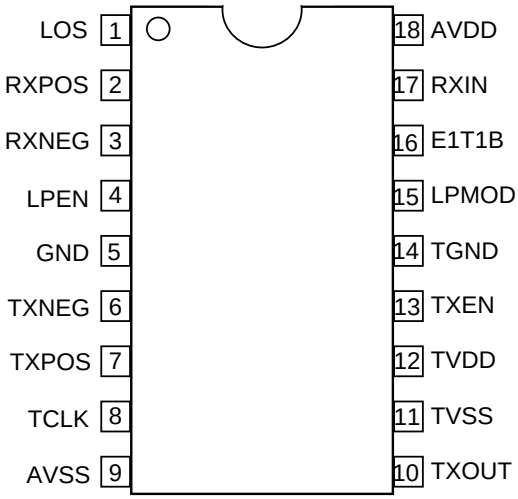
Fault tolerant systems

ABSOLUTE MAXIMUM RATINGS

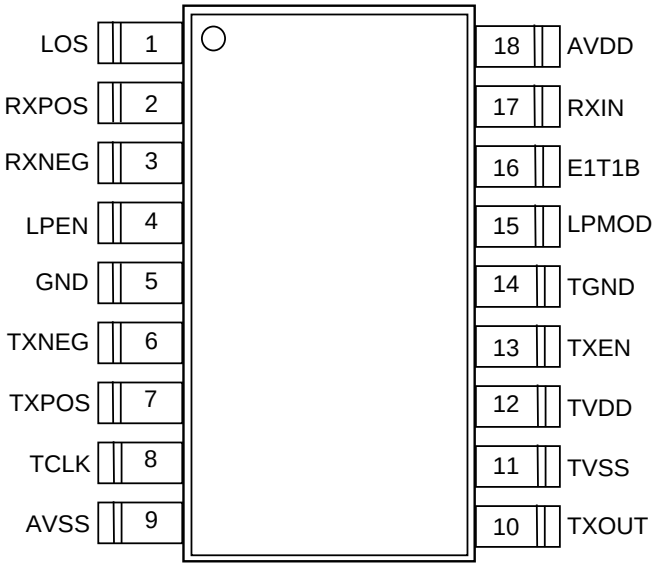
Storage Temperature	-65°C to +150°C
Supply Voltage	+/-7V

EXAR Corporation • 48720 Kato Road, Fremont, CA 94538 • (510)668-7000 • (510)668-7017 fax

PDIP



JEDEC
SOIC



XR-T5791 Pin Assignments

75 Ohm unbalanced (without transformer) Impedance selectable receivers. Return loss exceeds G.703

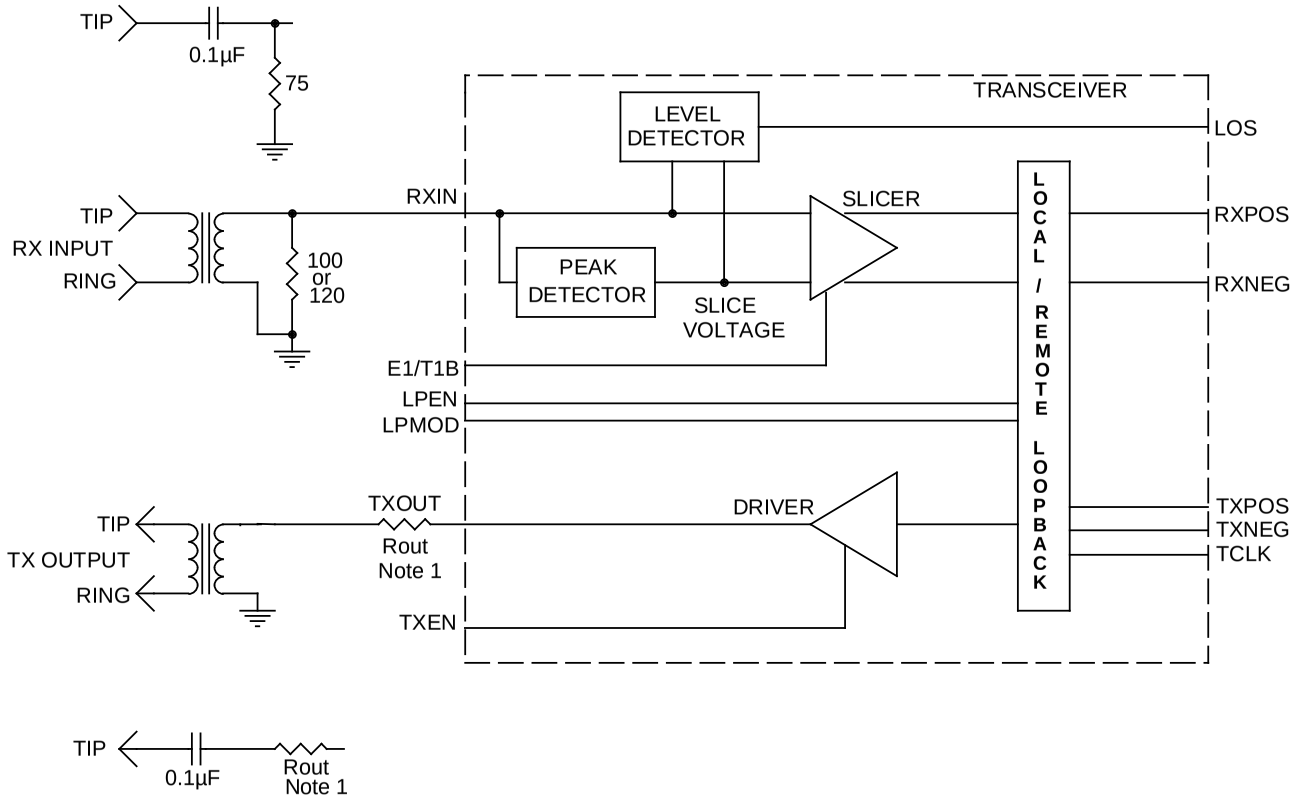
120 Ohm balanced (or 100 Ohm)

LOS Threshold based on G.775

120,100 or 75 Ohm balanced

Impedance selectable Tristate Driver Return Loss exceeds ETSI 300 166

75 Ohm unbalanced (without transformer)



Note 1: Rout = 68 Ohm for 120 Ohm line impedance
Rout = 62 Ohm for 100 Ohm line impedance
Rout = 68 Ohm for 75 Ohm line impedance

Figure 1. XR-T5791 Block Diagram

SYSTEM DESCRIPTION

This device is an E1 transceiver which provides electrical interface for 2.048 Mbps applications. Its unique architecture includes a receiver circuit that converts CCITT G.703 compliant bipolar signals to TTL compatible logic levels. Likewise, in the other direction, a transmitter translates TTL compatible logic levels to G.703 compatible bipolar signals.

This device supports two different types of loopback functions. The device can be independently looped either in local or remote sides. The remote loopback is performed between the receiver input and transmitter output. To activate the remote loopback, LPEN and LPMOD input are driven high. Local loopback, can be established similarly by driving LPEN high and LPMOD low.

RECEIVER

The E1 line receiver will accept bipolar signals meeting the CCITT G.703 pulse mask requirements. The input stage consists of a slicing circuitry which samples the incoming pulses at a fixed percentage of the signals maximum amplitude. The slicing voltage level is generated using a precision peak detector. The receiver section can tolerate up to 15 dB of line loss (measured at 1.024 MHz).

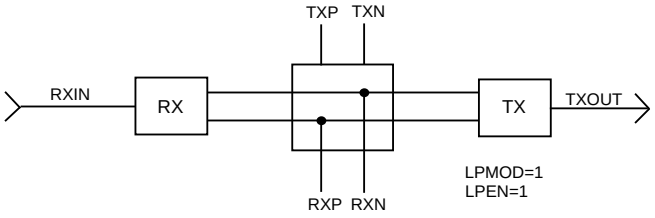
A loss of signal (LOS) is detected on the input by comparing the input signal against a reference voltage. There is a dedicated LOS pin. The LOS detection is based on signal energy instead of number of zeros. A LOS is declared if the input signal level drops below 240mV in E1 mode and 300mV in T1 mode.

A balanced signal (100 or 120 Ohms) must be coupled by a transformer. An unbalanced signal (75 Ohm) may be coupled via a capacitor or a transformer.

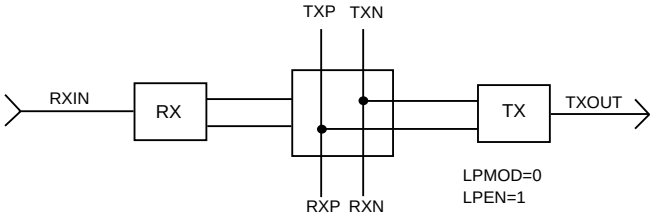
TRANSMITTER

This device contains a CCITT G.703 compliant transmitter which meets the return loss requirements. An external resistor is used to maintain an accurate source impedance that has a high return loss to the transformer or the capacitor. The driver can be disabled, as required in fault tolerant applications where redundancy is a requirement. During power-down mode of operation the bipolar output can be disabled.

Transmission is possible either with or without a clock. If a clock is used, the transmit input data must consist of full-width NRZ pulses, and the transmitter output pulse width is determined by the duty cycle of the clock. If the transmit clock is tied high, the transmitter output pulses are determined by the input data pulse width. In this mode, RZ data must be supplied to the device.



Remote Loopback



Local Loopback

Figure 2. Loopback Configurations

Output Transformer Selection

The 1:1.265 ratio output transformer is recommended for the XR-T5791 because this ratio gives the best possible transmitter output return loss for 120 Ohm balanced E1 service. However, other transformers may provide an adequate return loss for many applications. The two characteristics that determine series build-out resistor requirements are:

- Driver output impedance is less than 5 Ohms.
- V_S, which is the driver open circuit output voltage, is 4.5 Volts peak.

The following method may be used to determine transformer suitability for a given use.

1. List the application requirements.

   Transformer ratio = 1:n
   V_O = Peak output pulse amplitude
   R_L = Load resistance

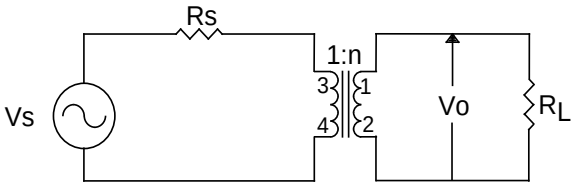


Figure 3. Equivalent Impedance Schematic

2. Calculate equivalent output voltage and load resistance without the transformer.

$$R_{eq} = \frac{R_L}{n^2}$$

$$V_{eq} = \frac{V_o}{n}$$

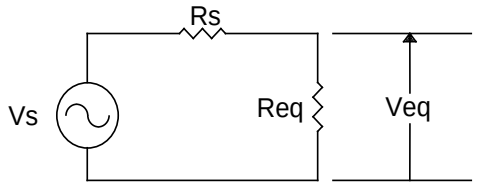


Figure 4. Equivalent Simplified Schematic

3. Calculate the source resistance, R_S.

$$R_S = R_{eq}\left(\frac{V_S}{V_{eq}} - 1\right)$$

4. Now calculate the theoretical return loss.

$$\text{Return Loss} = 20 \log \left(\frac{R_{eq} + R_S}{R_{eq} - R_S}\right)$$

The calculation given below uses the recommended 1:1.265 ratio transformer as an example:

Transformer Ratio = 1:1.265
V_O = 3.0 Volts Peak
R_L = 120 Ohms

$$Req = \frac{R_L}{n^2} = \frac{120}{1.6} = 75\Omega$$

$$V_{eq} = \frac{V_o}{n} = \frac{3.0}{1.265} = 2.37V$$

$$R_S = R_{eq}\left(\frac{Vs}{Veq} - 1\right) = 75\left(\frac{4.5}{2.37} - 1\right) = 67.4\Omega$$

(Datasheet specifies standard value of 68Ω)
Calculate the theoretical return loss to determine if the transformer is acceptable.

$$\text{Return Loss} = 20 \log \left(\frac{75 + 67.4}{75 - 67.4}\right) = 25.5dB$$

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
1	LOS	O	**Receiver Loss of Signal.** Asserted during LOS condition. Clear otherwise.
2	RXPOS	O	**Receiver Positive Data Out.** Positive data output in NRZ or RZ output.
3	RXNEG	O	**Receiver Negative Data Out.** Negative data output in NRZ or RZ output.
4	LPEN	I	**Loop Enable.** If driven high the loop-back mode will be enabled. Otherwise normal operation will continue.
5	GND	-	**Ground.**
6	TXNEG	I	**Transmitter Negative Data In.** Negative data input in NRZ or RZ format.
7	TXPOS	I	**Transmitter Positive Data In.** Positive data input in NRZor RZ format.
8	TCLK	I	**Transmitter Clock Input.** Tie high when RZ signals are applied.
9	AVSS	-	**Analog VSS Supply.** -5V (±5%).
10	TXOUT	O	**Transmitter Output.** Transmitter bipolar output connected to coupling capacitor or pulse transformer by a resistor.
11	TVSS	-	**Transmit VSS.** -5V (±5%).
12	TVDD	-	**Transmit VDD.** +5V (±5%).
13	TXEN	I	**Transmitter Output Enable.** If asserted the transmitter output drivers are enabled. High-Z otherwise.
14	TGND	-	**Transmitter Ground.**
15	LPMOD	I	**Loop Mode.** If driven high the loop-back mode will be set to remote loop. Otherwise the loop-back mode will remain at local loop. The actual loop-back will be activated when the LPEN is asserted.

PIN DESCRIPTION (Cont.)

PIN #	SYMBOL	TYPE	DESCRIPTION
16	**E1T1B**	**I**	**E1/T1 - Selection.** Tie high to select the receive data threshold appropriate for E1 operation. Tie to ground to select the T1 data threshold.
17	**RXIN**	**I**	**Receiver Input.** Receiver bipolar input connected to coupling capacitor or pulse transformer.
18	**AVDD**	**-**	**Analog VDD.**

Table 1: Return Loss Requirements (resistor tolerance:1% on transmit side, 2% on receive side)

TRANSMIT INTERFACE	**75**	**Ohm**	**100**	**Ohm**	**120**	**Ohm**	
	MIN	TYP	MIN	TYP	MIN	TYP	UNITS
51KHz TO 102 KHz	18	22	18	22	18	22	dB
102 KHz TO 2.048 MHz	18	22	18	22	18	22	dB
2.048 MHz TO 3.072 MHz	18	22	18	22	18	22	dB

RECEIVE INTERFACE	**75**	**Ohm**	**100**	**Ohm**	**120**	**Ohm**	
	MIN	TYP	MIN	TYP	MIN	TYP	UNITS
51KHz TO 102 KHz	20	30	20	30	20	30	dB
102 KHz TO 2.048 MHz	20	30	20	30	20	30	dB
2.048 MHz TO 3.072 MHz	20	30	20	30	20	30	dB

Note: *The return loss has been measured on the evaluation board coupled via a capacitor and terminated with 75 Ohm impedance.*

ELECTRICAL CHARACTERISTICS

Test Conditions: TA = -40 to **25** to 85°C, all VDDs = **5V** +/- 5%, all VSSs = **-5V** +/-5%, all GNDs = 0V

DC PARAMETERS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
VDDs	DC supply positive	4.75	**5.00**	5.25	V	
VSSs	DC supply negative	-4.75	**-5.00**	-5.25	V	

INPUTS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
VIH	High level input	**2.0**			V	
VIL	Low level input			**0.8**	V	
Ipdc	Input pull down current			**40**	µA	

OUTPUTS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
VOH	High level output	3.5			V	IOH = -10µA
VOH	High level output	**2.4**			V	IOH = -40µA
VOL	Low level output			**0.4**	V	IOL = 1.6mA

RECEIVER SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
R_{XP}	Receiver sensitivity	0.6		4.2	Vp	
R_{XCL}	Allowed cable loss	0	10	12	dB	1.024 MHz (E1)
	(0dB=2.4V)	0	10	12	dB	772 KHz (T1)
R_{XIWT}	Interference margin (E1)	16			dB	with 6dB cable loss
Rxt1	Receiver slicing level (T1) (Note 1)	**60**	65	**70**	%	Peak Voltage %
Rxe1	Receiver slicing level (E1) (Note 1)	**45**	50	**55**	%	Peak Voltage %
Rxlos	Receiver LOS threshold		0.2	**0.3**	V	
R_{in}	Input resistance	2.5			kΩ	Up to 3.072 MHz

Note 1: *Selected by E1/T1-*
Note 2: *Bold face parameters are covered by production test and guaranteed over operating temperature range.*

CONSUMPTION SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
Pd	Power dissipation		170	**220**	mW	
Pd	Power dissipation		90	130	mW	Driver in High-Z
Pc	Power Consumption 75 Ohm (Note 1)		210	260	mW	All 1's transmit & receive
Pc	Power Consumption 100 Ohm (Note 1)		212	265	mW	All 1's transmit & receive
Pc	Power Consumption 120 Ohm (Note 1)		210	260	mW	All 1's transmit & receive
P_{VDD}	Power supply requirement			Pc/2+5mW	mW	
P_{VSS}	Power supply requirement			Pc/2-5mW	mW	

Note 1: *Power consumption = power dissipation + power to the cable.*
Note 2: *Bold face parameters are covered by production test and guaranteed over operating temperature range.*

INPUT TRANSFORMER REQUIREMENTS

TURNS RATIO	LINE IMPEDANCE	R_{LOAD}
1:1	75 Ohms	75 Ohms
1:1	120 Ohms	120 Ohms
1:1	100 Ohms	100 Ohms

OUTPUT TRANSFORMER REQUIREMENTS

TURNS RATIO	LINE IMPEDANCE	R_{OUT}
1:1	75 Ohms	68 Ohms
1:1.265	120 Ohms	68 Ohms
1:1.265	100 Ohms	62 Ohms

Magnetic Supplier Information:

Pulse
Telecom Product Group
P.O. Box 12235
San Diego, CA 92112
Tel. (619)674-8100
Fax. (619)674-8262

ELECTRICAL CHARACTERISTICS (Continued)

Test Conditions: TA = -40 to **25** to 85°C, all VDDs = **5V** +/- 5%, all VSSs = **-5V** +/-5%, all GNDs = 0V

AC PARAMETERS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{TXOUT}	Output pulse amplitude (75 Ohm)	**2.13**	2.37	**2.60**	V	
V_{TXOUT}	Output pulse amplitude (120 Ohm)	2.70	3.0	3.30	V	
V_{TXOUT}	Output pulse amplitude (100 Ohm)	2.3	3.0	3.7	V	
T_{XPW}	Pulse width (2.048 MHz)	**224**	244	**264**	ns	Determined by TX clock
T_{XPW}	Pulse width (1.544 MHz)	274	324	374	ns	Determined by TX clock
	Pos/neg pulse imbalance	-5		+5	%	
T_1	TXCLK clock period (E1)		488		ns	
T_2	TXCLK clock period (T1)		648		ns	
T_3	TXCLK duty cycle	48	50	52	%	
T_4	Data setup time, TDATA to TCLK	**50**			ns	
T_5	Data hold time, TCLK to TDATA	**50**			ns	
Tr	Clock rise time			30	ns	
Tf	Clock fall time			30	ns	
T_6	Receive data high (E1)	**219**	244	**269**	ns	0 dB cable loss
T_7	Data propagation delay			**100**	ns	
T_8	Receive Rise Time			**50**	ns	
T_9	Receive Fall Time			**50**	ns	

Note : *Bold face parameters are covered by production test and guaranteed over operating temperature range.*

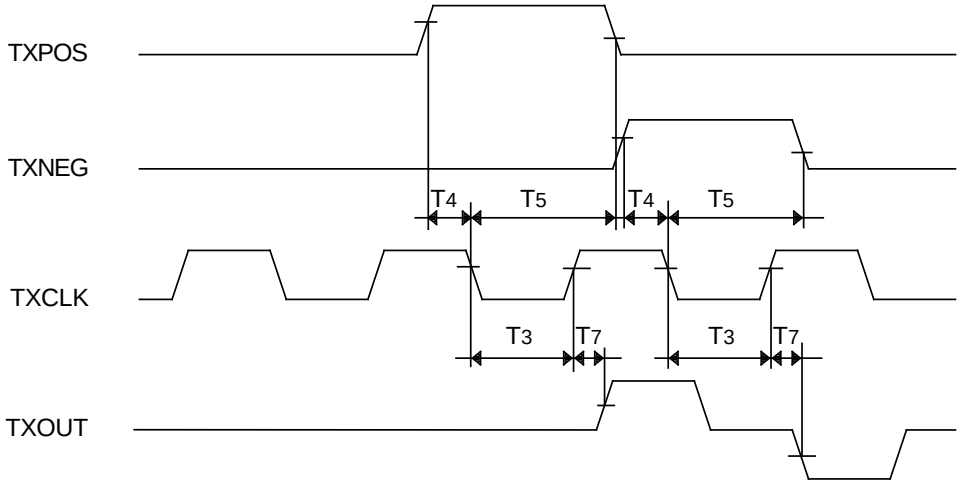


Figure 5. Transmit Timing Diagram

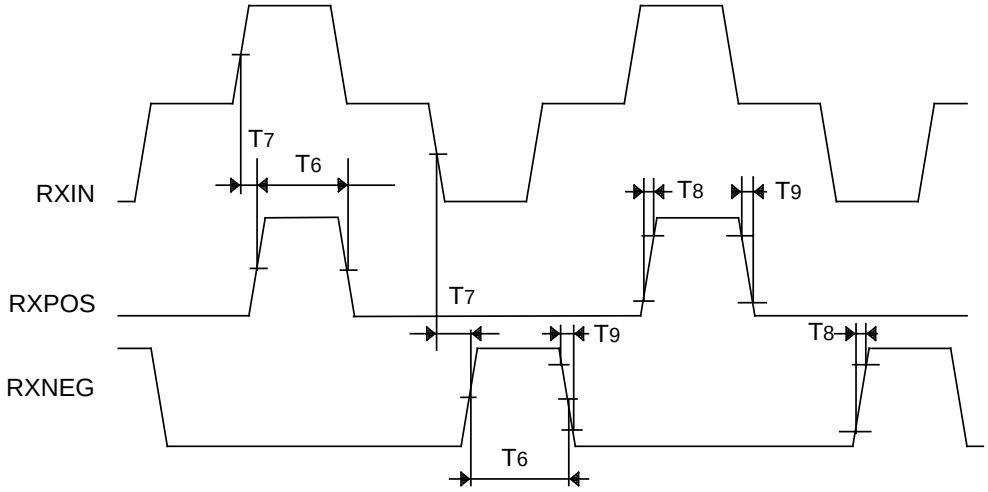


Figure 6. Receive Timing Diagram

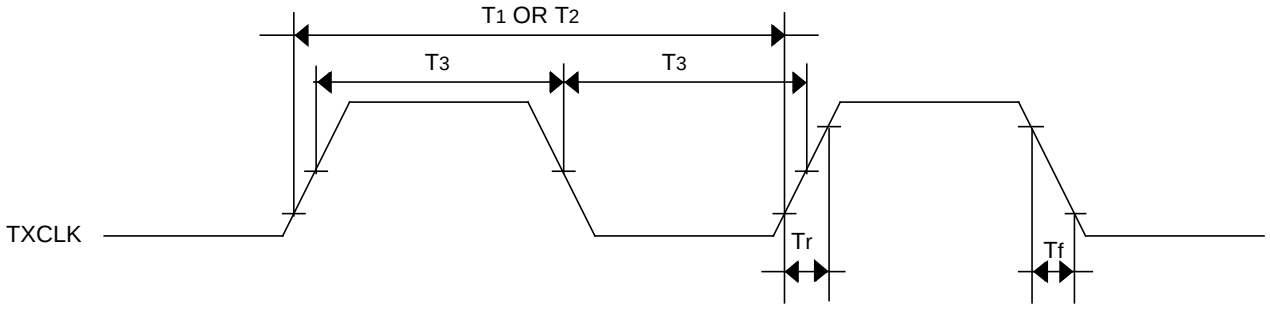
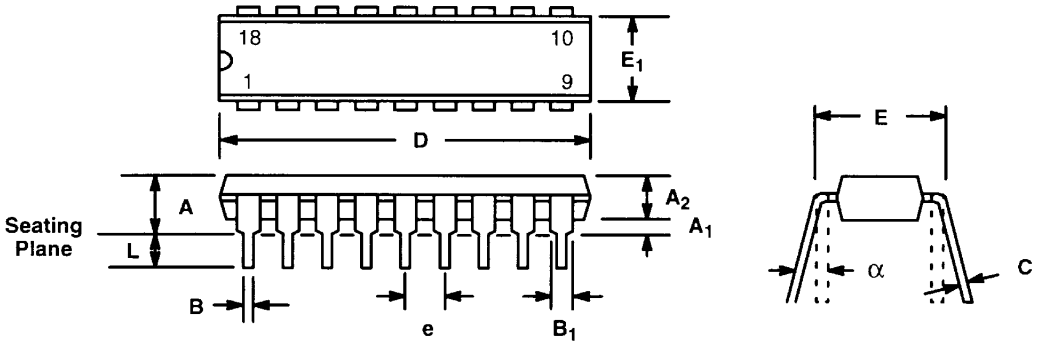


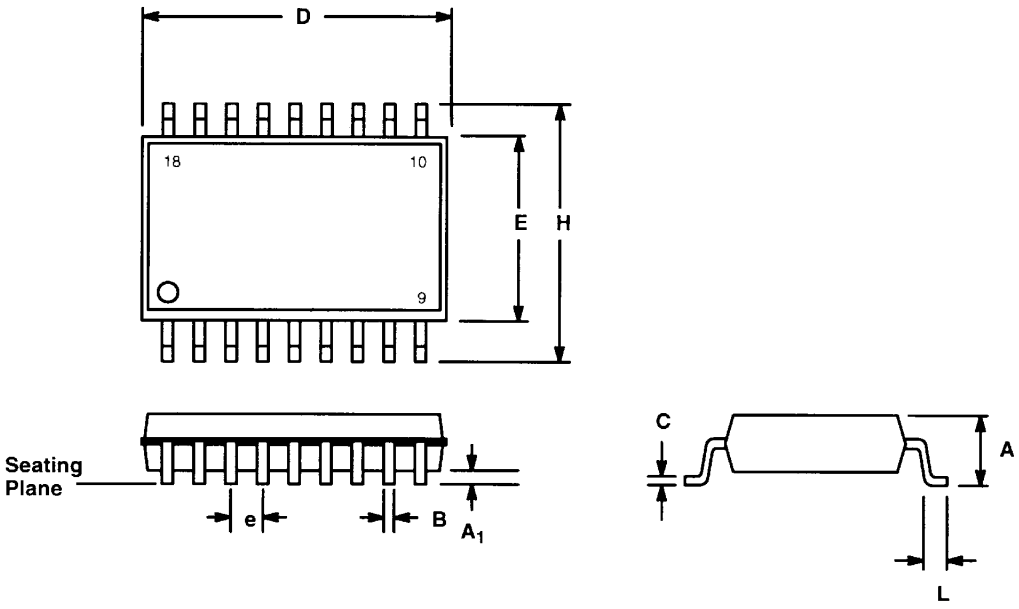
Figure 7. Transmit Clock Timing

18 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)



SYMBOL	INCHES	
	MIN	MAX
A	0.145	0.210
A_1	0.015	0.070
A2	0.115	0.195
B	0.014	0.024
B_1	0.030	0.070
C	0.008	0.016
D	0.845	0.925
E	0.300	0.325
E_1	0.240	0.280
e	0.100 BSC	
L	0.115	0.160
α	0°	15°

18 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A_1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.447	0.463	11.35	11.75
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

Notes

Notes

NOTICE

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Data Sheet March 1996