November 1994-3

Low Power Repeater/Receiver

GENERAL DESCRIPTION

The XR-T56L22 is a very low power monolithic repeater/ receiver IC designed for PCM carrier systems operating between 1.544 Mbps and 2.37 Mbps. The IC provides all the active circuitry required to implement one side of a PCM repeater. The XR-T56L22 features on chip adjustable phase shifting, an extracted clock output and an on-board shunt regulator. The very low power consumption of the device makes it ideal for long haul “tandem” repeater applications.

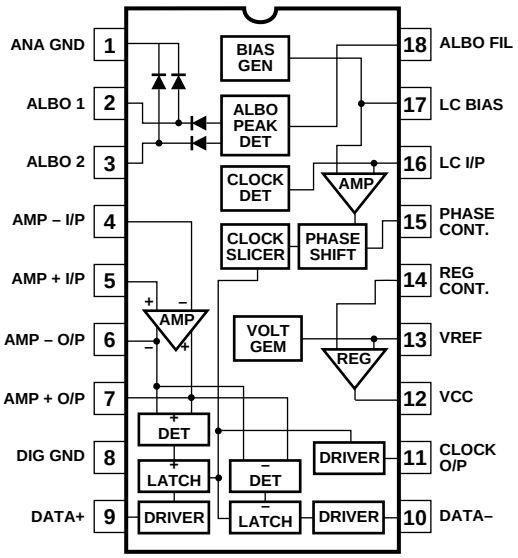
FEATURES

Contains All The Active Components For A Long Haul PCM Repeater Or Receiver
Low Voltage Operation (5.1V)
Low Power Consumption (8.75mA Max)
2 Mbps Operation Capability
Dual Matched ALBO Ports
Internal Adjustable Phase Shift Circuitry
Extracted Clock Output
Internal Shunt Regulator
Temperature Independent Current Biasing

APPLICATIONS

T1 PCM Repeater/Receiver
T148C PCM Repeater/Receiver
European 2.048 Mbps PCM Repeater/Receiver
Digital Multiplexers, CSU’s, Switching Equipment
ISDN Compatible Equipment: Fax Machines, Computers etc.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Operating Temperature	–40°C to +85°C
Supply Voltage	–0.5 to 7V
Supply Voltage Surge (10ms)	+25V
Data Output Voltage (Pin 9, 10)	+12V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T56L22AP	Plastic	–40°C to +85°C
XR-T56L22AN	Ceramic	–40°C to +85°C
XR-T56L22AD	SOIC	–40°C to +85°C

EXAR Corporation, P.O. Box 49007, 2222 Qume Drive, San Jose, CA 95161-9007 · 408/434-6400 · 408/943-8245 (fax)

PIN DESCRIPTION

Pin #	Symbol	Description
1	ANA GND	Ground for analog sections of IC and substrate.
2	ALBO 1	ALBO PORT 1 output. Port impedance varies between 25Ω and 20kΩ proportional to input signal level.
3	ALBO 2	ALBO PORT 2 output. Similar to pin 2.
4	AMP – I/P	Inverting input of signal preamp R_{IN} > 20kΩ.
5	AMP + I/P	Non-inverting input of signal preamp. R_{IN} > 20kΩ.
6	AMP – O/P	Inverting output of signal pre-amp. Rout < 200Ω. DC level typically 3.2V.
7	AMP + O/P	Non-inverting output of signal preamp. Similar to pin 6.
8	DIG GND	Ground for digital portion of IC.
9	DATA+	Positive data driver output (open collector). V_{OL} < 0.95V @ I_{OUT} = 32mA.
10	DATA–	Negative data driver output (open collector). V_{OL} < 0.95V @ I_{OUT} = 32mA.
11	CLOCK O/P	Phase shifted clock output (open collector). Decouple to GND with 0.1µF if not required. With $R_{pull-up}$ = 1K, V_{OL} < 1.1V @ Iout = 4mA.
12	V_{CC}	Input pin of shunt regulator and supply pin for IC. For voltage feed applications the regulator must be disabled and a 5V ± 5% supply connected. For line feed a current of 48-120mA is required. I_{CC} < 8.75mA @ R_{ON}, ALBO = 25Ω typical.
13	V_{REF}	Output voltage of internal reference of shunt regulator. For parallel operation of regulators should be tied to pin 13 of 2nd T56L22 device. V_{REF} approxi-mately V_{CC}/2. Decouple to GND with 0.1µF.
14	REG CONT	Input voltage of shunt regulator amp. To inhibit regulator, pin should be tied to ground. For line feed operation decouple to GND with 0.1µF. For parallel operation of regulators tie pin 14 of 2nd T56L22 device. V_{REG} approximately V_{REF}.
15	PHASE CONT	Phase shift adjust input. A resistor to GND from the pin allows adjustment of phase shift from 90° to approximately 0°. R_P typical 1.8K to 1K. V_{phase} typical 340mV.
16	LC I/P	Clock amplifier input. Pulsed with current from clock comparator. Connect LC tank between 16, 17 for clock recovery. I_{ckon} = –110µA typical.
17	LC BIAS	Clock amplifier reference volt-age. VLC = 3.6V typical.
18	ALBO FIL	Control pin for ALBO ports. Voltage developed across a capacitor on this pin defines ALBO on impedance V_{ALBO} = 1.5V typical.

ELECTRICAL CHARACTERISTICS

Test Conditions: –40°C to +85°C, V_{CC} = 5.1V ± 5%, unless otherwise specified — refer to test circuit (Fig 6).

PARAMETERS	PIN	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL						
Supply Voltage	12	4.85		5.35	V	Pin 12,13 to V_{CC}, Note 1
Supply Current	12		7	8.75	mA	
Data Output Leakage Current	9,10			100	µA	$V_{pull\text{-}up}$ = 8V V_{CC} = 5.35V, Note 1
ALBO Port Off Voltage	2,3			0.1	V	
Amplifier Pin Voltage	4,5 6,7	2.7	3.2	3.7	V	

Note: 1) Internal Regulator disabled.

AMPLIFIER						
Input Impedance	4,5	40			KΩ	
Input Offset Voltage	4,5	–10		+10	mV	R_S = 8.2K, Note 1
Input Bias Current	4,5			5	µA	"
Input Offset Current	4,5	–1		+1	µA	"
Output Offset Voltage	6,7	–50		+50	mV	"
Common Mode Rejection Ratio	4,5,6,7	40			dB	
Output Voltage Swing	6,7	1.9			V	

Note: 1) Source Resistance

CLOCK AMPLIFIER						
Input Offset Voltage	17,16	0.5		6	mV	R_S = 10K, Note 1
Input Bias Current	17,16			5	µA	Note 2
AC Gain		40			dB	
–3dB Bandwidth		10			MHz	
Delay			35		nS	

Notes: 1) R_S = Source resistance Pin 16 positive with respect to Pin 17

2) Pin 16 = Pin 17 = 3.6V

ALBO						
ALBO Filter Resistance	18-1	31		57	KΩ	
ALBO Impedance Match	2,3			10	%	
On Current	1	1.3		2.4	mA	
Drive Current	18	0.4		1.4	mA	
Maximum On Impedance	2,3-1			25	Ω	Note 1
Minimum Off Impedance	2,3-1	20			KΩ	"

Note: *1) f_{test} = 1MHz*

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = –40°C to +85°C, V_{CC} = 5.1V ± 5% unless otherwise specified — refer to test circuit (Fig 6).

PARAMETERS	PIN	MIN	TYP	MAX	UNIT	CONDITIONS
THRESHOLD VOLTAGES						
ALBO Threshold +Ve	7,6	1.4		1.6	V	Notes 1 & 2
ALBO Threshold -Ve	7,6	1.4		1.6	V	Notes 1 & 2
ALBO Threshold Difference		–3		+3	%	Note 3
Clock Drive on Current +Ve		80		140	µA	Note 4
Clock Drive on Current -Ve		80		140	µA	Note 4
Clock Drive Difference		–3		+3	%	Note 3
Clock Threshold +Ve	7,6	69		79	%	Note 5
Clock Threshold -Ve	7,6	69		79	%	Note 5
Clock Threshold Difference		–3		+3	%	Note 3
Data Threshold +Ve	7,6	41		50	%	Note 5
Data Threshold -Ve	7,6	41		50	%	Note 5
Data Threshold Difference		–3		+3	%	Note 3

Notes: 1) Pk/pk voltage at Pins 6 and 7 of a 1MHz sine wave derived through amplifier and measured differentially.

2) Pk/pk voltage at Pins 6 and 7 adjusted for a current increase of 2mA at pin 1.

3) Calculation only: percentage difference $= \left[\frac{\text{higher value}}{\text{lower value}} \right] - 1 \times 100\%$

4) $V_6 - V_7$ adjusted to ALBO threshold voltage (Pin 16 = 3.6V)

5) Figure taken as a percentage of ALBO threshold

DATA OUTPUT STAGES						
Output Pulse Rise Time +Ve (Tr)	9			40	nS	10%-90% Note 1
Output Pulse Rise -Time –Ve (Tr)	10			40	nS	"
Output Pulse Fall Time +Ve (Tf)	9			40	nS	"
Output Pulse Fall Time –Ve (Tf)	10			40	nS	"
Output Pulse Width +Ve (Tw)	9	224		264	nS	at 50%
Output Pulse Width –Ve (Tw)	10	224		264	nS	"
Output Pulse Width Difference (dTw)		–12		+12	nS	"
Output Voltage (low) (V_{OL})	9,10	0.6		0.95	V	Note 1
Output Voltage Difference (V_{OL})	9,10	–0.15		+0.15	V	"

Note: 1) Using a 130Ω pull up resistor between 9, 10 and V_{CC} and 15pF capacitance to GND.

CLOCK OUTPUT STAGE						
Output Pulse Rise Time (Tr)	11			40	nS	Note 1
Output Pulse Fall Time (Tf)	11			40	nS	
Output Pulse Width (Tw)	11	224		264	nS	
Output Voltage Low (V_{OL})	11			1.1	V	

Note: 1) Using a 2K pull up resistor between 11 and Vcc and 15pF capacitance to GND.

SHUNT REGULATOR						
Output Voltage	12	4.85	5.1	5.35	V	Pin 13, 14 floating
Voltage Regulation Over Temp.	12		–0.02		%/°C	"
Load Regulation	12			0.027	%/mA	1mA to 100mA load

SYSTEM DESCRIPTION

With reference to the functional block diagram, the basic operation of the XR-T56L22 may be described as follows: The received bipolar signal, is applied to a linear amplifier and automatic equalizer. These circuits provide the necessary amount of gain and phase equalization to recover the transmitted data, and band limit the signal, to optimize repeater performance for near-end crosstalk produced by other systems operating within the same cable bundle.

The preamplifier output signals which are balanced and of opposite phase, are applied to the clock extraction and pulse regenerator circuits. Here they are rectified and then applied to a high Q resonant circuit which extracts the 1.544/2.048 Mbps frequency component from the received signal. This signal is then sliced and fed to an adjustable phase shift circuit. A second slicer is used to control the time at which the output signals from the preamplifier are sampled by the pulse regenerator circuits. The phase shifted clock signal is made available as an output from the circuit for interface applications. The clock phase adjustment is performed with a single pin using an external resistor. Adjustment of the position of the clock sampling edge by the phase shift circuit allows performance of the pulse regenerator to be optimized. The pulse regenerator performs the sampling and data slicing to regenerate the appropriate output pulse. These pulses are applied to an external output transformer to create the bipolar signal that drives the next section of twisted pair.

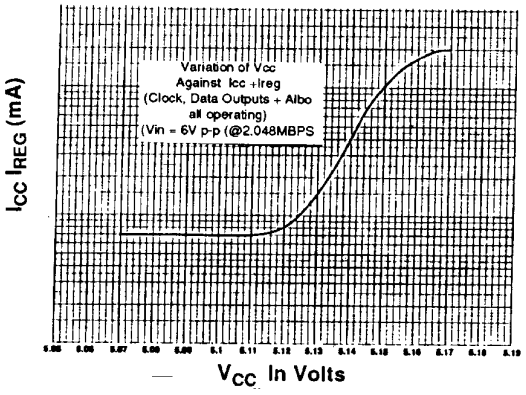


Figure 1. Regulator Output Voltage Versus Current (I_{CC} + I_{REG})

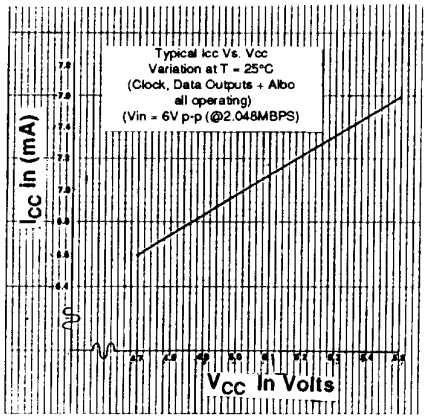


Figure 2. Supply Current Variation with V_{CC} (Regulator Inhibited)

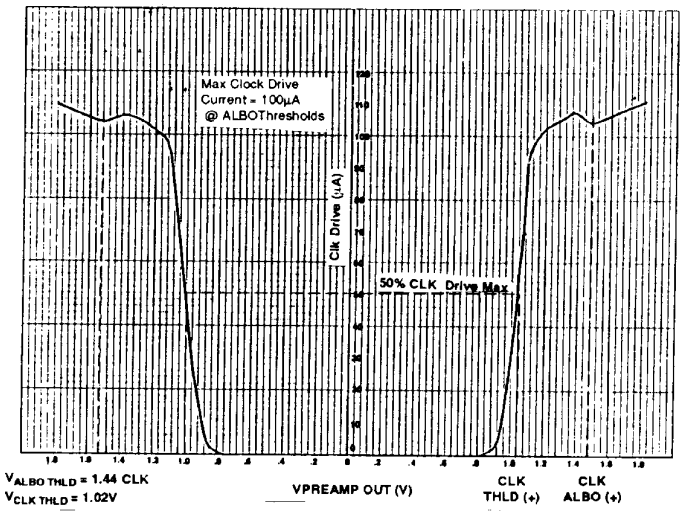


Figure 3. Clock Drive Current Against Preamp Output Voltage

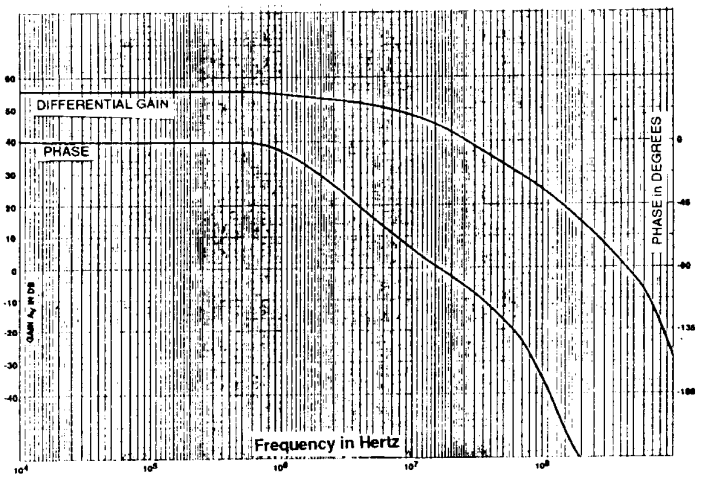


Figure 4. Preamp Gain/Phase Characteristics

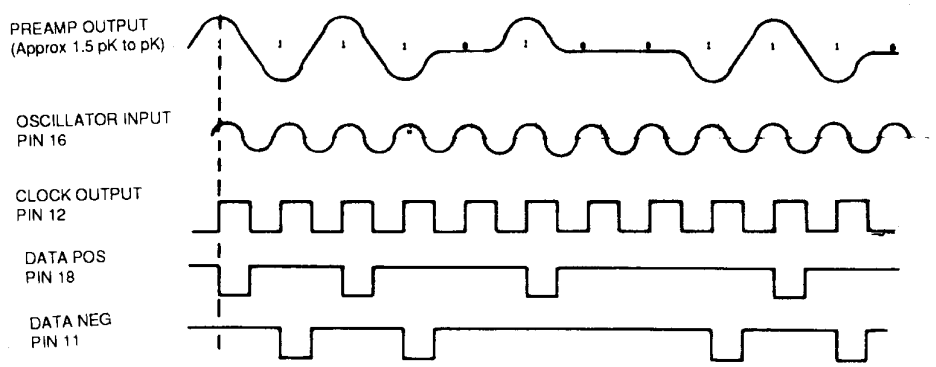


Figure 5. Typical T56L22 Waveforms

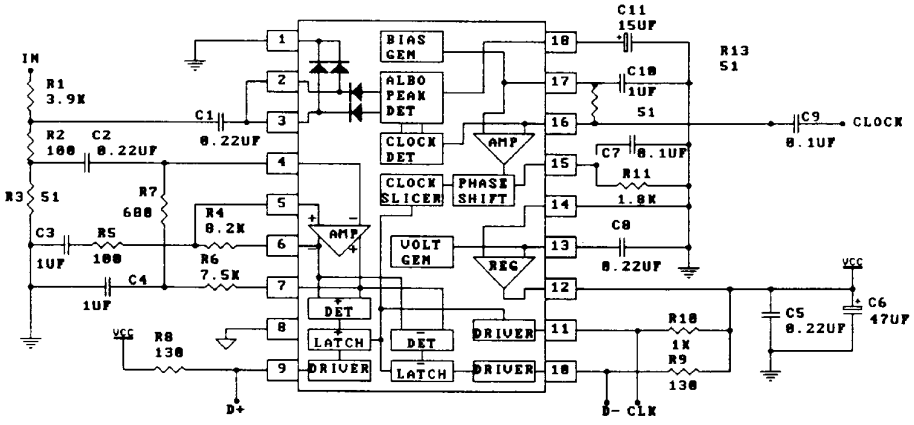
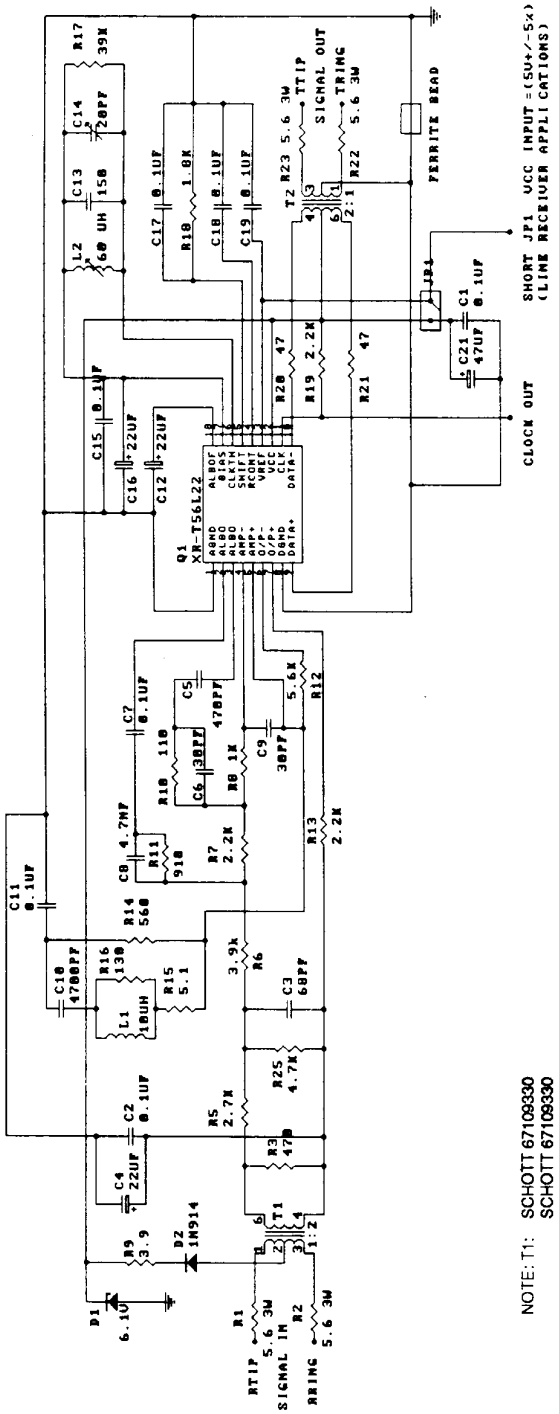
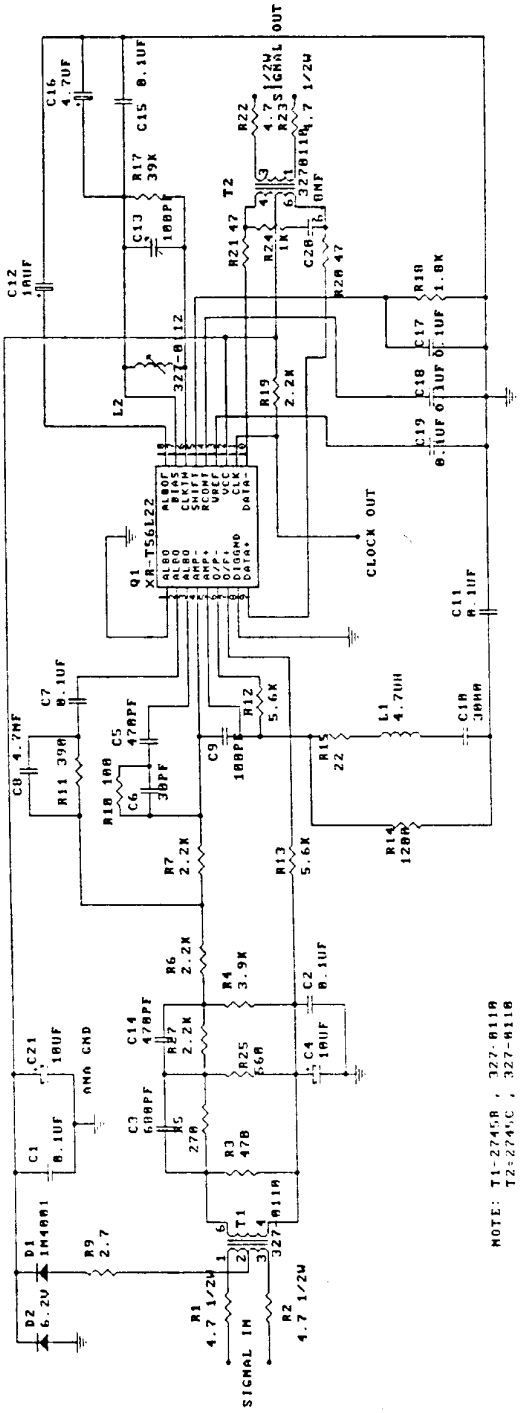


Figure 6. AC Parameter Test Circuit



Typical Application for the XR-T56L22 at 1.544 MBPs.



Typical Application for the XR-T56L22 at 1.544 MBPs..

Notes