January 1995-2

Low Power T1 Analog Interface

GENERAL DESCRIPTION

The XR-T5684 is a fully integrated PCM line transceiver intended for DSX-1 digital cross-connect applications. It combines both transmit and receive circuitry in a 28 pin PLCC or PDIP package. The receiver extracts data from AMI coded input signal, and outputs synchronized clock and unipolar RPOS and RNEG data by means of an external 8X or 16X oversampling clock. The oversampling clock is necessary only for application where the clock recovery feature is required. The transmitter of the device pre-shapes the transmit pulse internally, providing the appropriate pulse shape at the cross-connect for line lengths ranging from 0 to 655 feet.The XR-T5684 is manufactured using advanced CMOS technology and requires only a single +5V power supply.

FEATURES

Fully Integrated T1 Transceiver
Low Power Consumption (normally 225 mW)
Recovered Data and Clock Outputs
Driver Performance Monitor
Internal Transmit LBO for Line Lengths Between 0 to 655 Feet
Compliance with TR-TSY-000499, 43802 and 43801 Input Jitter Tolerance Specifications

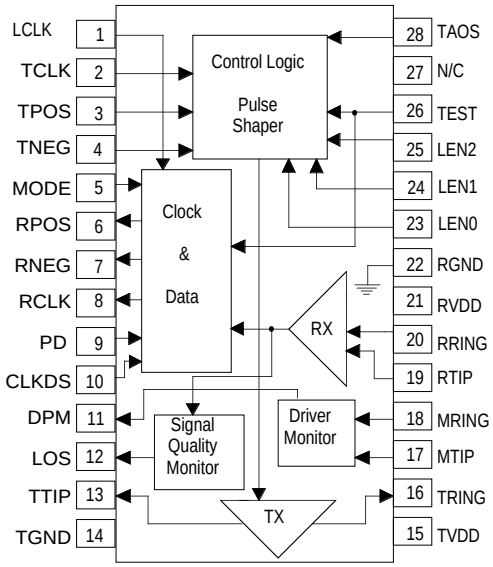
APPLICATIONS

Interfacing T1 Network Equipment such as Multiplexors, Channel Banks and DSX-1 Switching Systems.
Interfacing Customer Premises Equipment such as CSUs, PBX's, T1 Measurement and Test Equipment.

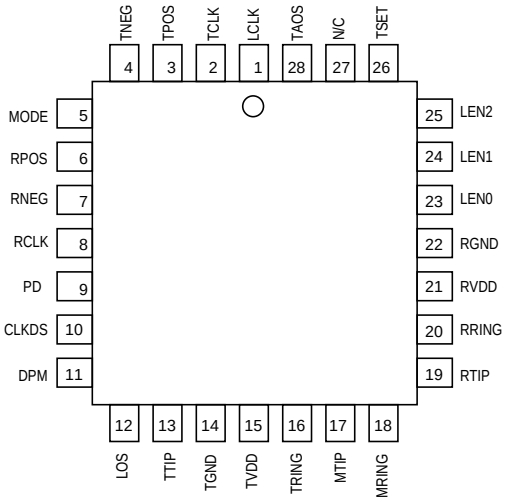
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (continuous)	-0.5 to +7V
Supply Current (continuous)	20mA to -20mA
Storage Temperature	-65°C to +150°C

PIN ASSIGNMENT



PDIP Package



PLCC Package

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5684IJ	28 pin PLCC	-40 to + 85°C
XR-T5684IP	28 pin PDIP	-40 to + 85°C

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PIN DESCRIPTION

Pin No.	Symbol	Type	Description
1	LCLK	I	**Oversampling Clock**. 8X or 16X input clock for receive clock recovery circuit. 8X=12.352MHz+/-200ppm with pin 9 set to low. 16X=24.704MHz+/-200ppm with pin 9 set to high.
2	TCLK	I	**Transmit Clock**. T1=1.544MHz+/-50ppm.
3	TPOS	I	**Transmit Positive Data.** A positive NRZ data on this pin causes a positive pulse to be transmitted on TTIP. TPOS is sampled on the falling edge of TCLK.
4	TNEG	I	**Transmit Negative Data.** A positive NRZ data on this pin causes a negative pulse to be transmitted on TRING. TNEG is sampled on the falling edge of TCLK.
5	MODE	I	**Receive Output Data Select**. With this pin set to high, the extracted data at RPOS and RNEG are re-timed using the recovered clock RCLK. With this pin set to low, the received data have no relation to RCLK and are typically stretched by 80nS before being sent to the output. This pin is pulled down internally.
6	RPOS	O	**Receive Positive Data Output.** A positive pulse on this pin corresponds to a positive pulse on RTIP.
7	RNEG	O	**Receive Negative Data Output.** A positive pulse on this pin corresponds to a positive pulse on RRING.
8	RCLK	O	**Receive Clock Output**. Recovered clock using oversampling clock applied to pin 1.(see MODE select of pin 5 and PD of pin 9).
9	PD	I	**Programmable Divider.** The state of this pin determines the oversampling clock applied to pin 1. When LCLK=16X1.544MHz, set PD to high. When LCLK=8X1.544MHz, set PD to low. This pin is pulled down internally.
10	CLKDS	I	**Clock Disable.** With this pin set to high, the recovered clock at pin 8 is disabled. This function is provided for applications where upon input data loss, the output clock can be inhibited by connecting LOS to CLKDS externally. This pin is pulled down internally.
11	DPM	O	**Driver Performance Monitor.** Used as an early warning signal on non-functioning T1 links. If no signal is present on MTIP and MRING for 63 clock cycles. DPM goes high until a next pulse is detected.

Pin No.	Symbol	Type	Description
12	LOS	O	**Loss of Signal.** This pin goes high either when the input signal at RTIP and RRING drops to below 0.4V peak or after 175 zeros are detected. The 175 zeros detection is active only when LCLK is applied.
13	TTIP	O	**Transmit Positive Data**. Transmit AMI signal is driven to the line via a step-up transformer from this pin.
14	TGND	—	**Transmitter Supply Ground**. This pin can be connected to RGND externally.
15	TVDD	—	**5 V +/-5%** Transmitter Supply.
16	TRING	O	**Transmit Negative Data**. Transmit AMI signal is driven to the line via a step-up transformer from this pin.
17	MTIP	I	**Driver Performance Monitor Input.** This pin is normally connected to TTIP for monitoring the driver's activity. It is pulled high internally.
18	MRING	I	**Driver Performance Monitor Input.** This pin is normally connected to TRING for monitoring the driver's activity. It is pulled high internally.
19	RTIP	I	**Receive Tip Input.** The AMI receive signal is input to this pin via a centre-tapped transformer.
20	RRING	I	**Receive Ring Input.** The AMI receive signal is input to this pin via a centre-tapped transformer.
21	RVDD	—	**5 V +/-5% Receive Supply.** This pin can be connected to TVDD externally.
22	RGND	—	**Receive Supply Ground.** This pin is also connected to the substrate of the device.
23	LEN0	I	**Pulse Shaper Select Pin**. Least significant bit.
24	LEN1	I	**Pulse Shaper Select Pin**. Second significant bit.
25	LEN2	I	**Pulse Shaper Select Pin**. Most significant bit.
26	TEST	I	**Factory Test Pin.** This pin must be grounded for normal operation.
27	N/C	—	**No Connection Pin.** This pin can be grounded or left floating.
28	TAOS	I	**Transmit All Ones Select.** Setting TAOS high causes continuous AMI ones to be transmitted to the line at the frequency set by TCLK.

PIN DESCRIPTIONS *(continued)*
SYSTEM DESCRIPTION

The device consists of receiver and transmitter circuitry with separate power supplies to reduce crosstalk between the two sections.

RECEIVER

The receiver is sensitive to the entire cable length from the cross-connect and requires no external equalization networks. The receive AMI input signal is applied to RTIP and RRING through a center-grounded transformer. The positive pulse is input to RTIP and the negative pulse is input to RRING.

Comparators are used to slice the data on RTIP and RRING. The slicing level of the comparators are dynamically set at around 70% of peak level of the input signal to ensure optimum signal-to-noise ratio. With Mode Select (pin 5) set to low, the clock recovery feature is bypassed and the output data from the comparators are typically stretched by 80nS before output to RPOS and RNEG respectively.

A positive data at RPOS corresponds to a positive pulse received at RTIP and a positive data at RNEG corresponds to a positive pulse received at RRING.

With Mode Select (pin 5) set to high and an oversampling clock applied to pin 1, the recovered data can be synchronized with RCLK at pin 8. The clock recovery circuit extracts the timing contents from the incoming data transitions by means of an 8X or 16X divider. If there is no data on the input, the divider operates in its free running mode, generating a equal mark-and-space ratio output clock. This free running mode will be interrupted if a positive pulse is detected; the resultant mark-and-space ratio of the output clock is then determined by the position of the occurrence of the positive data relative to its free running position. See timing diagram in Figure 1 and Figure 2.

In all cases, the output data RPOS and RNEG remains stable on the falling edge of RCLK so as to be sampled correctly. The input jitter tolerance with an 8X oversampling clock is shown in Figure 3 and that with a 16X oversampling clock is shown in Figure 4.

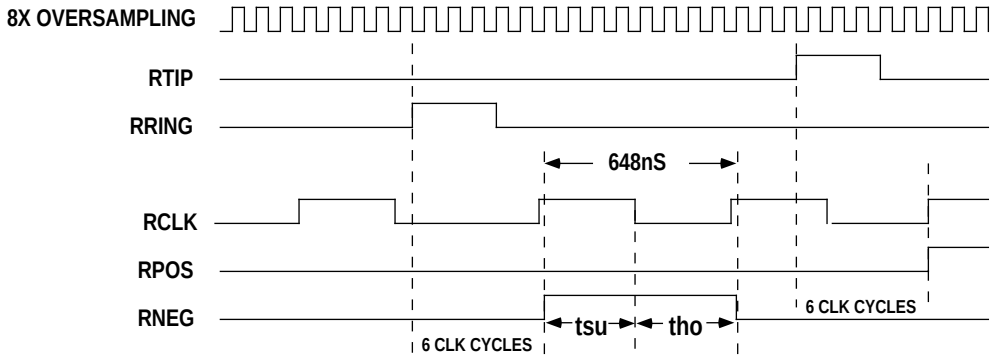


Figure 1. Typical Receive Timing Diagram Using 8X Oversampling Clock.

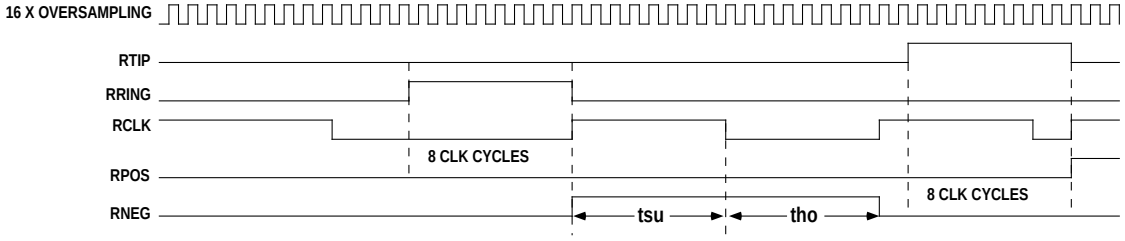


Figure 2. Typical Receive Timing Diagram Using 16X Oversampling Clock.

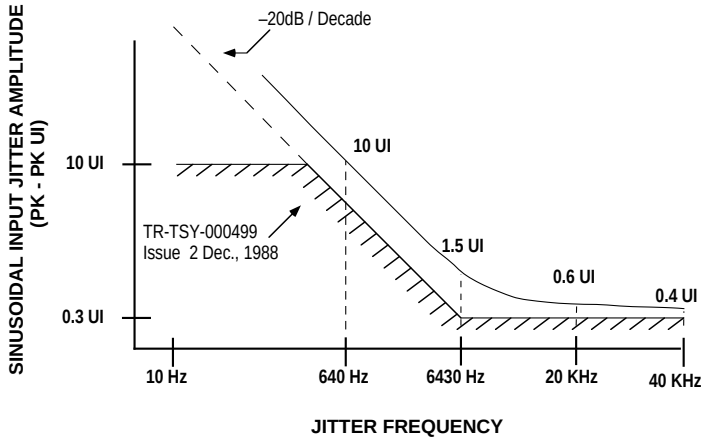


Figure 3. XR-T5684 Input Jitter Tolerance Using 8X Oversampling Clock.

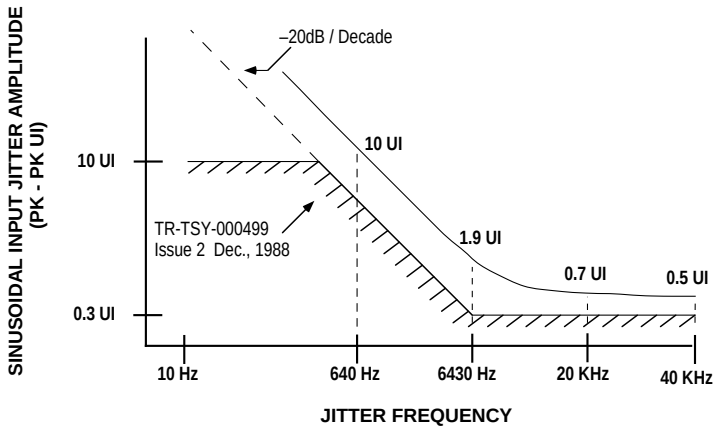


Figure 4. XR-T5684 Input Jitter Tolerance Using 16X Oversampling Clock.

Another function of the receiver is the signal quality monitor that reports loss of signal when the input level on RTIP and RRING falls below 0.4V or upon detection of 175 +/- 15 consecutive zeros in the incoming data stream. The zero detection circuit is active only when LCLK clock is applied. In both cases, the receiver reports loss of signal by setting LOS high, and at the same time, RPOS and RNEG are forced to low. Under the loss of signal conditions, the receiver will continue to recover data and will return to its normal operation if a valid data is detected on RTIP and RRING.

TRANSMITTER

The transmitter is designed to take dual rail NRZ data, plus a synchronized input clock and produces a bipolar signal with the appropriate shape for transmission to the line.

After sampling by the falling edge of TCLK, TPOS and TNEG data are processed by a digital to analog converter together with a slew-control circuit to generate output pulses at TTIP and TRING with the appropriate amplitude and shape to meet the cross-connect template specified in CB 119. A typical output pulse is shown in Figure 5. In order to meet the amplitude requirement with a single +5V supply, the transmit signal is driven to the line differentially via a 1:1.36 step-up transformer.

Pulse shaping is selectable through input control pins LEN2, LEN1 and LEN0 for line lengths ranging from 0 to 655 feet of ABAM cable as illustrated in Table 1.

LEN2	LEN1	LEN0	Line Length Selected (ft.)
0	1	1	0-133
1	0	0	133-266
1	0	1	266-399
1	1	0	399-533
1	1	1	533-655

Table 1. ABAM or ALVYN Cable Type Line Length Selection

The transmitter can be set to transmit a continuous AMI encoded all ones signal to the line by forcing TAOS high. In this mode, input data TPOS and TNEG are ignored and the frequency of the transmitted signal is determined by TCLK.

With TTIP connected to MTIP and TRING connected to MRING, the driver monitor can detect a non-functional T1 transmitter by monitoring the activity at its input. If no signal is presented on MTIP and MRING for 63 TCLK clock cycles, DPM goes high until the next AMI signal is detected.

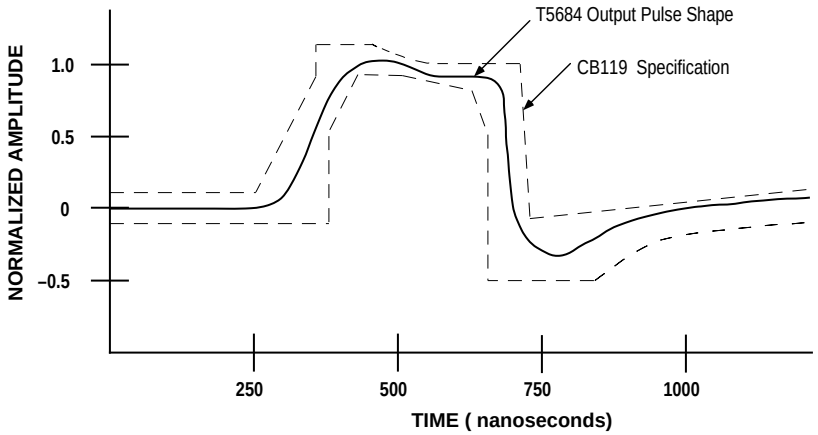


Figure 5. Typical Output Pulse at DSX-1 Cross-connect.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = -40 to + 85°C, RVDD and TVDD = 5V+/-5%, RGND and TGND = 0V.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
RECOMMENDED OPERATING CONDITIONS						
VDD/TVDD	DC Supply Voltage	4.75	5	5.25	V	
PD	Total Power Dissipation			400	mW	100% ones density & max. line length @ 5.25V and with 16X oversampling clock running.
PD	Normal Power Dissipation		225		mW	50% ones density & 300ft. line length @5.0V and with over - sampling clock disabled.
INPUTS						
VIH	High Level Input (Note 1)	2.0			V	
VIL	Low Level Input (Note 1)			0.8	V	
IIL	Input Leakage Current			±10	µA	Pins = TCLK, TPOS, TNEG, LEN0/1/2.
OUTPUTS						
VOH	High Level Output (Note 2)	2.4			V	
VOL	Low Level Output (Note 2)			0.4	V	

Note 1: All input pins except RTIP, RRING, MTIP and MRING.

Note 2: All output pins except TTIP and TRING.

ANALOG SPECIFICATIONS

Test Conditions: TA= -40 to +85°C, RVDD and TVDD = 5V+/-5%, RGND and TGND = 0V.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
VPA	AMI Output Pulse Amplitudes	2.4	3.0	3.6	V	Measured at DSX-1 using a 1:1.36 step up transformer with all line length select as shown in Table1.
TXJA	Jitter added by the transmitter					
	10Hz - 40KHz (Note 3)	—	0.025	—	UI	
	Broad Band (Note 3)	—	0.05	—	UI	
RXS	Receiver Sensitivity Below DSX(0dB=2.4V)	6	—	—	dB	
RLOS	Receiver Loss of Signal Threshold	—	0.4	—	V	
	Number of consecutive zeros before LOS	160	175	190	—	
RTH	Receiver Data Slicing Threshold	—	70	—	% of peak	

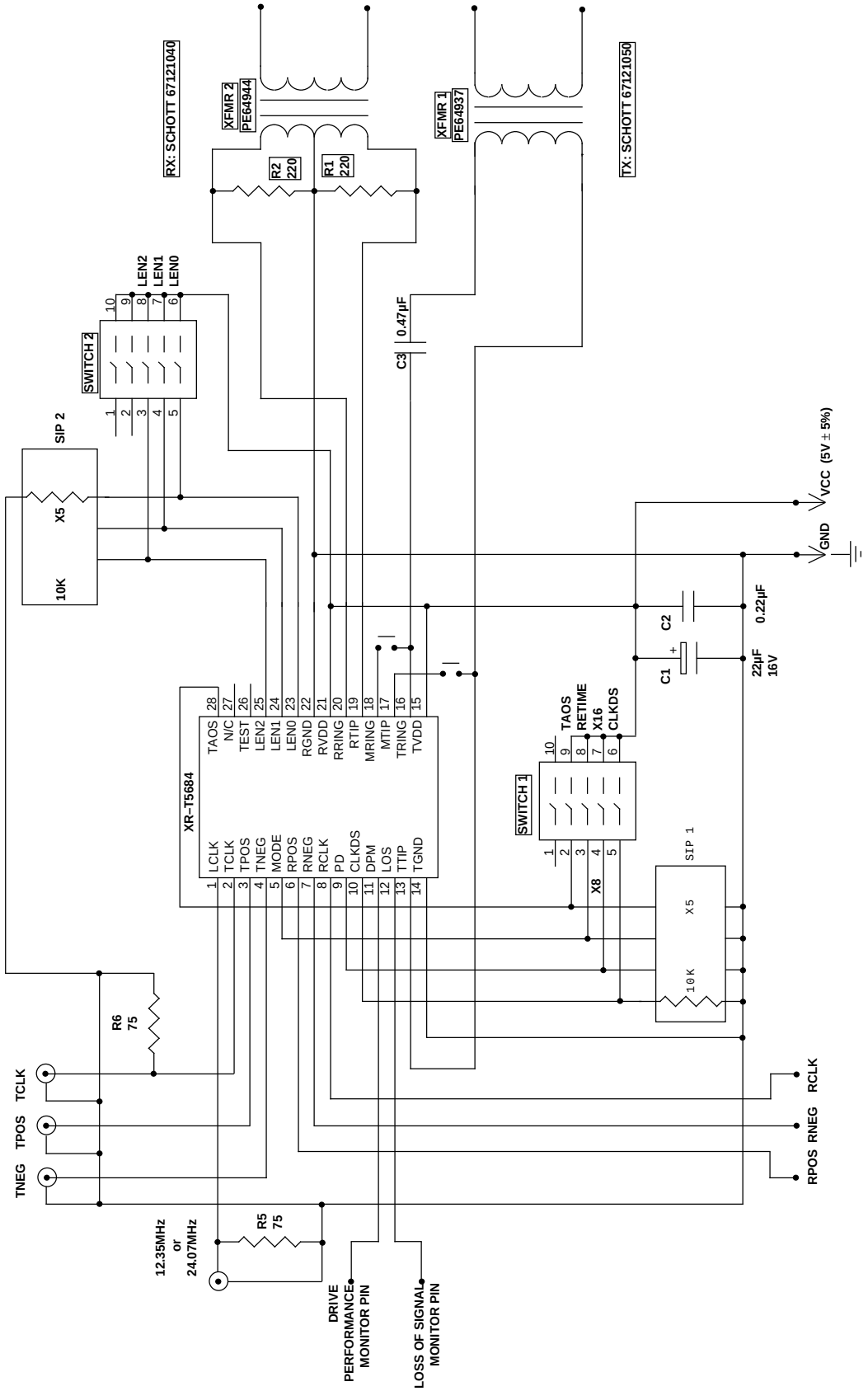
Note 3 : Input clock to TCLK is jitter free.

AC CHARACTERISTICS

Test Conditions: TA = -40 to + 85°C, RVDD and TVDD = 5V+/-5%, RGND and TGND = 0V.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
TCLKf	Clock Frequency		1.544		MHz	
	TCLK Clock Duty Cycle	40	50	60	%	
LCLKf	Frequency 8X		12.352		MHz	
LCLKf	16X		24.704		MHz	
	LCLK Clock Tolerance	—	—	+/-200	ppm	
	LCLK Clock Duty Cycle	35	50	65	%	
tsu	TPOS/TNEG to TCLK setup time	25	—	—	ns	
tho	TCLK to TPOS/TNEG hold time	25	—	—	ns	
tdr	RTIP/RRING Rising to RPOS/RNEG Rising (Note 4)	15	30	120	ns	
tdf	RTIP/RRING Falling to RPOS/RNEG Falling (Note 4)	60	120	250	ns	
	RCLK Duty Cycle	—	50	—	%	
tsu	RPOS/RNEG to RCLK Falling setup time	—	300	—	ns	
tho	RCLK Falling to RPOS/ RNEG hold time	—	324	—	ns	

Note 4. Pin 5 Set to Low .



Application Schematic Diagram

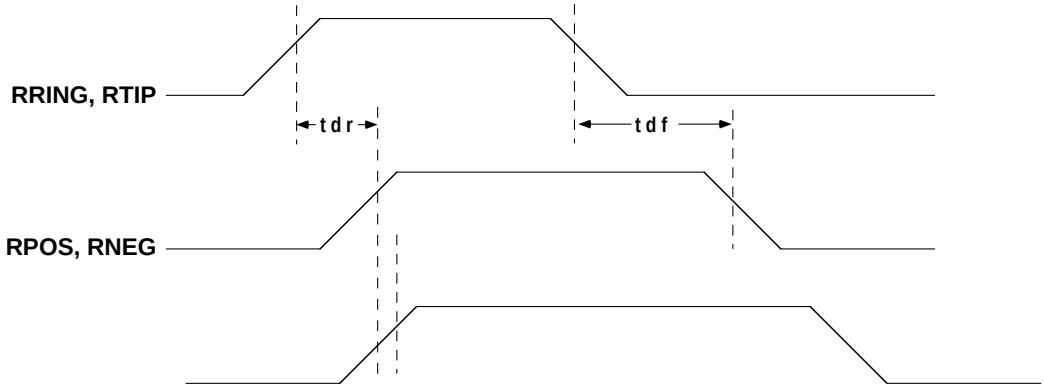


Figure 6. Receiver Clock and Data Switching Characteristics

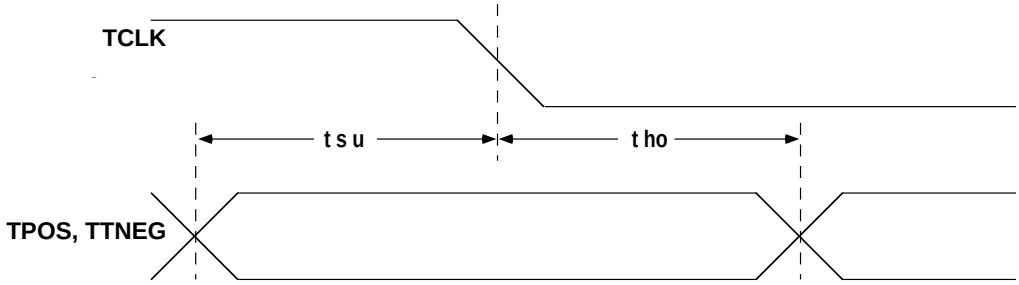


Figure 7. Transmit Clock and Data Switching Characteristics

Notes

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Data Sheet January 1995