May 1996-2

PCM Line Interface Chip

GENERAL DESCRIPTION

The XR-T5683A is a PCM line interface chip. It consists of both transmit and receive circuitry in a device. This device is offered in dual in-line plastic or in a surface mount package. The maximum bit rate the chip can handle is 8.448 M Bits/s and the signal level to the receiver can be attenuated by –10dB cable loss at half the bit rate. At nominal supply voltage operation, the typical current consumption is 40mA.

FEATURES

- Single 5V Supply
- Receiver input can be either balanced or unbalanced
- Up to 8.448 M Bits/s operation in both Tx and Rx directions
- TTL Compatible interface
- Device can be used as a line interface unit without clock recovery

APPLICATIONS

T1, T2, E1 & E2 rates, PCM Line Interface
Network multiplexing and terminating equipment

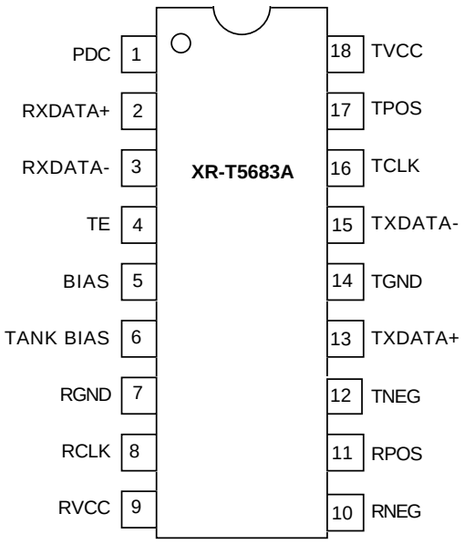
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+20V
Storage Temperature	-65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5683AIP	PDIP	-40°C to +85°C
XR-T5683AID	SOIC	-40°C to +85°C

PIN ASSIGNMENT



Note: *Pin assignment is for DIP and SOIC packages*

SYSTEM DESCRIPTION

The incoming bipolar PCM signal which is attenuated and distorted by the cable is applied to the threshold comparator and the peak detector. The peak detector generates a DC reference for the threshold comparator for data and clock extraction. An external tank circuit tuned to the appropriate frequency is added for the later operation. The clock signal, data (+) and data (–) all go through a similar level shifter to be converted into TTL level to be compatible for digital processing.

In the transmit direction, the output drivers consist of two identical TTL inputs with open collector output stages. The maximum low level current these output stages can sink is 40 mA. With full width data (NRZ) applied to the inputs together with a synchronized clock, the output will generate a bipolar signal when driving a center-tapped transformer. A block diagram of the XR-T5683A is shown in Figure 1.

The clock recovery uses an external tank circuit. The receive data will create an excitation for the tank circuitry which in turn will create a recovered, received clock (RCLK).

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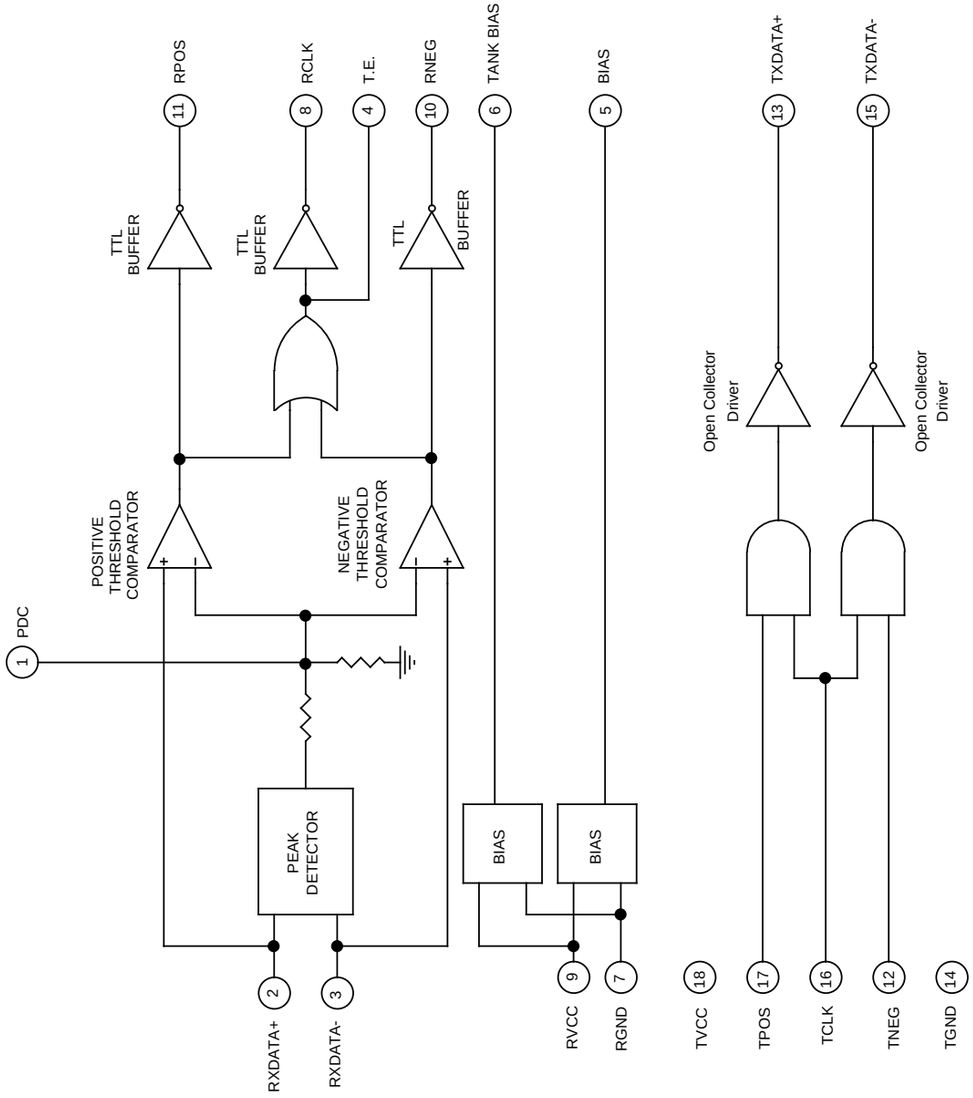

Figure 1. Block Diagram

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	PDC	-	**PEAK DETECTOR CAPACITOR**. This pin should be connected to a 0.1µF capacitor.
2	RXDATA+	I	**RECEIVE ANALOG INPUT POSITIVE**. Line analog input.
3	RXDATA-	I	**RECEIVE ANALOG INPUT NEGATIVE**. Line analog input.
4	T.E.	O	**TANK EXCITATION OUTPUT**. This output connects to one side of the tank circuitry.
5	BIAS	O	**BIAS**. This output is to be connected to the center tap of the receive transformer.
6	TANK BIAS	O	**TANK BIAS**. The tank circuitry is biased via this output.
7	RGND	-	**RECEIVER GROUND**. To minimize ground interference a separate pin is used to ground the receive section.
8	RCLK	O	**RECOVERED RECEIVE CLOCK**. Recovered clock signal to the terminal equipment.
9	RVCC	-	**RECEIVE SUPPLY VOLTAGE**. 5 Volt supply voltage to the receive section.
10	RNEG	O	**RECEIVE NEGATIVE DATA**. Negative pulse data output to the terminal equipment. (Active Low)
11	RPOS	O	**RECEIVE POSITIVE DATA**. Positive pulse data output to the terminal equipment. (Active Low)
12	TNEG	I	**TRANSMIT NEGATIVE DATA**. TNEG is valid while TCLK is high.
13	TXDATA+	O	**TRANSMIT POSITIVE OUTPUT.** Transmit bipolar signal is driven to the line via a transformer.
14	TGND	-	**TRANSMIT GROUND**.
15	TXDATA-	O	**TRANSMIT NEGATIVE OUTPUT**. Transmit bipolar signal is driven to the line via a transformer.
16	TCLK	I	**TRANSMIT CLOCK**. Timing element for TPOS and TNEG.
17	TPOS	I	**TRANSMIT POSITIVE DATA**. TPOS is valid while TCLK is high.
18	TVCC	-	**TRANSMIT SUPPLY VOLTAGE**. +5 Volts.

DC ELECTRICAL CHARACTERISTICS:
Test Conditions**: Vcc = 5.0V** ± 5%, **TA = 25°C**, unless otherwise specified.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
Supply voltage	4.75	**5**	5.25	V	
Supply current		40	**55**	mA	Total current to pin 9 & Pin 18 transmitter outputs open
RECEIVER SECTION					
Tank drive current	**300**	500	**700**	µA	Measured at pin 4, V_{CC} = 5V
Clock output low		0.3	**0.6**	V	Measured at pin 8, I_{OL} = 1.6mA
Clock output high	**3.0**	3.6		V	Measured at pin 8, I_{OH} = -400µA
Data output low		0.3	**0.6**	V	Measured at pin 10 & 11, I_{OL} = 1.6mA
Data output high	**3.0**	3.6		V	Measured at pin 10 & 11, I_{OH} = -400µA
TRANSMITTER SECTION					
Driver output low	**0.6**	0.8	**1.0**	V	Measured at pin 13 & 15, I_{OL} = 40mA
Output leakage current		0	**100**	µA	Measured in off state, Output pull-up to + 20V
Input high voltage	**2.2**		**Vcc**	V	Measured at pin 12, 16 & 17, I_{OL} = 40mA, V_{OL} = 1.0V
Input low voltage			**0.8**	V	Measured at pin 12, 16 & 17, Output off
Input low current			**–1.6**	mA	Measured at pin 12, 16 & 17, Input low voltage = 0. 4V
Input high current			**40**	µA	Measured at pin 12, 16 & 17, Input high voltage = 2.7V
Output low current			**40**	mA	Measured at pin 13 & 15, V_{OL} = 1.0V

Note: *Bold face parameters are covered by production test.*

AC ELECTRICAL CHARACTERISTICS:
Test Conditions: **V_{CC} = 5.0V**, **T_A = 25°C**, unless otherwise specified.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
RECEIVER SECTION					
Input level		6	**6.6**	Vp	Measured between pin 2 & 3
Loss input signal alarm level		1.6		Vpp	Measured between pin 2 & 3, Alarm on pull data output high
Input impedance at 8.448MHz		2.5		kΩ	Measured between pin 2 & 3, with sinewave input
Clock duty cycle	**35**	50	**65**	%	Measured at pin 8 at 2.0V
Clock rise & fall time		20		ns	Measured at pin 8, C_L = 15pF
Data pulse width	**35**	50	**75**	% of clock period	Measured at pin 10 & 11, At 1V DC level, cable loss = 0
TRANSMITTER SECTION					
Pulse width at 8.448M/Hz	**53**		**65**	ns	Measured at pin 13 & 15 See Figure 6
Output rise time		12	**25**	ns	See Figure 7
Output fall time		12	**25**	ns	See Figure 7
Output pulse imbalance		2.5		ns	At 50% output level

Note: *Bold face parameters are covered by production test.*

Table 1 shows typical expected jitter tolerance. The following measurements have been done at a transmission rate of T1 (1.544 MHz). (See Figure 2)

V_{CC}=+5V +/- 5%, T_A=25°C

JITTER	1.544Mbps in UI	JITTER	1.544Mbps in UI
10Hz	>10UI	5KHz	1.3UI
100Hz	>10UI	8KHz	0.8UI
500Hz	>10UI	10KHz	0.7UI
1KHz	6.5UI	32KHz	0.5UI
2KHz	3.3UI	50KHz	0.45UI
3KHz	2.1UI	77KHz	0.45UI
4KHz	1.5UI	-	-

Table 1. Jitter tolerance at 1.544 Mbps with 6db cable loss.

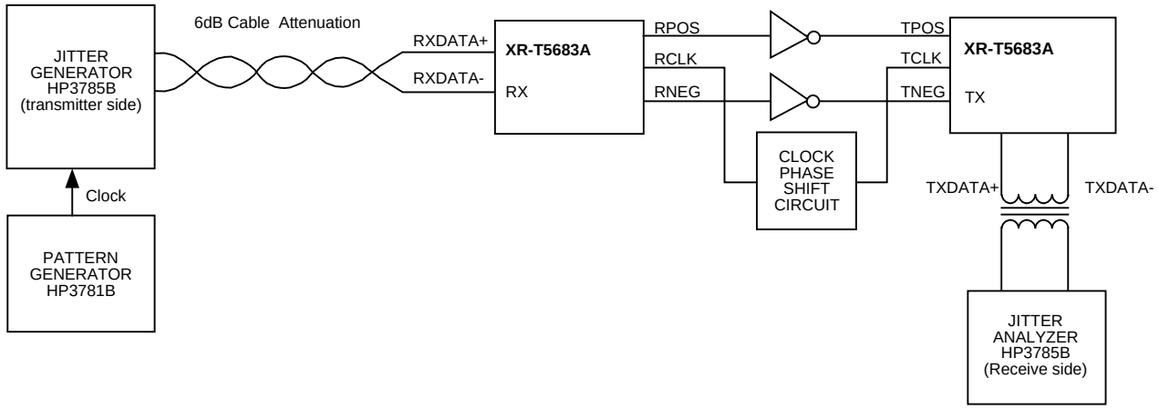

Figure 2. Jitter Measurement Set-up

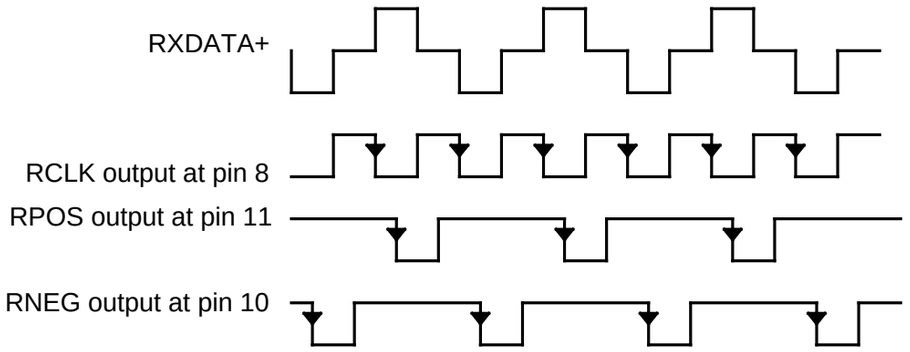

Figure 3. Receiver Timing Diagram with 1-1-1-1-1-1 Pattern

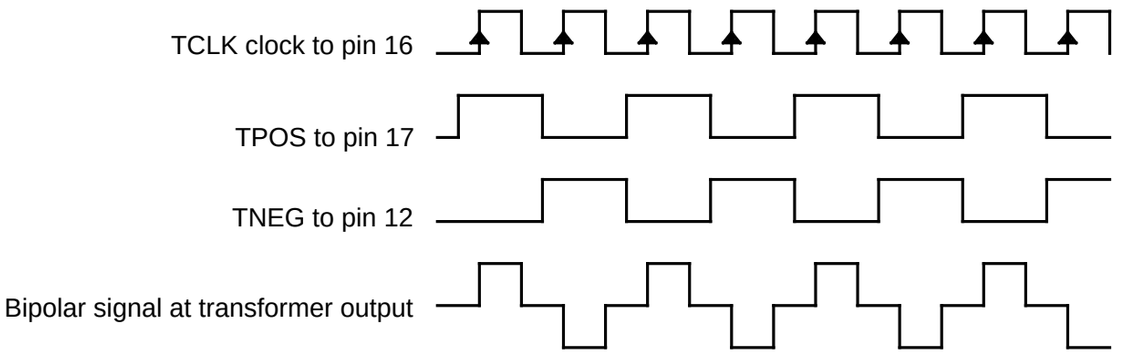

Figure 4. Transmitter Input Timing Diagram

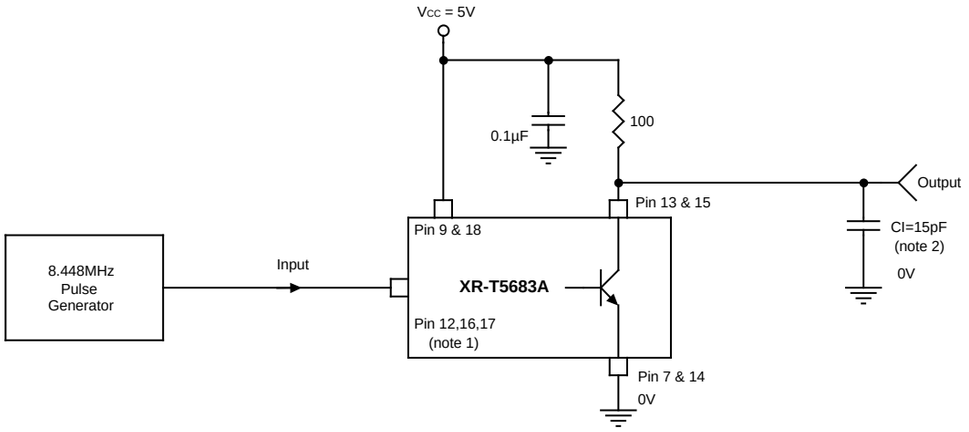

Figure 7. Test Circuit

Note 1. *Inputs that are not connected to pulse generator will be tied to Vcc via 1K resistor*
Note 2. *C1 includes probe and jig capacitance.*

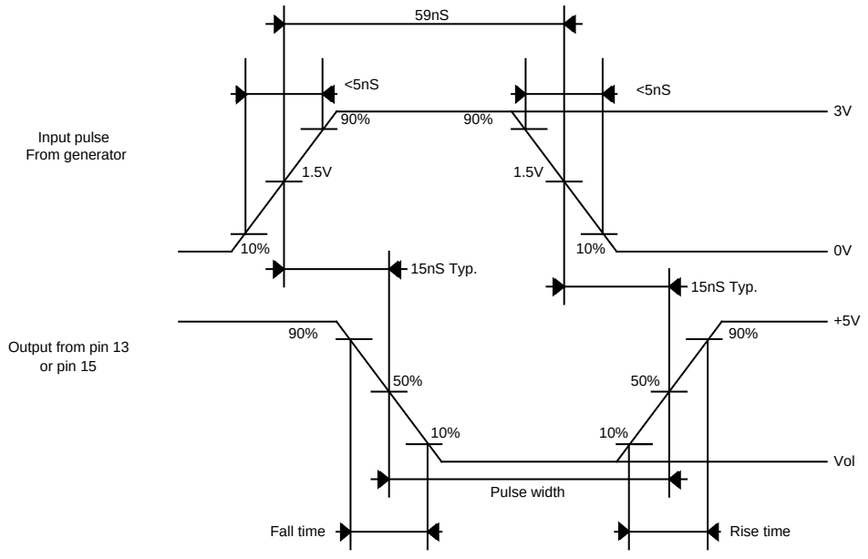

Figure 8. Transmitter Test Citcuit and Switching Waveforms (Measured @ 8.448 Mbps)

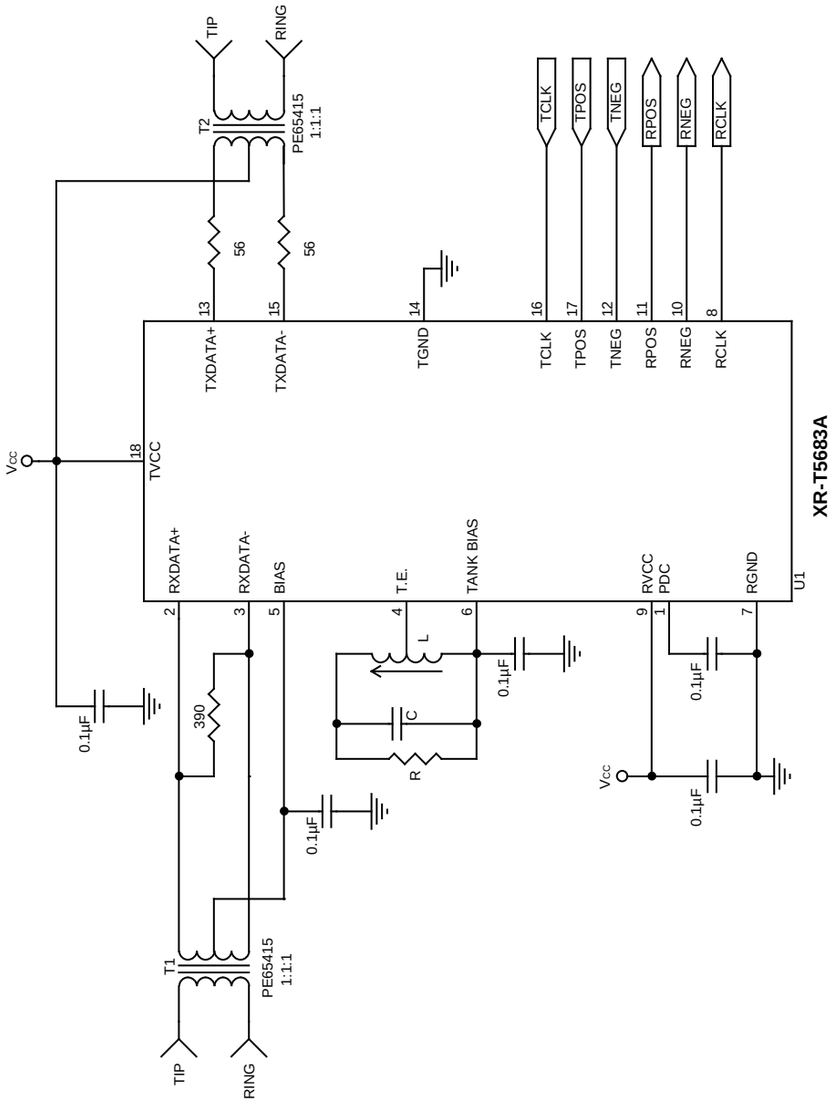

Figure 9. Application Circuit

INPUT AND OUTPUT TRANSFORMERS

Pulse Engineering types PE-65415, PE-65771 or PE-65835 transformers, may be used for both the input and output transformers. These three parts, which are all 1CT:2CT turns ratio and have similar electrical specifications, are wound on small, epoxy-encapsulated, torroid cores. They differ in physical size, operating temperature range and voltage isolation. These transformers are suitable for operation over the 1.544 through 8.448 Mbps range which includes T1, T2, E1 and E2.

Schott- Part Number	Nominal Inductance	Mechanical Style	Bit Rate (MBIT/S)	Tuning Cap. (See Note)
24443	48µHy with CT	RM 5 core, 4 pin bobbin	1.544(T1)	200pF
			2.048(E1)	100pF
24444	5µHy with CT	14 x 8 potcore, 6 pin bobbin	6.312(T2)	100pF
			8.448(E2)	60pF

Table 2. Inductor Selection

Notes:

Capacitor values shown combined with typical stray capacitance will normally resonate the tank circuit at the specific bit rate.

The center-tapped inductor (L) eliminates clock amplifier overload by reducing the signal amplitude applied to T5683 pin 4. While feeding pseudo-random data into the receive input, tune this inductor for minimum jitter on the recovered clock (pin 8) as viewed on an oscilloscope.

R, which may be in the 20K to 50K Ohm range, is optional and may be used to lower clock recovery circuit Q if desired.

Magnetic Supplier Information:

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