XR-T5681

PCM
Transceiver Chip

October 1996-4

FEATURES

- Single +5.0V Supply
- Receiver Can Accept Either Balanced or Unbalanced Inputs
- TTL Compatible Interface
- Transmitter and Receiver in One Package

APPLICATIONS

- T1 and 2.048 MBits/s PCM Line Interface

GENERAL DESCRIPTION

The XR-T5681 is a PCM transceiver chip. It consists of both transmit and receive circuitry in a CDIP 18 pin package. The transceiver is designed for short line application (<-10 dB) such as in digital multiplexed interfacing and digital PBX environments. The maximum frequency of operation is 3 MBits/s so it covers T1 and Europe's 2.048 MBits/s PCM system. The device is designed to operate over the temperature range of 0°C to +70°C.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-T5681	18 Lead 300 Mil CDIP	0°C to +70°C

BLOCK DIAGRAM

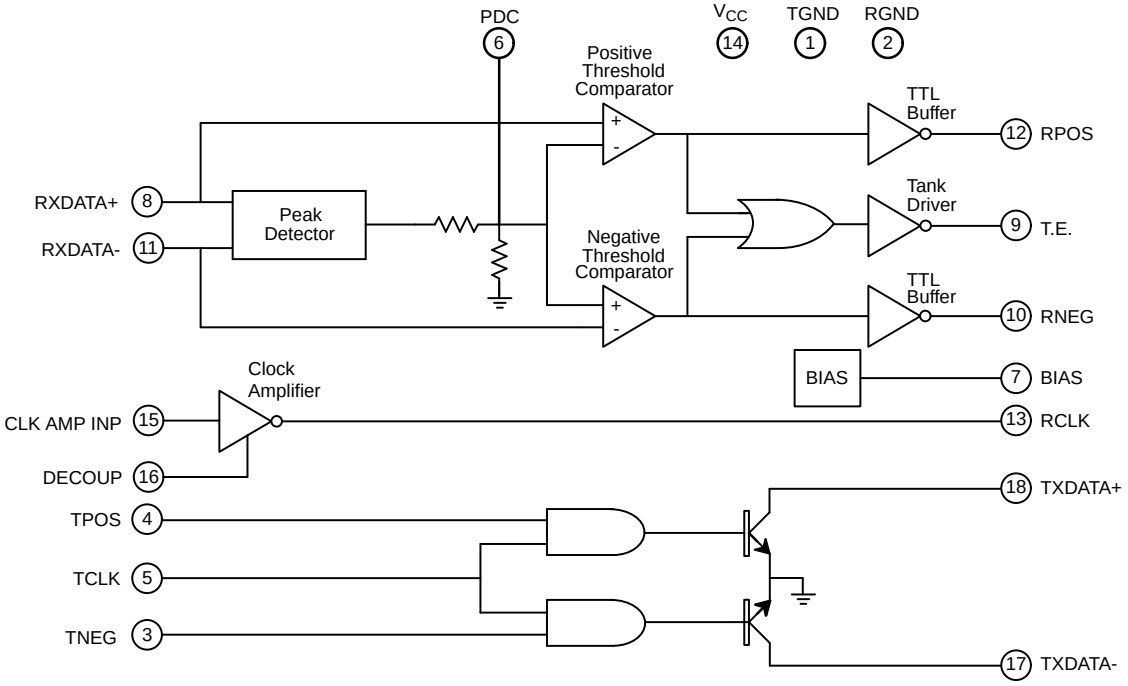
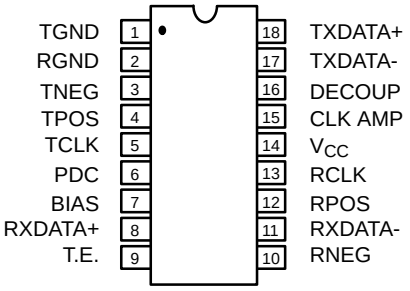


Figure 1. Block Diagram

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

PIN CONFIGURATION



18 Lead CDIP (0.300")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	TGND		**Transmit ground.**
2	RGND		**Receiver ground.** To minimize ground interference a separate pin is used to ground the receiver section.
3	TNEG	I	**Transmit negative data.** TNEG is samples while TCLK is high.
4	TPOS	I	**Transmit positive data.** TPOS is sampled while TCLK is high.
5	TCLK	I	**Transmit clock for TPOS and TNEG.**
6	PDC		**Peak detector capacitor.** This pin should be connected to a 0.1µF capacitor.
7	BIAS	O	**Bias.** This output is to be connected to the center tap of the receiver transformer.
8	RXDATA+	I	**Receive analog input positive.** Line analog input.
9	T.E.	O	**Tank excitation output.** This output connects to one side of the tank circuitry.
10	RNEG	O	**Receive negative data.** Negative pulse data output to the terminal equipment.
11	RXDATA-	I	**Receive analog input negative.** Line analog input.
12	RPOS	O	**Receive positive data.** Positive pulse data output to the terminal equipment.
13	RCLK	O	**Recovered receive clock.** Recovered clock signal to the terminal equipment.
14	V_{CC}		**Positive supply voltage.** +5V.
15	CLK AMP	I	**Receive clock amplifier input.** Connects to pin 9 through a 200 pF capacitor.
16	DECOUP	I	**Decoupling capacitor.** 0.1µF bypass capacitor for clock amplifier.
17	TXDATA-	O	**Transmit negative output.** Transmit AMI signal is driven to the line via a transformer.
18	TXDATA+	O	**Transmit positive output.** Transmit AMI signal is driven to the line via a transformer.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.0V ±5%, T_A = 0°-70°C, Unless Otherwise Specified.

Parameter	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	4.75	5	5.25	V	
Supply Current		30	**46**	mA	Measured at pin 14 Transmit Outputs Open
Receiver Section					
Tank Drive Current	**1.5**	2.0	**2.5**	mA	Measured at Pin 9, V_{CC}=5.0V
Clock Output Low		0.3	**0.8**	V	Measured at Pin 13, I_{OL}=1.0mA
Clock Output High	**3.0**	4.3		V	Measured at Pin 13, I_{OH}=-400µA
Data Output Low		0.4	**0.8**	V	Measured at Pin 10 & 12, I_{OL}=1.0mA
Data Output High	**3.0**	4.5		V	Measured at Pin 10 & 12, I_{OH}=-400µA
DC Voltage Level	0.5	0.7	0.9	V	Measured at Pin 7
DC Voltage Level	0.5	0.7	0.9	V	Measured at Pin 15
DC Voltage Level		3.2		V	Measured at Pin 16
Transmitter Section					
Driver Output Low	**0.6**	0.8	**0.95**	V	Measured at Pin 17 & 18, I_{OL}=40mA
Output Leakage Current		0	**100**	µA	Measured in Off State, Pin 17 & 18 Pull-Up to +20V
Input High Voltage	**2.0**			V	Pin 3, 4, & 5
Input Low Voltage			**0.8**	V	Pin 3, 4, & 5
Input Low Current		-0.7	**-1.3**	mA	Pin 3 &4, V_{OL}=0.4V
Input Low Current		-1.4	**-2.6**	mA	Pin 5, V_{OL}=0.4V
Input High Current		5	**40**	µA	Measured at Pin 3,4, & 5, I_{OH}=2.4V
Output Low Current			**40**	mA	Measured at Pin 17 & 18, V_{OL}=0.95V

Note

-Bold face parameters are covered by production test and guarenteed over operating temperature range.

AC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.0V, T_A = 0°-70°C, Unless Otherwise Specified.

Parameter	Min.	Typ.	Max.	Unit	Conditions
Receiver Section					
Input Level	**1.0**		**6.6**	Vpp	Measured Between Pin 8 & 11
Input Impedance		2.5		kΩ	Measured Between Pin 8 & 11
Clock Duty Cycle	**40**	50	**60**	%	Measured at Pin 13 with 2048kbits AMI Data
Clock Rise & Fall Time (t_{RR}, t_{FR})		20	**35**	ns	Measured ar Pin 13, C_L=15pF
Data Pulse Width (t_{WR})		300		ns	Measured at pin 10 & 12, 0dB Cable Loss, 2048kBits AMI Data, See *Figure 2*
Data Set Up Time (t_{SET})		150		ns	Measured at Pin 10 & 12, 0dB Cable Loss, 2048kBits AMI Data, See *Figure 2*
Data Hold Time (t_{HOLD})		150		ns	Measured at Pin 10 & 12, 0dB Cable Loss, 2048kBits AMI Data, See *Figure 2*
Transmitter Section					
Pulse Width at 2048kHz	**230**	244	**260**	ns	See *Figure 3* & *Figure 4*
Output Rise Time (t_{RT})		15	**30**	ns	See *Figure 3* & *Figure 4*
Output Fall Time (t_{FT})		15	**30**	ns	See *Figure 3* & *Figure 4*
Output Pulse Width Imbalance		±2.5		ns	At 50% Output Level
Tx Prog. Delay t_{PHL}		20	**30**	ns	See *Figure 4*
Tx Prog. Delay t_{PLH}		30	**40**	ns	See *Figure 4*

Note

-Bold face parameters are covered by production test and guarenteed over operating temperature range.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +20V
Storage Temperature . . . . . -65°C to +150°C
Operating Temperature . . . . . 0°C to +70°C

SYSTEM DESCRIPTION

The incoming bipolar PCM signal which is attenuated and distorted by the cable is applied to the threshold comparator and the peak detector. The peak detector generates a DC reference for the threshold comparator for data and clock extraction. An external tank circuit tuned to the appropriate frequency is added for the later operation. The clock signal, RXDATA+ and RXDATA- all go through a similar level shifter to be converted into TTL level to be compatible for digital processing.

In the transmit direction, the output drivers consist of two identical TTL inputs with open collector output stages. The maximum low level current these output stages can sink is 40mA. With full width data (NRZ) applied to the inputs together with a synchronized clock, the output will generate a bipolar signal when driving a center–tapped transformer. A block diagram of the XR–T5681 is shown in *Figure 1*.

The clock recovery uses an external tank circuit. The receive data will create an excitation for the tank circuitry which in turn will create a recovered, received clock (RCLK).

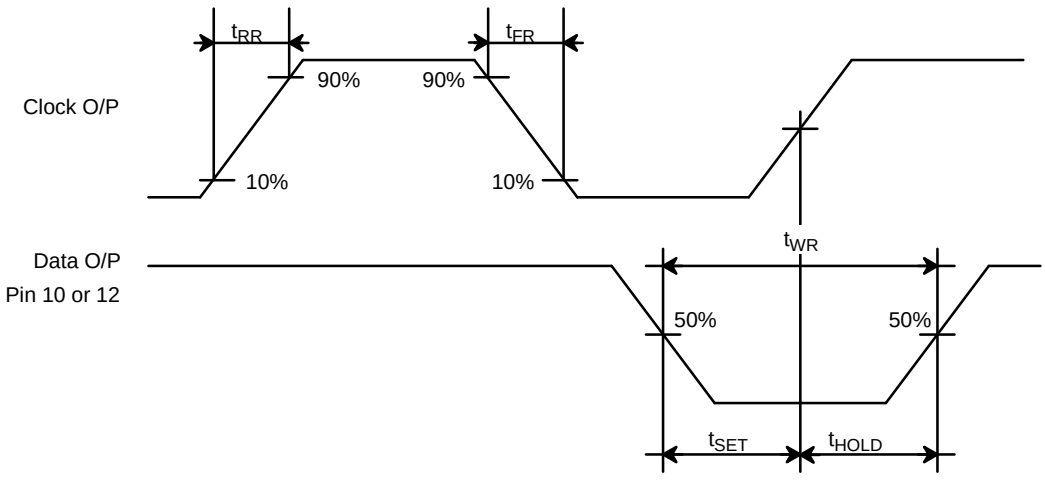


Figure 2. RX Receiver Timing Diagram

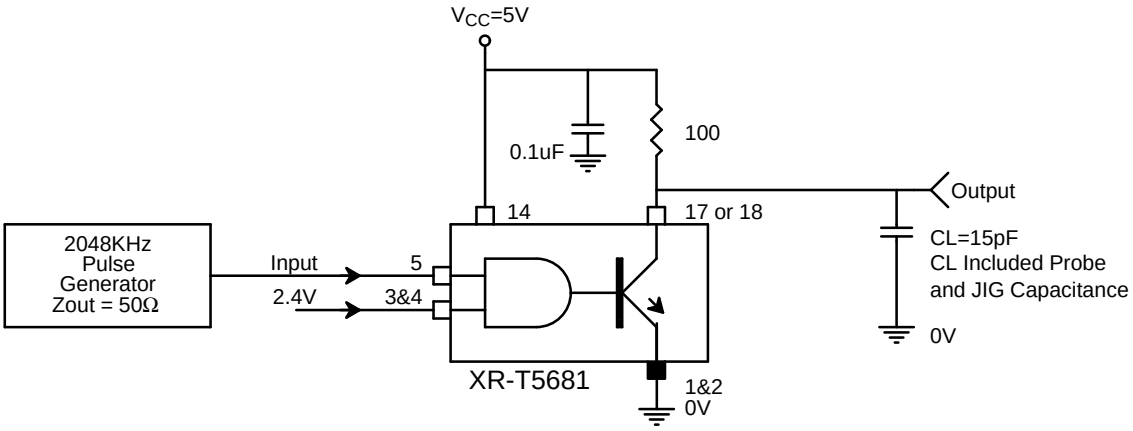


Figure 3. TX Test Circuits

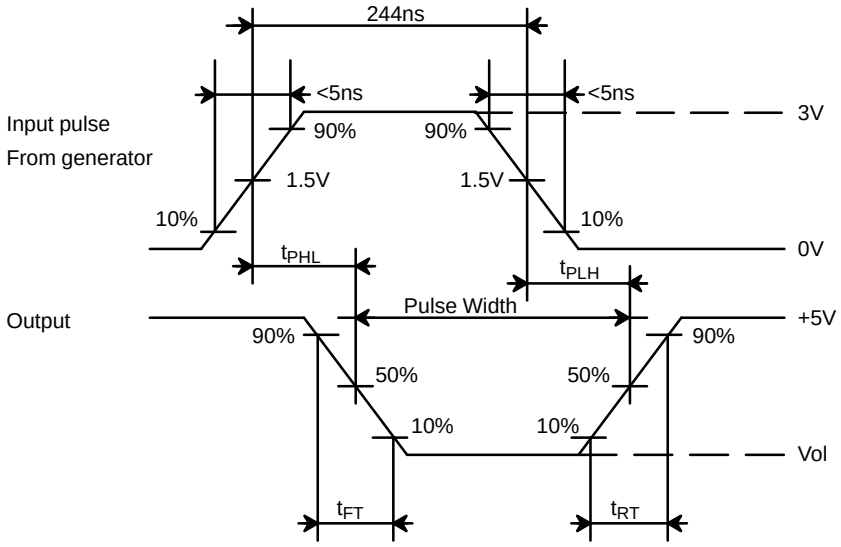


Figure 4. TX Test Circuits and Switching Waveforms

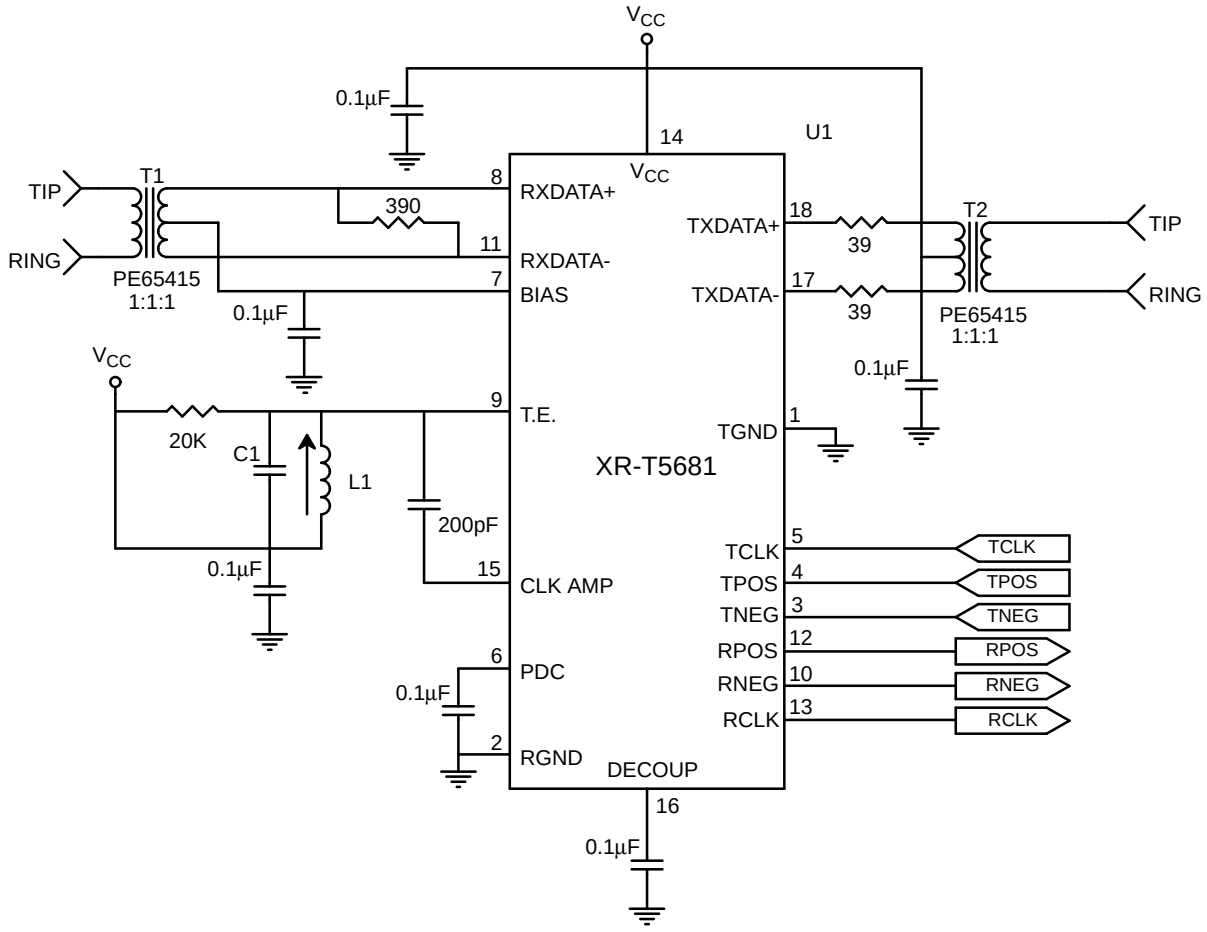


Figure 5. Application Circuit for XR-T5681

INPUT AND OUTPUT TRANSFORMERS

Pulse Engineering types PE-65415, PE-65771 or PE-65835 transformers, may be used for both the input and output transformers. These three parts, which are all 1CT:2CT turns ratio and have similar electrical specifications, are wound on small, epoxy-encapsulated, torroid cores. They differ in physical size, operating temperature range and voltage isolation. These transformers are suitable for operation over the 1.544 and 2.048 Mbps T1 and E1 range.

L1 Schott-Part Number	Nominal Inductance	Mechanical Style	Bit Rate (MBIT/S)	Tuning Cap. (C1)
24443	48µHy with CT	RM 5 Core, 4 Pin Bobbin	1.544(T1)	200pF
			2.048(E1)	100pF

Table 1. Inductor Selection

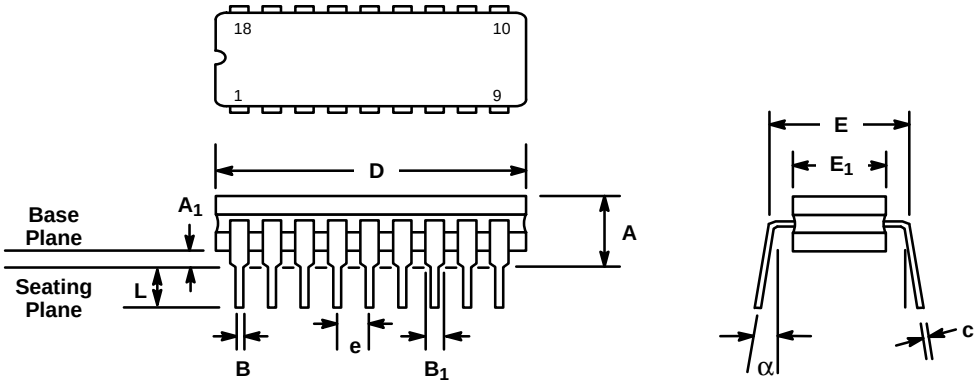
Magnetic Supplier Information:

Pulse
P.O. Box 12235
San Diego, CA 92112
Tel. (619) 674-8100
Fax. (619) 885-0834

John Marshall
Schott Corporation
1838 Elm Hill Pike, Suite 100
Nashville, TN 37210
Tel. (615) 889-8800
Fax (615) 885-0834

18 LEAD CERAMIC DUAL-IN-LINE (300 MIL CDIP)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.200	2.54	5.08
A_1	0.015	0.070	0.38	1.78
B	0.014	0.026	0.36	0.66
B_1	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.860	0.960	21.84	24.38
E_1	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

Notes

Notes

NOTICE

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