Single Chip V.35 Transceiver

GENERAL DESCRIPTION

XR-T3590 is a single chip device which contains three V.35 receivers and transmitters. This device by itself is sufficient to implement all the data and clock signals required for a V.35 interface. For the handshaking signals, separate RS-232 transceivers are necessary.

This device supports multiple modes of operation including DCE and DTE. Diagnostic loopbacks are supported both in the DCE and DTE modes. To accommodate diagnostics in both direction, a mirrored loopback is implemented. It needs to be mentioned that both clock and data paths are looped back during the diagnostics mode. This feature can be invoked by applying appropriate patterns to SEL lines. (See Table 1) For power management flexibility, all of the drivers and receivers can be placed in a shut down mode. For applications where only receivers are required, all the drivers can be disabled and vice versa. During disable mode the output drivers are placed in Hi-Z state.

The differential V.35 output drivers of this device are implemented using a current mode type design. This minimizes the number of external resistors required. Due to low voltage swing required in the current mode of operation, the emission in a typical V.35 interface using this device is minimized. Each transmitter and receiver would require an external resistor network consisting of 3 resistors for termination. This device does not require any large capacitors in addition to two 0.1 µF decoupling caps needed across the power supplies. In order to reduce the number of external components, resistor network can be used to realize both the driver and receiver termination.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Supply Voltage	+/-7V

FEATURES

- Single device provides three receivers and transmitters fully compliant with electrical specification of V.35 interface (receiver differential inputs are V.11 compliant)
- Supports all V.35 clock and data signals in DTE and DCE modes of operation
- Transmitters are short circuit protected
- Supports a maximum data rate of 10 MBPS up to 100 meters
- Full compliance with CCITT V.35 specification
- Supports mirrored diagnostic loopbacks in DTE and DCE modes of operation
- Allows disabling all receivers, or all drivers, or all receivers and drivers
- During the disable mode the outputs are placed in Hi-Z state
- Maximum power dissipation 540 mW (All active mode)
- Maximum power consumption 600 mW (All drivers loaded)
- Current consumption during shut down mode is less than 300 µA

APPLICATIONS

Bridges and Routers
Modems
Digital Service Units (DSUs)
Multiplexers
HDSL and ADSL equipment
Inverse Multiplexers
Workstations

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T3590IP	PDIP	-40°C to +85°C
XR-T3590ID	SOIC	-40°C to +85°C

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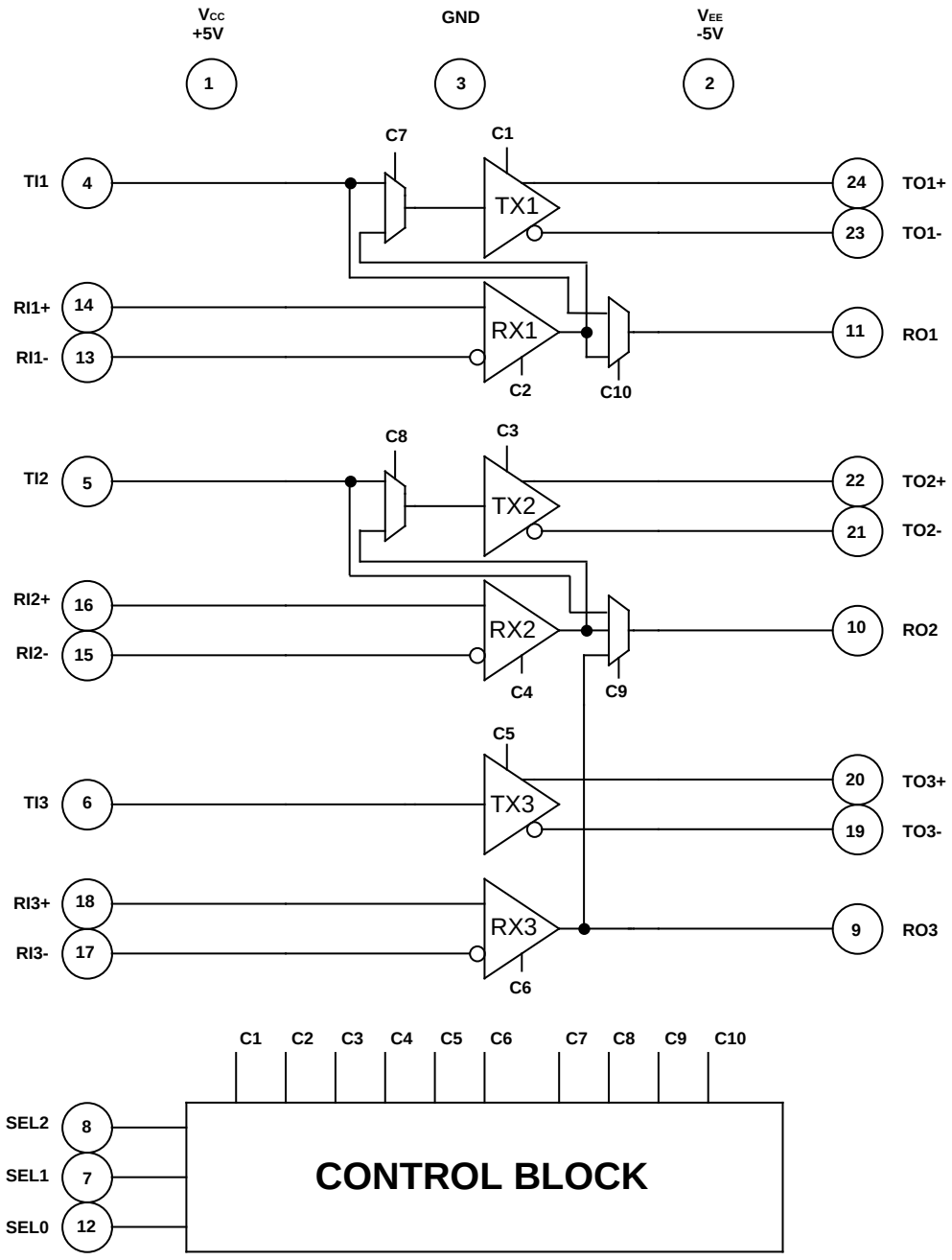
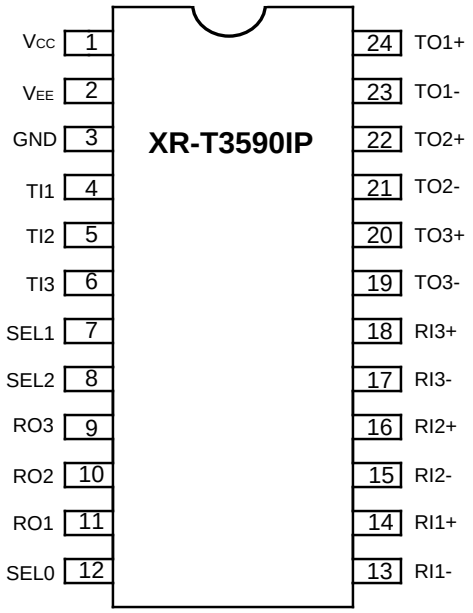
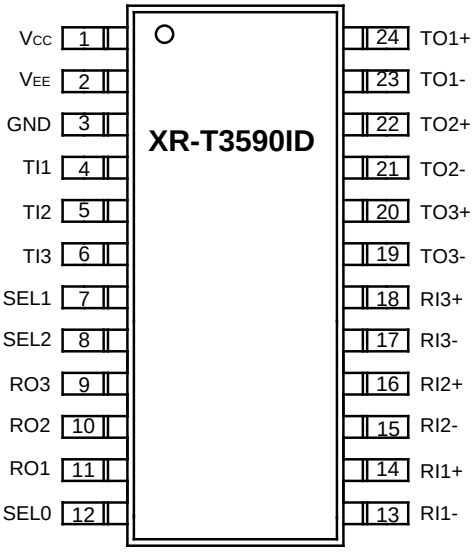


XR-T3590 Block Diagram



24 Pin Dual In Line Package



24 Pin SOIC Package

XR-T3590 Pin Assignments

PIN DESCRIPTION

PIN#	SYMBOL	TYPE	SIGNAL	DESCRIPTION
1	V_{CC}	-	-	+5 V (+/-0.25 V).
2	V_{EE}	-	-	-5 V (+/-0.25 V).
3	GND	-	-	GROUND.
4	TI1	I	TTL	TRANSMITTER 1 INPUT.
5	TI2	I	TTL	TRANSMITTER 2 INPUT.
6	TI3	I	TTL	TRANSMITTER 3 INPUT.
7	SEL1	I	TTL	MODE SELECT 1. (see table 1 for details)
8	SEL2	I	TTL	MODE SELECT 2. (see table 1 for details)
9	RO3	O	TTL	RECEIVER 3 OUTPUT.
10	RO2	O	TTL	RECEIVER 2 OUTPUT.
11	RO1	O	TTL	RECEIVER 1 OUTPUT.
12	SEL0	I	TTL	MODE SELECT 0. (see table 1 for details)
13	RI1-	I	V.35	RECEIVER 1 NEGATIVE INPUT.
14	RI1+	I	V.35	RECEIVER 1 POSITIVE INPUT.
15	RI2-	I	V.35	RECEIVER 2 NEGATIVE INPUT.
16	RI2+	I	V.35	RECEIVER 2 POSITIVE INPUT.
17	RI3-	I	V.35	RECEIVER 3 NEGATIVE INPUT.
18	RI3+	I	V.35	RECEIVER 3 POSITIVE INPUT.
19	TO3-	O	V.35	TRANSMITTER 3 NEGATIVE OUTPUT.
20	TO3+	O	V.35	TRANSMITTER 3 POSITIVE OUTPUT.
21	TO2-	O	V.35	TRANSMITTER 2 NEGATIVE OUTPUT.
22	TO2+	O	V.35	TRANSMITTER 2 POSITIVE OUTPUT.
23	TO1-	O	V.35	TRANSMITTER 1 NEGATIVE OUTPUT.
24	TO1+	O	V.35	TRANSMITTER 1 POSITIVE OUTPUT.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = **+5.0V** +/-5%, V_{EE}=**-5.0V** +/-5%, T_A = **25°C**, (Note 1), driver and receiver are enabled unless otherwise specified. (See Figure 1)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
$\|V_{OD}\|$	Transmitter Differential Output Voltage	***0.44***	0.55	***0.66***	V	-4V≤VOS≤+4V
V_{OC}	Transmitter Common-Mode Output Voltage	***-0.3***	0	***+0.3***	V	V_{OS} = 0 V
I_{OH}	Transmitter Output High Current	**-12.6**	-11	**-9.4**	mA	
I_{OL}	Transmitter Output Low Current	**9.4**	11	**12.6**	mA	
I_{OZ}	Transmitter Output Leakage Current		±1	±100	µA	V_{TO}^+ = ±5V V_{TO}- = ±5V While driver disabled
R_O	Transmitter Output Impedance		50		KΩ	
V_{TH}	Differential Receiver Input Threshold Voltage			*150*	mV	F=10 Mbps
V_{HYST}	Receiver Input Hysterisis		30		mV	V_{OS} = 0V
I_{IN}	Receiver Input Current			***±0.4***	mA	-5V≤V_{RI+}, V_{RI-}≤5V
R_{IN}	Receiver Input Impedance Differential		35		KΩ	-5V≤V_{RI+}, V_{RI-}≤5V
V_{OH}	Receiver Output High Voltage	***3***	4.5		V	I_{OH}=-4mA
V_{OL}	Receiver Output Low Voltage		0.4	***0.8***	V	I_{OL}=4mA
I_{OSC}	Receiver Output Short-Circuit Current		13		mA	0≤V_O≤V_{CC}
I_{OZR}	Receiver Three-State Output Current			***±10***	µA	Receiver DIsabled 0 ≤ V_O ≤ V_{CC}
V_{IH}	Logic Input High Voltage	***2***			V	TIn, SEL2-0
V_{IL}	Logic Input Low Voltage			***0.8***	V	TIn, SEL2-0
I_{IN}	Logic Input Current		***±2.5***	***±10***	µA	TIn, SEL2-0
I_{CC}	V_{CC} Supply Current		36 250	***50***	mA µA	All On, Loaded, F=10Mbps All Off
I_{EE}	V_{EE} Supply Current		-38 -180	***-50***	mA µA	All On All Off

Note 1: *All currents flowing into the device pins are marked positive. All current flowing out of the device pins are marked negative.*

Note 2: *Bold face parameters are covered by production test. Italicized parameters are guaranteed over full operating temperature range.*

AC Electrical Characteristics

V_{CC} = **+5.0V** +/-5%, V_{EE} = **-5.0V** +/-5%, T_A = **25°C**, driver and receiver are enabled unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
T_R, T_F	Transmitter Rise or Fall Time		5	***30***	ns	V_{OS}=0V
T_{TPLH}	Transmitter Input to Output Propagation Delay		25	***40***	ns	V_{OS}=0V
T_{TPHL}	Transmitter Input to Output Propagation Delay		27	***40***	ns	V_{OS}=0V
T_{OSKEW}	Transmitter Output to Output Skew		**3**		ns	V_{OS}=0V
T_{RPLH}	Receiver Input to Output Propagation Delay (rising)		37	***50***	ns	V_{OS}=0V
T_{RPHL}	Receiver Input to Output Propagation Delay (falling)		35	***50***	ns	V_{OS}=0V
T_{ISKEW}	Differential Receiver Skew (T_{RPLH} - T_{RPHL})		**2**		ns	V_{OS}=0V
T_{ZL}	Receiver Enable to Output Low		34		ns	
T_{ZH}	Receiver Enable to Output High		37		ns	
T_{LZ}	Receiver Disable from Output Low		55		ns	
T_{HZ}	Receiver Disable from Output High		57		ns	

Note 1: *All currents flowing into the device pins are marked positive.*
All current flowing out of the device pins are marked negative.

Note 2: *Bold face parameters are covered by production test. Italicized parameters are guaranteed over full operating temperature range.*

Table 1. FUNCTION TABLE

SEL2	SEL1	SEL0	DRIVERS ON	RECEIVERS ON	DESCRIPTION
0	0	0	-	-	All off
0	0	1	-	1, 2, 3	All receivers on
0	1	0	1, 2, 3	1, 2	DCE mode
0	1	1	1, 2, 3	1, 2	DCE mode with mirrored loopback
1	0	0	1, 2	1, 2, 3	DTE mode
1	0	1	1, 2	1, 2, 3	DTE mode with mirrored loopback
1	1	0	1, 2, 3	1, 2, 3	All on
1	1	1	1, 2, 3	-	All drivers on

Note: *The driver and receiver outputs which are not on, are placed in Hi-Z state.*

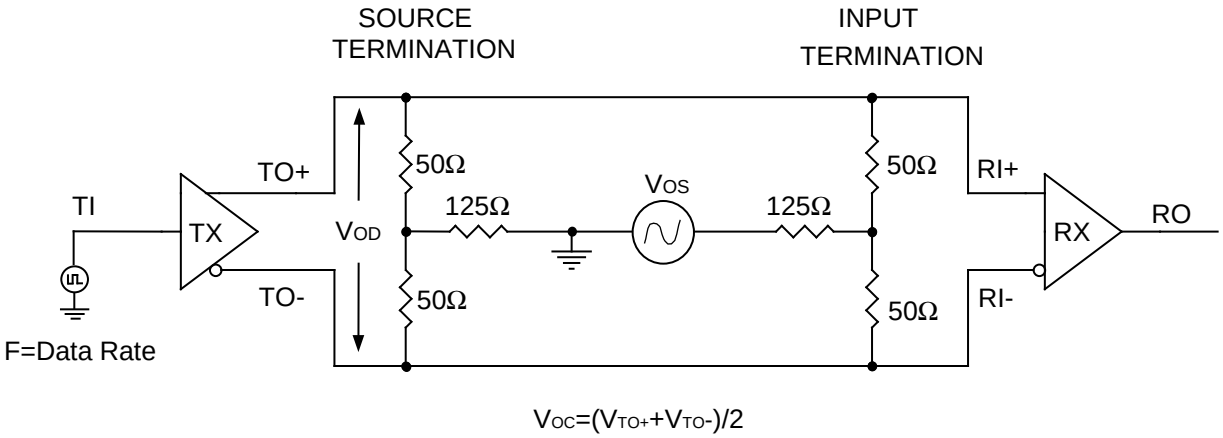


Figure 1. XR-T3590 Test Circuit

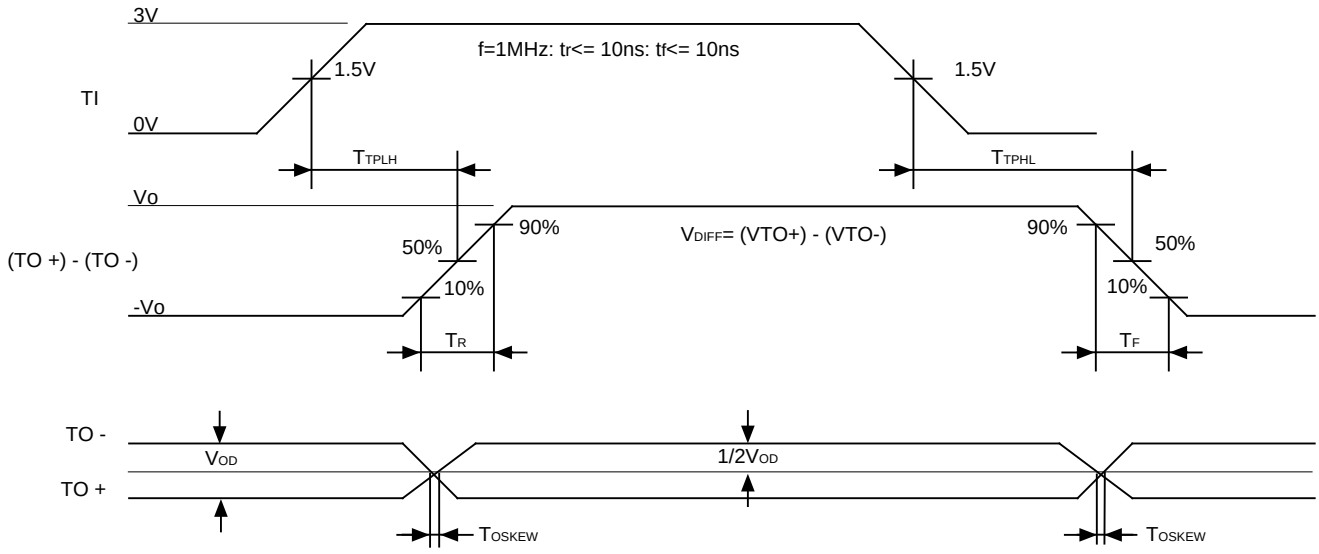


Figure 2. V.35 Transmitter Propagation Delays

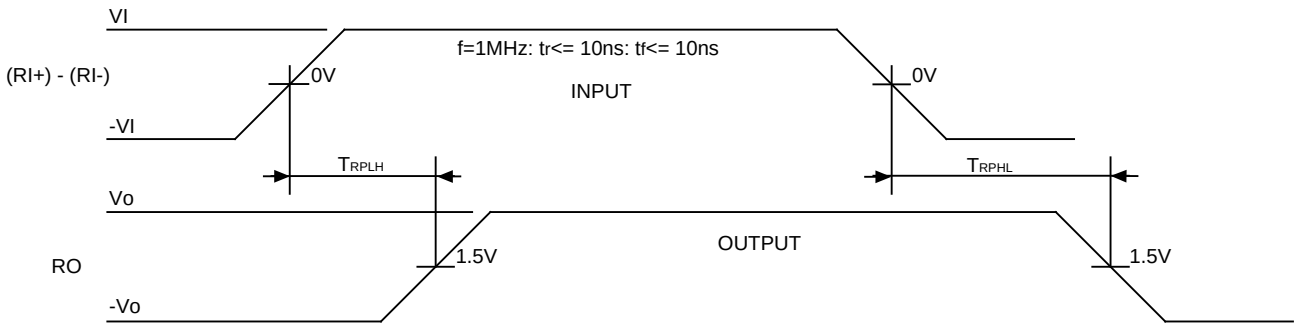


Figure 3. V.35 Receiver Propagation Delays

Cable Termination

For proper operation, the differential inputs and outputs of the XR-T3590 must be properly terminated. This is a requirement to assure full adherence to V.35 electrical signal specifications. The following diagram is a proposed termination configuration:

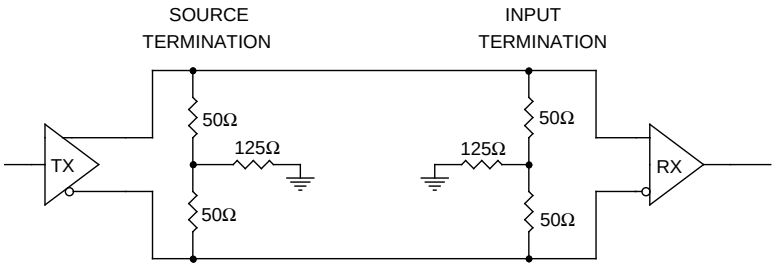


Figure 4. Proposed source and input terminations

Note: *In order to implement the terminations proposed above, standard 1/8 W surface mount or through hole 5% resistors can be used. Furthermore appropriate resistor networks can be used as well.*

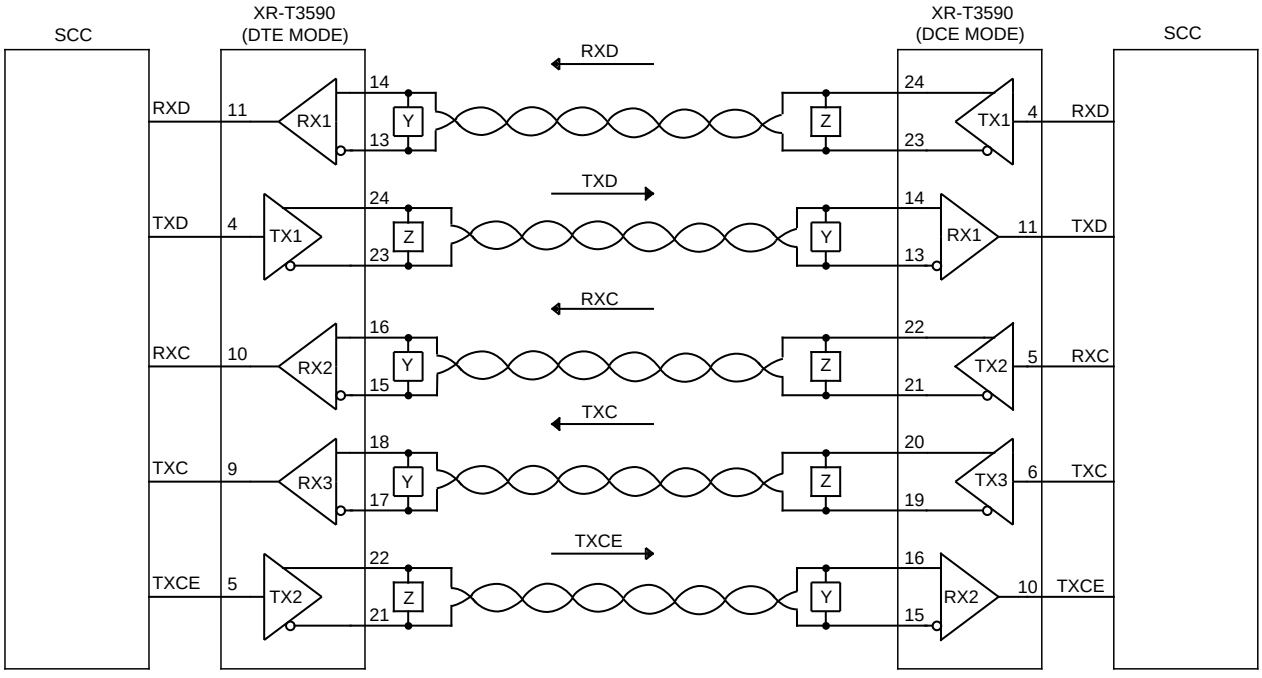


Figure 5. Typical V.35 clock and data configuration

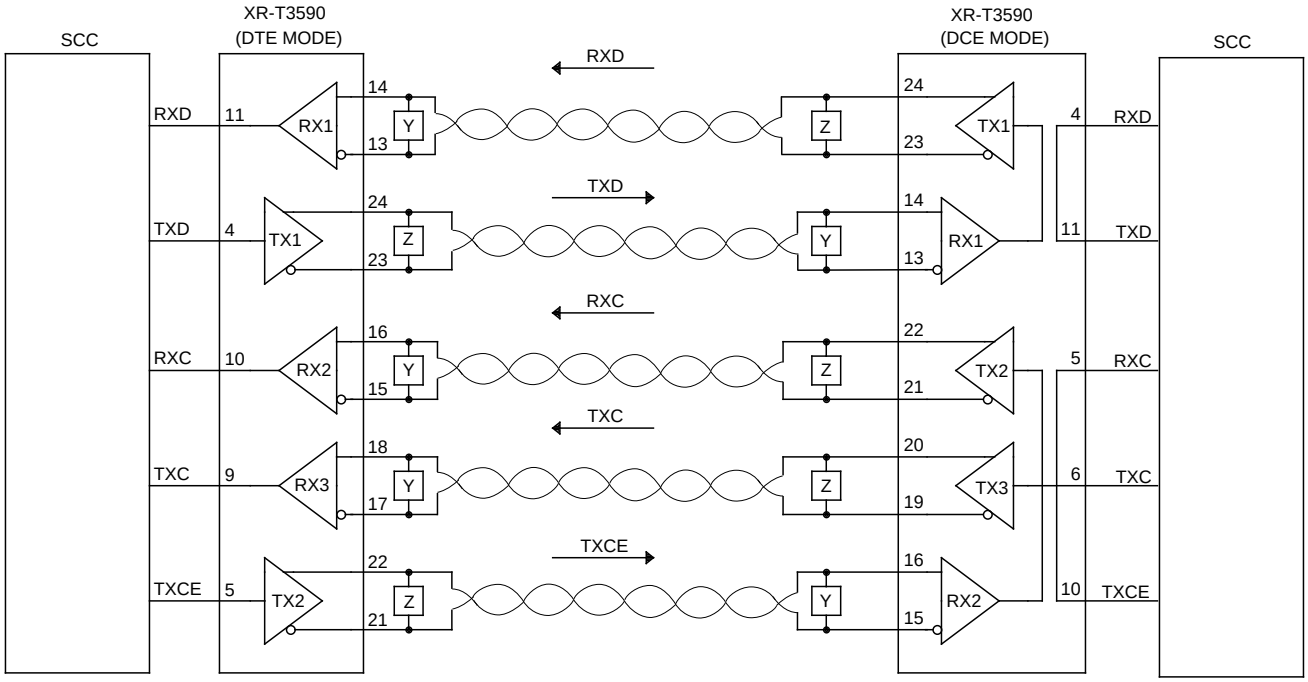


Figure 6. Typical V.35 configuration during DCE mirrored loopback

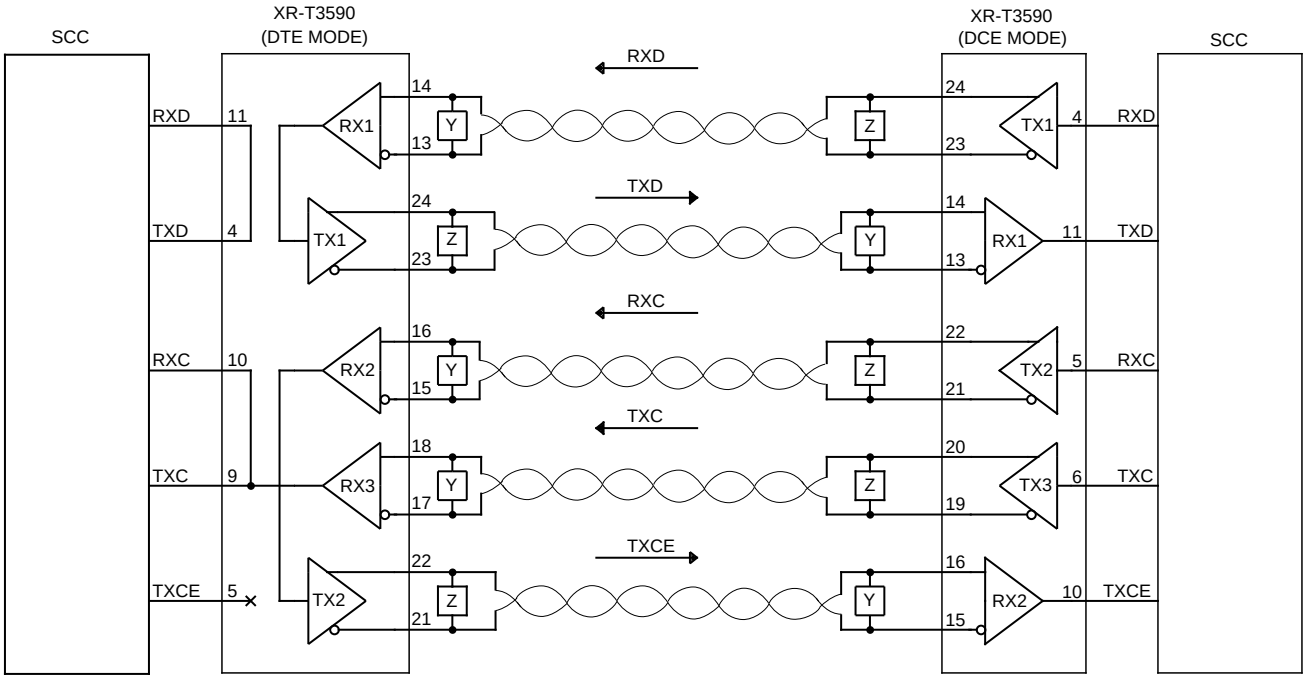


Figure 7. Typical V.35 configuration during DTE mirrored loopback

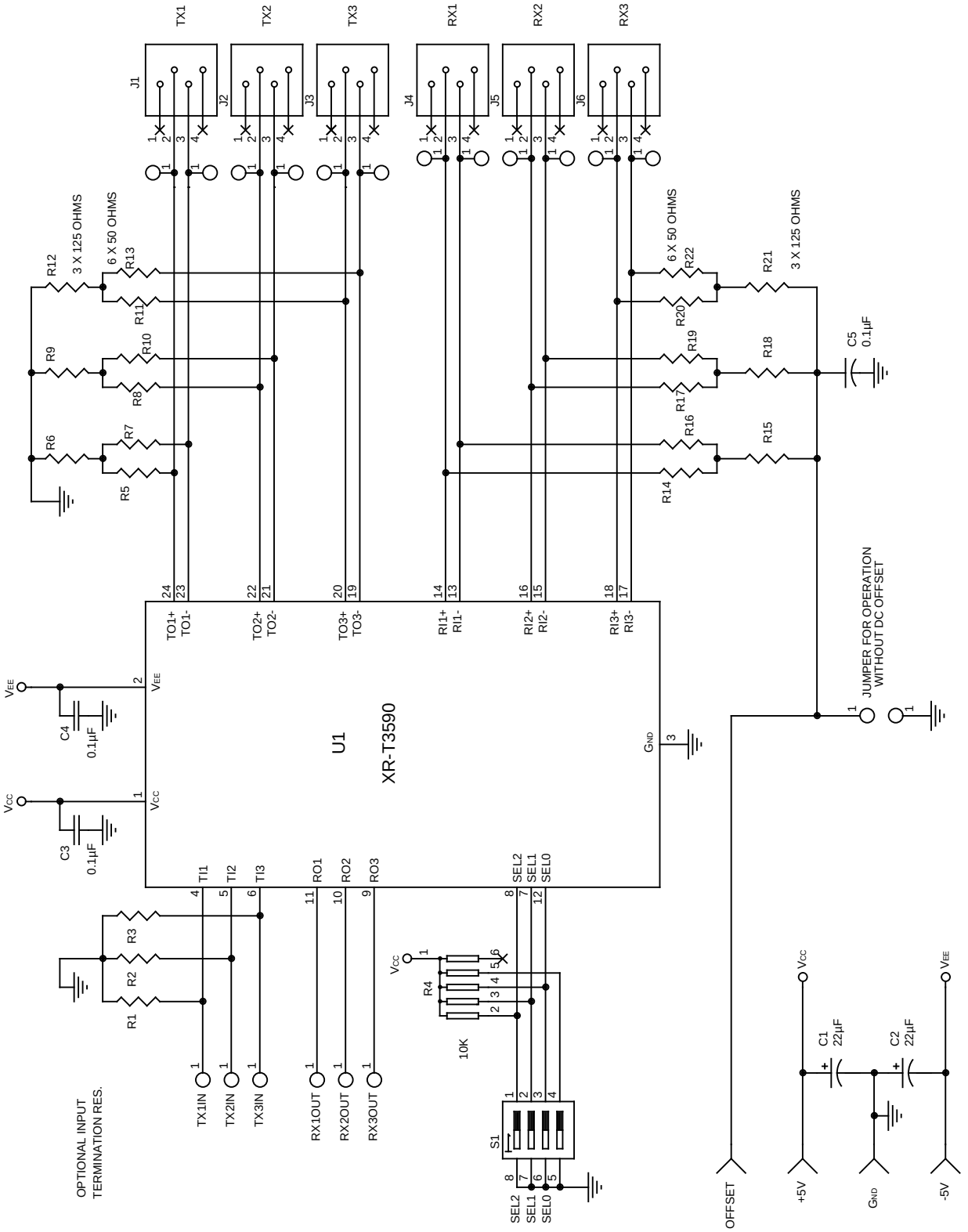
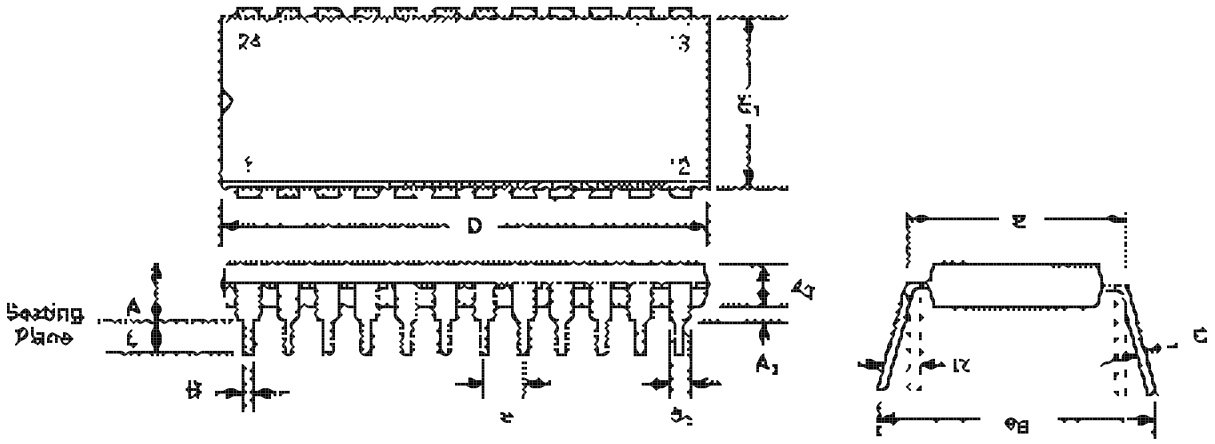


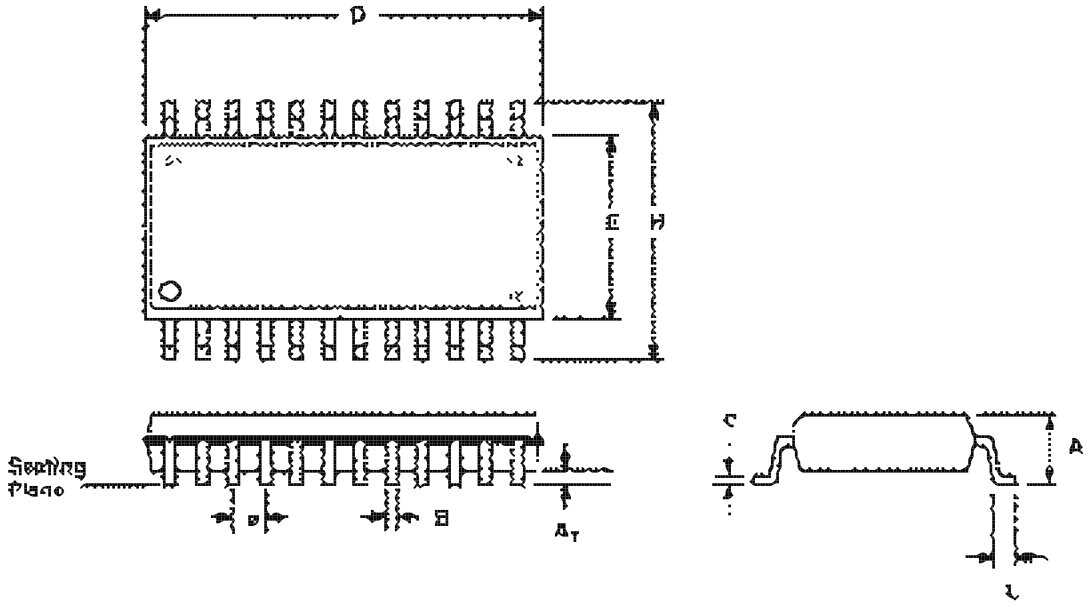
Figure 8. XR-T3590 Demo Board

24 LEAD PLASTIC DUAL-IN-LINE
(600 MIL PDIP)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.250	2.54	6.35
A_1	0.015	0.070	0.38	1.78
A_2	0.125	0.195	3.18	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.36
D	1.150	1.290	29.21	32.77
E	0.600	0.625	15.24	15.88
E_1	0.485	0.580	12.32	14.73
e	0.100 BSC		2.54 BSC	
eB	0.600	0.700	15.24	17.78
L	0.115	0.200	2.92	5.08
α	0°	15°	0°	15°

24 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.596	0.614	15.20	15.60
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

Notes

Notes

NOTICE

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Data Sheet March 1996