EVALUATION KIT PARTS LIST

This kit contains the following:

- XRD8794AB Application Board
- XRD8794 5V ADC or XRD87L94 3V ADC
- XRD8794AB Application Note
- XRD8794 or XRD87L94 Data Sheet

FEATURES

- Same Printed Circuit Board Design Used in Production Test Flow
- Easy Evaluation of XRD8794, XRD87L94 & MP8791*
- True 12 Bit Accurate Circuit & Board Layout
- Optimized Support Circuits
- User Friendly / Flexible Interface

INTRODUCTION

The XRD8794AB is a complete printed circuit test board designed to permit quick and accurate evaluation of EXAR's XRD8794 & XRD87L94, 12-bit 2 MSPS analog-to-digital converters.

The XRD8794AB is the same DUT board used in EXAR's production test. This results in a true 12-bit board that provides a common platform for both our customers and our engineers. The top of the XRD8794AB is designed as an applications board and the bottom for interfacing to EXAR's in-house testers.

The XRD8794AB can also be used to evaluate the MP8791 because the products are pin-for-pin compatible.* This applications board combines a proven PC Board layout with optimized analog and digital interface circuitry to satisfy the stringent requirements needed in evaluating high performance devices of this type.

The board contains the device being tested (XRD8794), operational amplifiers for input buffers, latches, numerous connectors, jumper options, and observation test points in commonly used locations.

Complete DC and AC performance of the part can be evaluated by interfacing external laboratory equipment to the flexible user interface.

** Functional Difference – MP8791 does not high-z digital outputs automatically, see section: MP8791 in XRD8794AB*

PREVIEW OF COMMON TEST CONFIGURATIONS

The board is set up as a general A/D test circuit where the references are fixed. *Figure 4.* shows this default test circuit. Circuit timing is demonstrated in *Figure 7.* There are many other circuit possibilities built into the universal test board, however, starting with the default circuit is recommended.

In addition to the default test circuit, two other test configurations are discussed: the cross plot test and the external reconstruction DAC test.

Options for analyzing the output results are discussed in detail below. The most effective of these is the use of a high speed data acquisition system and FFT software to compute the performance parameters.

PCB CONSTRUCTION & LAYOUT (DUAL PURPOSE BOARD)

The XRD8794AB is used as both an applications board and as a test board at EXAR. The board was designed on the top as an applications and characterization board. The bottom was designed to interface to EXAR's in-house production testers (with the exception of a few components that are common to both designs). This application note focuses on the top side of the board for laboratory characterization and not production test. Therefore, there are additional labels and patterns on the board that are not used or mentioned in this application note. *Figure 1.* clarifies which patterns are not used or discussed in this application note.

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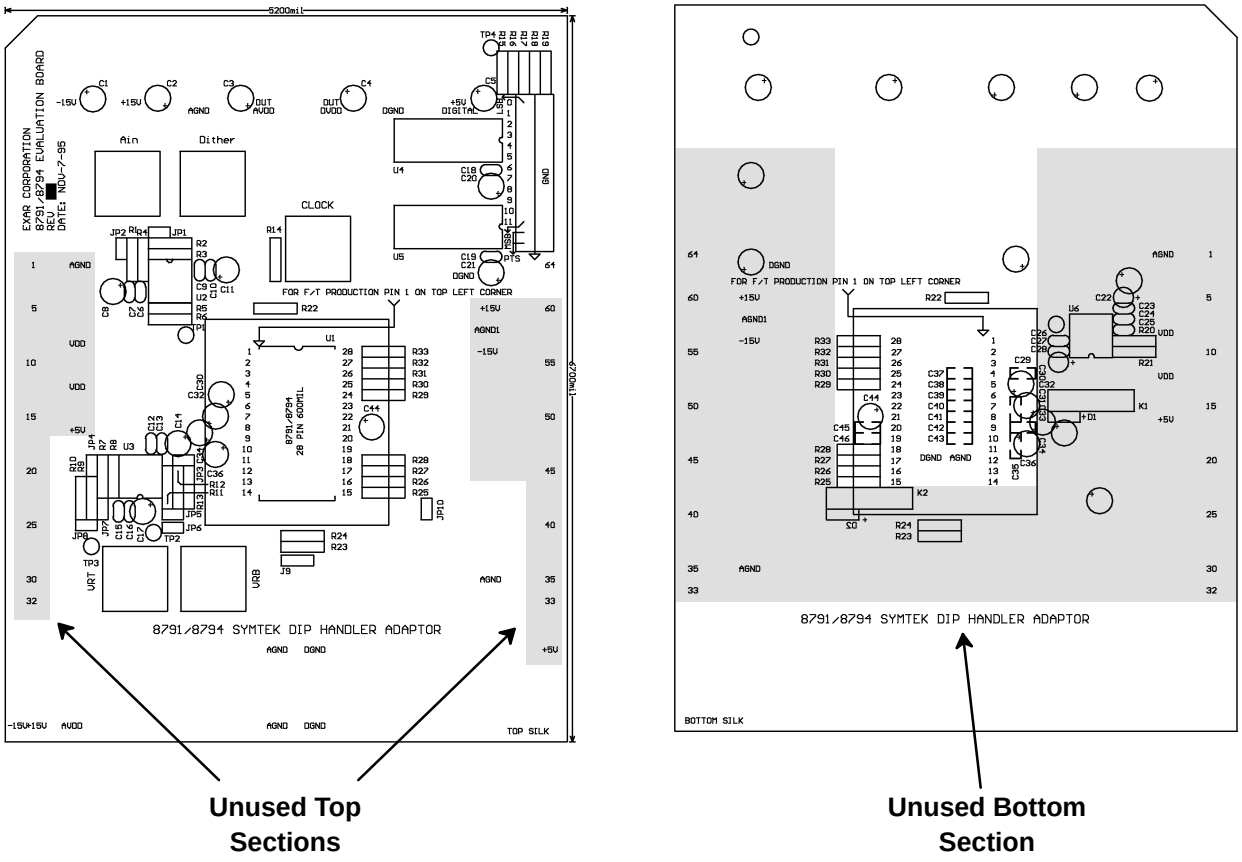

Figure 1. Unused Patterns On XRD8794AB
(Patterns in Grey Used For EXAR Production Test Only)

The XRD8794AB printed circuit board is a four layer board with two internal layers dedicated to power and ground. Top and bottom layers are used for the routing of circuitry. The internal power planes have a 5 mil separation that use the inherent board capacitance to aid power supply bypassing. The board's finished thickness is 100 mils. Figures 11 through 16 at the back of this application note show each layer of the board.

SYSTEM CONFIGURATION - LAB SETUP

The evaluation block diagrams of the XRD8794AB with typical external test equipment are shown in *Figure 4., Figure 5., and Figure 8.* The following is a more detailed description of the major on-board and external components used in these systems.

Application Board Circuitry

The application board support circuitry is shown in *Figure 2.*

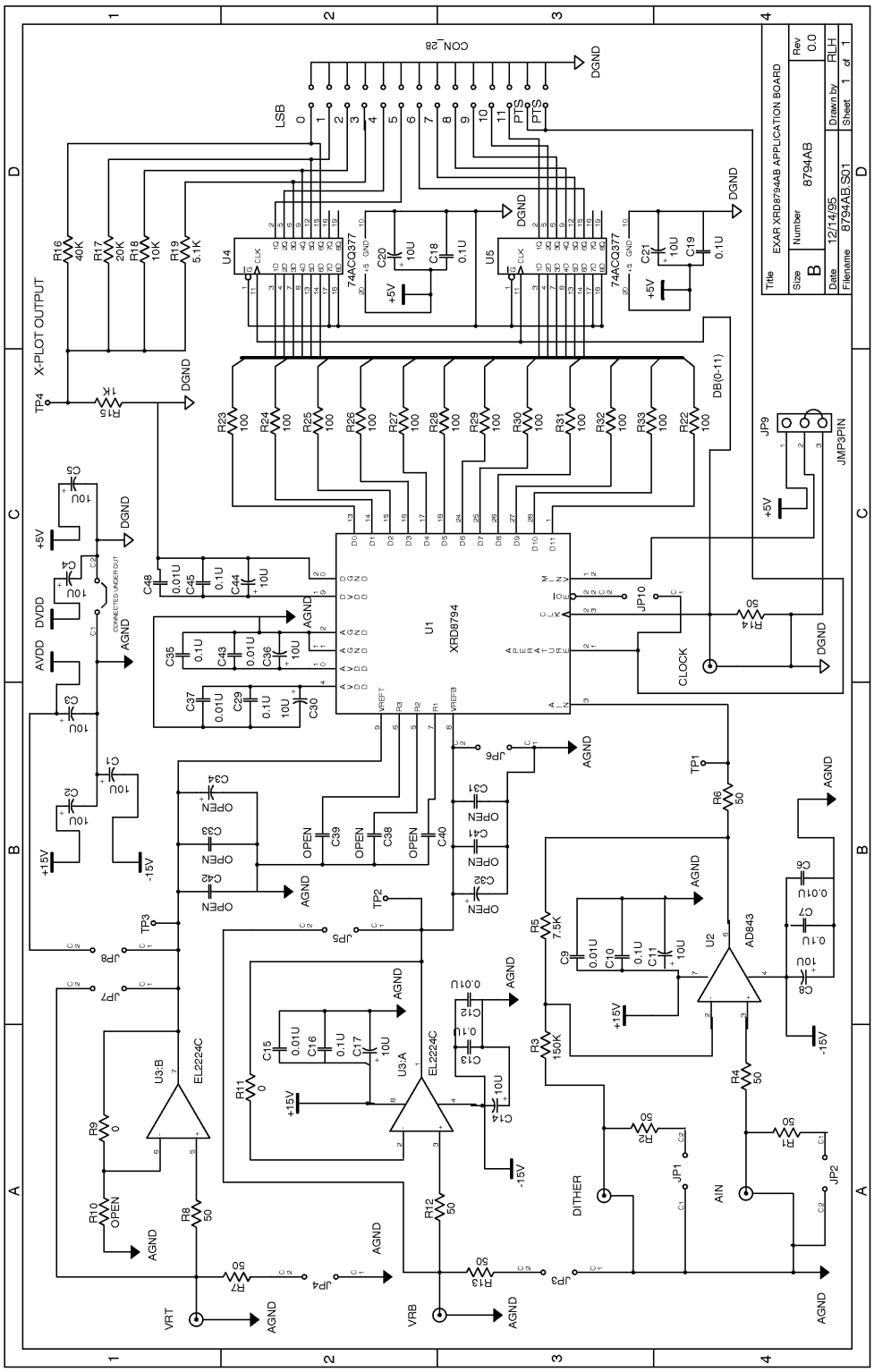

Figure 2. XRD8794AB Schematic

The major components supporting the A/D under test are:

1. V_{REF} BUFFERS - A dual op amp (EL2224C) can be used to isolate the externally supplied V_{RT} and V_{RB} from the device under test and provides a low source impedance. These buffers can be bypassed with on-board jumpers (JP5 and JP7). Holes for optional compensation and gain are provided.

2. ANALOG INPUT AMPLIFIER - An operational amplifier (AD843) is used to provide a low source impedance to the A/D. Provisions are made for summing a dither signal and/or offset voltage with the input.

3. DATA LATCHES - The digital output of the A/D drive on-board quiet latches (74ACQ377) which buffer the device under test from the external test equipment.

4. RECONSTRUCTION DAC - A simple resistor implementation of a reconstruction DAC allows for a cross plot test at TP4. TP4 outputs an analog waveform generated from the four LSBs taken at the outputs of the data latches. See Cross Plot Test.

5. DIGITAL & ANALOG WORK AREAS - 100 mil spaced holes allow configuration of additional circuitry powered from either analog or digital planes. The work area power and ground pads are shown in *Figure 3.* for both the analog and digital planes.

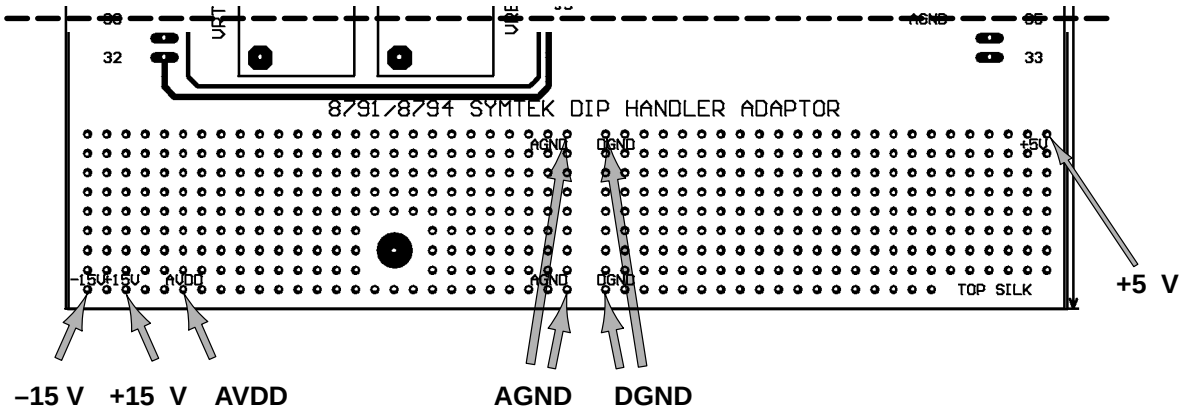

Figure 3. Analog and Digital Work Area with Power and Ground Pads

External Equipment Required

The system block diagrams (*Figure 4., Figure 5., and Figure 8.)* show the external test equipment required to perform all test and evaluation functions. These include:

1. POWER SUPPLIES - ±15V and several +5V external power supplies are needed. Separate digital and analog grounds are provided. The analog and digital ground planes are soldered together underneath the board. The XRD8794 substrate is common to both the digital and analog ground pins. Treat the data converter as an analog device when considering layout grounding options. Decoupling circuits are provided on the applications board, however, low noise, low output impedance supplies are necessary for best performance. Banana connectors are used for all power and ground connections. For best results, twist the power supply cable pairs. This minimizes coupling to and from unrelated sections of the setup.

2. CLOCK GENERATOR - A symmetrical clock signal must be applied to the BNC coax connector labeled CLOCK. Select a low jitter clock for best spectral results. Note the 50Ω input impedance.

3. REFERENCE SUPPLIES - A positive and negative reference voltage is connected through the BNC coax connectors labeled V_{RT} and V_{RB} (typically +5 and 0V respectively). The external reference voltages can be configured to go through op amp buffers or go directly to the A/D by using jumpers JP5 and

JP7. Using JP8 the positive reference can be shorted to AV_{DD} and using JP6 the negative reference can be shorted to AGND. If JP6 and JP8 are in, remove JP5, JP7 and the dual op-amp. This avoids potentially loading the power supplies with 50Ω, shorting the op-amp output or shorting the external reference. Note that V_{RT} must be more positive than V_{RB}, since the positive reference voltage must be greater than the negative reference voltage on chip.

4. INPUT SIGNAL GENERATOR - A clean, low distortion sine wave generator is used as a signal source. A band pass filter is sometimes required to further reduce harmonics and band limit noise as shown. The BNC coax connector labeled A_{IN} accepts the analog input. An op amp (AD843) is used to amplify this input and provide low source impedance to drive the A/D under test. This input can be used for single ended inputs or applying a DC offset for level shifting the Dither input. JP2 50Ω terminates this input. The socket has a standard 741 type pin out which allows experimentation with alternative amplifiers.

5. DITHER INPUT SIGNAL GENERATOR - The cross plot test configuration (described later) requires a triangle wave signal source. This signal is added through the BNC connector labeled DITHER (an inverting input with gain of 1/20). JP1 connects this input to ground via a 50Ω resistor.

6. OSCILLOSCOPE - The output of a reconstruction DAC, TP4, is used to drive the vertical input of the oscilloscope for manual linearity testing using the "cross plot" method. The reconstruction DAC is simply a resistor implementation using R15 through R19.

7. DSP - Evaluation of dynamic and static performance is done by external processing devices that perform histogram and harmonic analysis to determine characteristics like linearity, noise, distortion, intermodulation effects, etc. The data is available at the 28 pin connector labelled D0 through D11. Each output pin is complemented by a ground pin. The external clock output is available on two pins labelled PTS. The output data on the 28 pin connector is valid when the PTS clock is high.

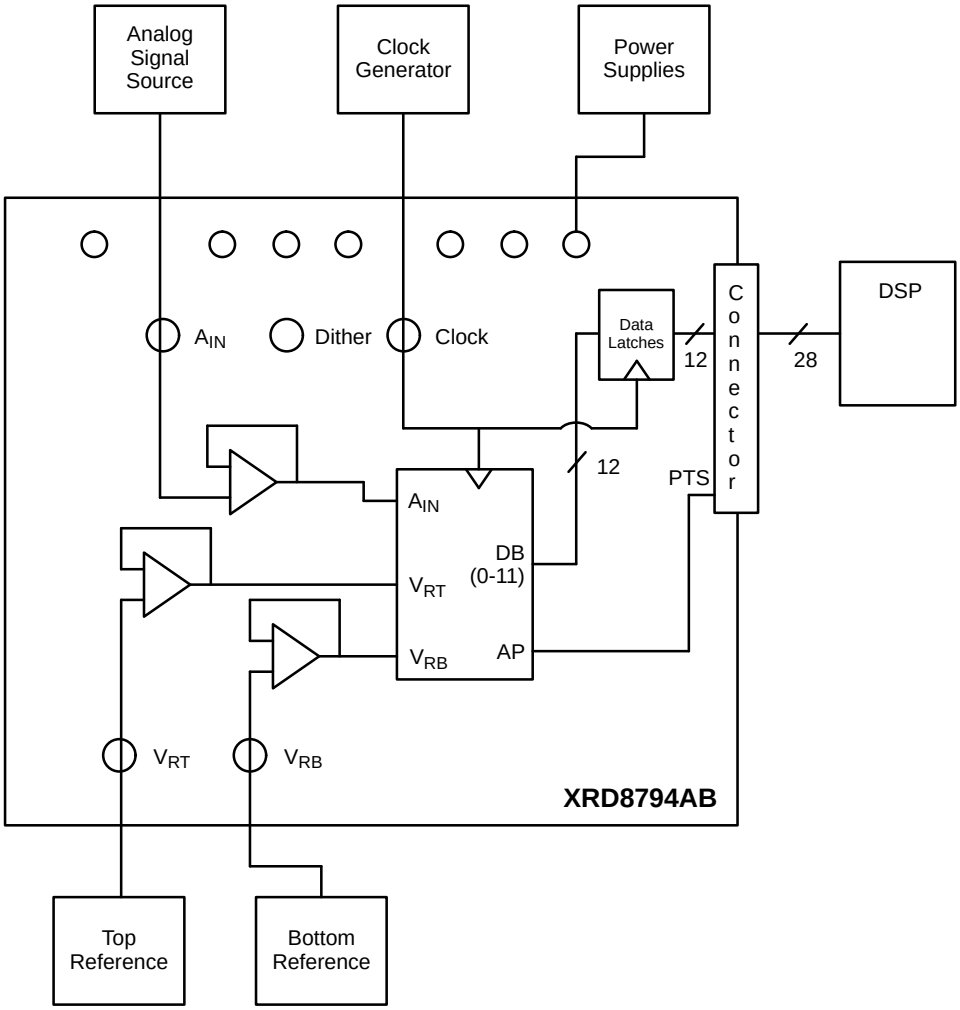

Figure 4. Default A/D Test Circuit with Fixed Reference

Optional Equipment

1. EXTERNAL PRECISION OUTPUT DAC - As an alternative to DSP, a high speed precision digital-to-analog converter can reconstruct the output in analog form. The analog measurements can be used to evaluate the A/D's performance using conventional analog instrumentation.

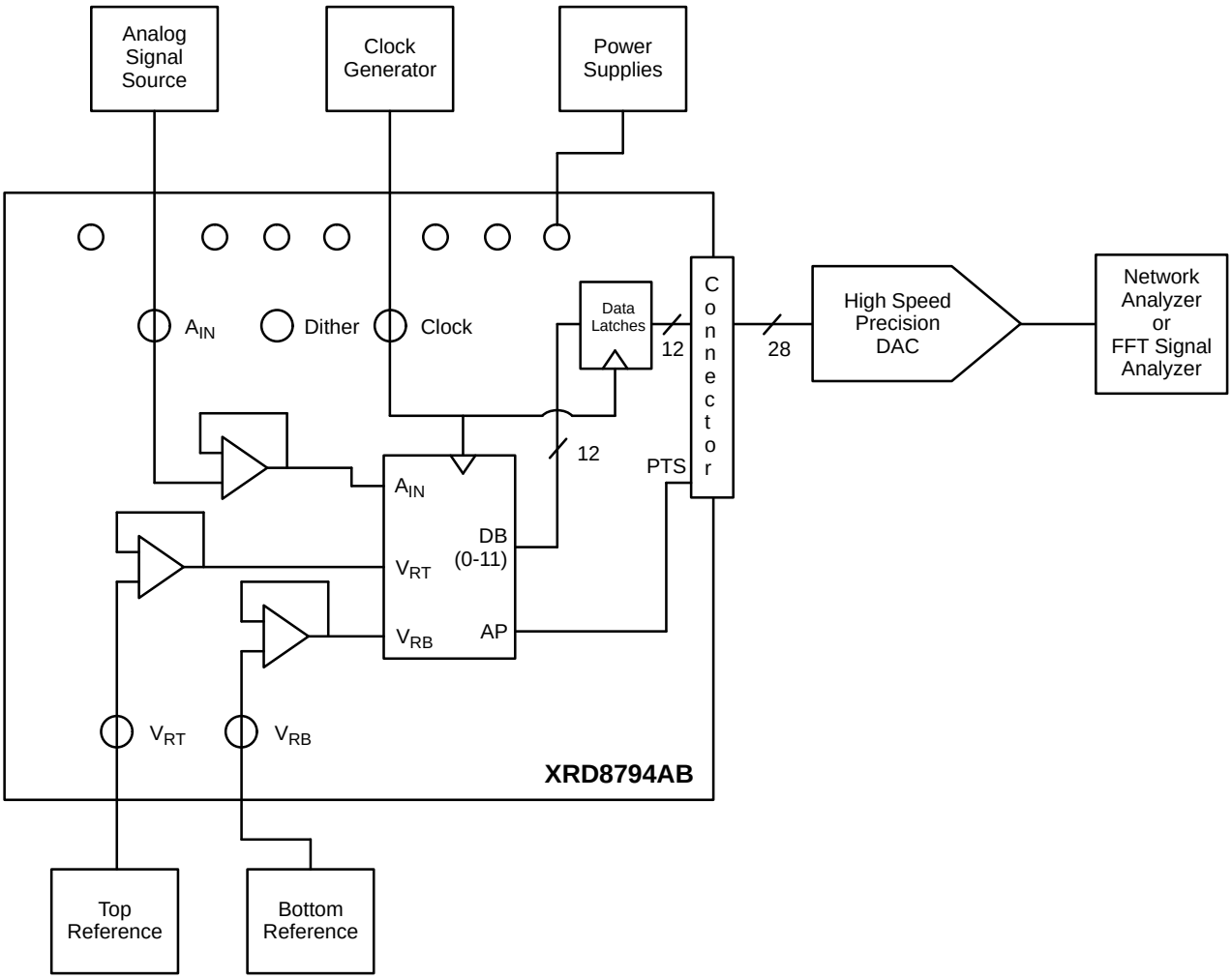

Figure 5. External Precision DAC Reconstruction Test

2. REFERENCE CONTROL DACS (PIXEL-BY-PIXEL ADJUSTMENT) - The reference voltage at the top (V_{RT}) and bottom (V_{RB}) of the A/D can be changed by external DACs on alternate CLOCK cycles to change offset and scale factor. The two DACs must have resolution and settling time characteristics consistent with the application. Note the decoupling capacitors at the reference pins have to be removed when V_{RT} and V_{RB} are driven dynamically. *Figure 6.* demonstrates the timing for dynamically adjusting the reference ladder of the XRD8794.

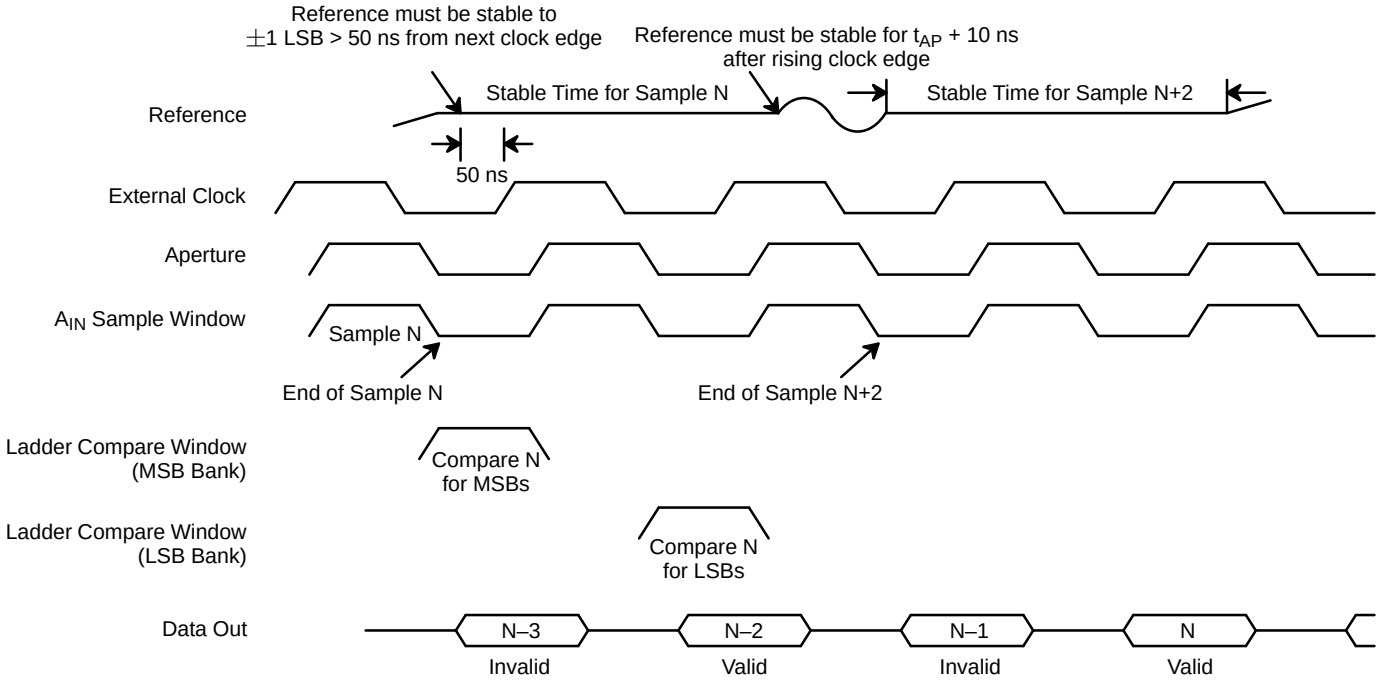

Figure 6. Timing For The Dynamically Adjusted Reference Ladder (Pixel-by-Pixel Adjustment)

SYSTEM OPERATION

Reference Inputs

With the reference op amps in circuit, the ADC's reference pins (V_{RB} and V_{RT}) are driven in an offset and range mode:

$$V_{RB} = V_{REF(-)},\ V_{RT} = V_{REF(-)} + V_{REF(+)}$$

Hence $V_{REF(-)}$ defines the offset and $V_{REF(+)}$ defines the span.

A_{IN} Input

If the DITHER input is left floating, then the input to the ADC (ADCIN) is given by:

$$ADC_{IN} = A_{IN}$$

If JP1 is in, then the input to the ADC (ADCIN) is given by:

$$ADC_{IN} = [1 + (R5 / (R3 + R2))\ ]\ A_{IN}$$

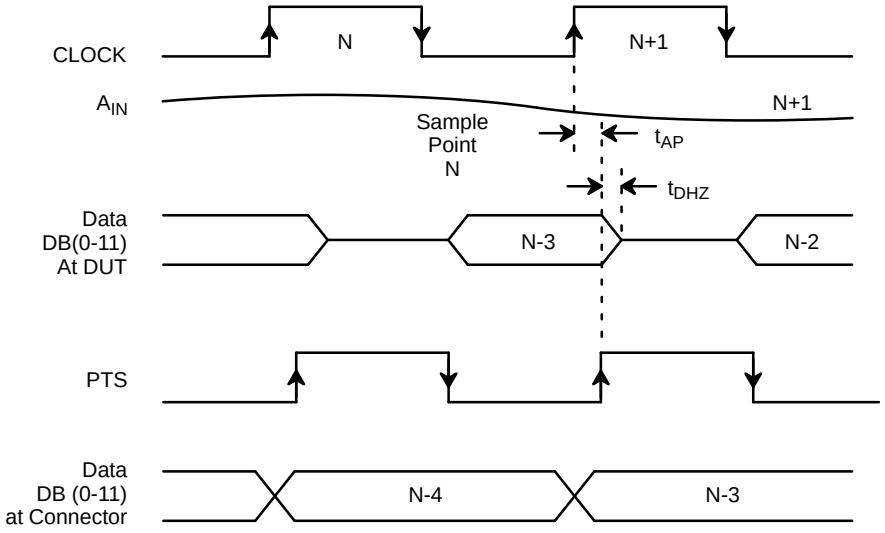

Figure 7. XRD8794AB Circuit Timing

DITHER with A_{IN}

Setting A_{IN} to a DC voltage and a signal applied to DITHER, then the input to the ADC (ADCIN) is given by:

$$ADC_{IN} = A_{IN} + (R5 / R3)(A_{IN} - DITHER)$$

Timing

Figure 7. demonstrates the circuit timing of the XRD8794AB. The CLOCK is provided by the user as specified on the XRD8794 data sheet. The PTS clock is an output that allows for synchronization of external lab equipment with the output data DB(0–11). DB(0–11) is valid after the rising edge of the PTS clock.

Outputs

The parallel digital output of the A/D can be accessed on the 28 pin connector. A system clock (PTS) is also available on that connector. This output data, in conjunction with various input stimuli, is used to evaluate the A/D and timing performance. The three common methods are described below.

DIGITAL SIGNAL PROCESSING

A comprehensive dynamic performance evaluation is most often done by using external hardware capable of fast data acquisition and storage. The computation of integral linearity, differential linearity, signal-to-noise and distortion ratios, the effective number of bits, and other useful figures of merit is done using software having histogram and FFT capability. The accuracy of the test results depends upon the quality of the input sinewave. A low distortion sinewave generator with a band pass filter will be necessary.

Commercial software packages with the needed computational features are available. The Tektronix PTS101 and other internally developed proprietary systems are used by EXAR to acquire and analyze the ADC data.

ANALOG TESTING WITH EXTERNAL DAC

The logic output of the system can be converted back to analog by using a high performance digital-to-analog converter. Laboratory spectrum analyzers and oscilloscopes can be used to measure linearity, frequency response, harmonic distortion, noise, intermodulation distortion, etc. These measurements can be converted to the specifications commonly used in specifying A/D's dynamically. In addition to a high quality sinewave input, the output digital-to-analog converter must be significantly more accurate than the A/D under test.

CROSS PLOT

An evaluation of differential linearity can be simply done with an oscilloscope, a triangle wave generator and a low noise DC signal source. Input BNCs are provided on the board so this "cross plot" method can be conveniently implemented (See *Figure 8.*) The oscilloscope must be set in the X-Y display mode.

A triangle wave (500 Hz) with a peak-to-peak amplitude of approximately 320 LSBs is supplied to the "DITHER" input. This is attenuated by a factor of R5/R3 by the input amplifier. The triangle wave is also used to drive the x axis of the scope. The horizontal gain is set so that 16 divisions are swept. Look at Test Point 4 (TP4) with the vertical input. Set the horizontal gain at about 2 LSB per division.

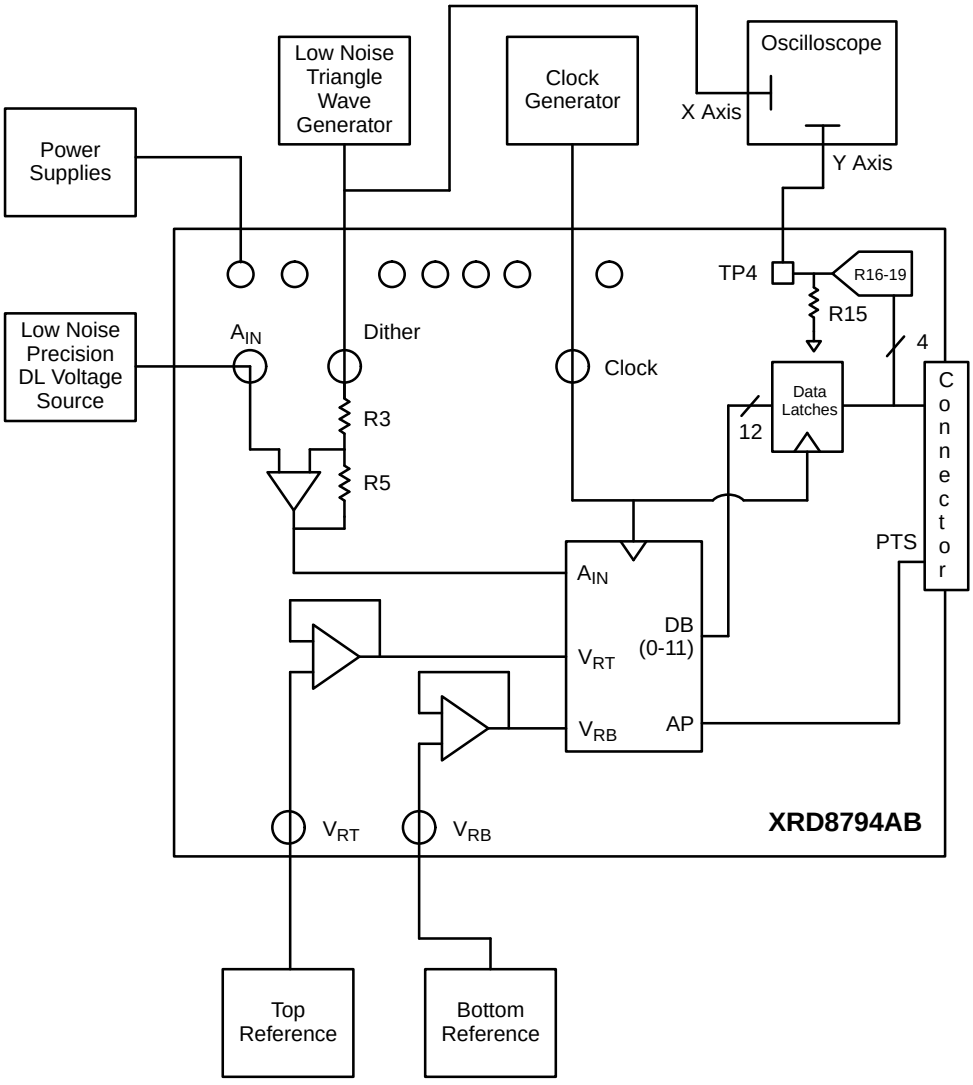

Figure 8. Crossplot Setup

A stair step waveform will result (See *Figure 9.*) By changing the DC input, sixteen code transitions can be observed about any DC input level. The horizontal distance between these transitions is the code width. Missing codes cause steps to be absent. By setting the end point thresholds to coincide with the scope grid lines, integral linearity errors are displayed as thresholds which are off-centered from these grid lines. A precision DC voltage source is necessary for the integral linearity measurement.

Since the conversion speed is much faster than the dither frequency, multiple readings are taken at each threshold. The horizontal variation of each threshold gives a qualitative measure of noise (in LSB's).

Using this "cross plot" method is a good way to prove out the lab setup prior to more sophisticated DSP test.

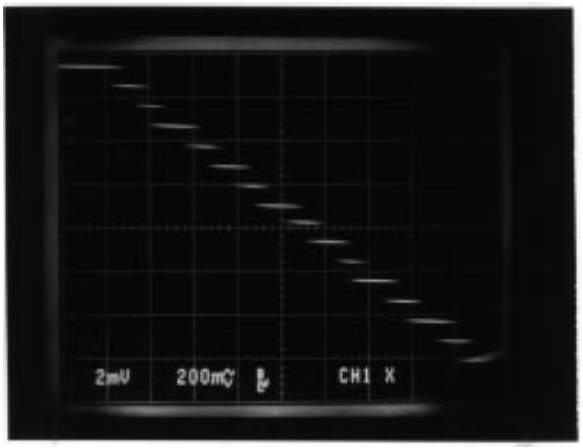

Figure 9. Crossplot Staircase Output

JUMPER OPTIONS

The XRD8791AB offers flexibility through configuration determining jumpers. These optional jumpers furnish choices for (1) input termination resistors, (2) bypassing of the reference input buffers, and (3) the selection of several logic and clock options. *Table 1.* shows the jumper functions along with the default configuration set-up prior to shipment.

Termination Options

Termination resistors (50 Ω) can be added to the four analog input coax BNC connectors as indicated in *Table 1.* Note that the CLOCK input termination is not optional.

Bypass Options

The reference input buffers can be bypassed with JP5 and JP7. The V_{RB} pin of the A/D is grounded if JP6 is inserted. The V_{RT} pin of the A/D is connected to AV_{DD} if JP8 is inserted. Remove U3, the dual op amp (EL2224), JP5, and JP7 when using these unbuffered modes.

Logic Options

A digital logic work area is provided if logic options or timing issues are to be characterized. The work area has 100 mil spaced holes with several pads dedicated to digital ground and the digital power supply.

MP8791 IN THE XRD8794AB

The XRD8794 is pin-for-pin compatible with the MP8791. An XRD8794AB can therefore be used to characterize the MP8791. The MP8791 has one functional difference that should be considered when evaluating the product. Digital outputs of the MP8791 are not placed in a high impedance state when the DUT clock is high. This can be done however, by connecting the MP8791 $\overline{OE}$ to the aperture output pin (*Figure 10.*) In either mode, the XRD8794AB will capture data from the output of an MP8791. If system timing is implemented in another fashion please refer to the individual data sheets to ensure proper operation.

XRD87L94 3V Operation

The XRD87L94 can be evaluated in the XRD8794AB by simply lowering DUT AVDD and DUT DVDD to 3V. Typically, the 74377 latches can remain operating from the 5V provided by the separate power supply +5V DIGITAL. If 3V logic is also to be evaluated, then lower +5 DIGITAL to 3V and swap out the 74377s.

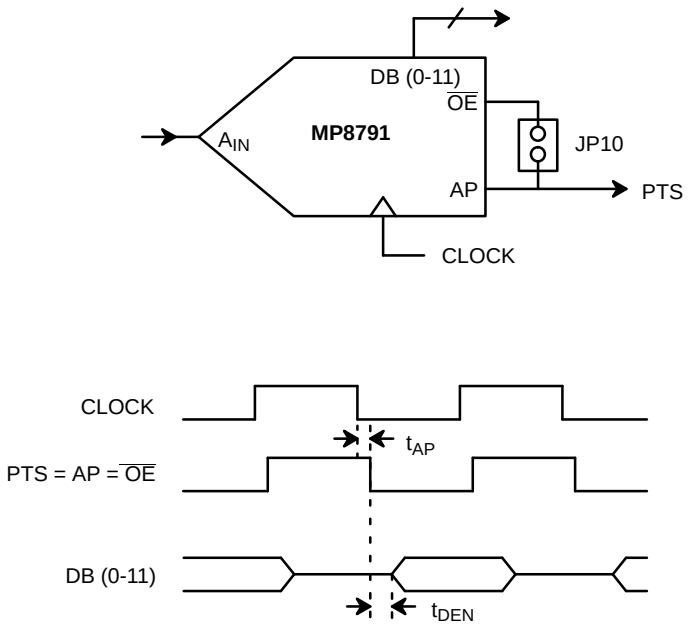

Figure 10. MP8791 Does Not High Z When Clock Is High Unless $\overline{OE}$ Is Connected To The Aperture Output Pin

FINAL DESIGN CONSIDERATIONS

After the XRD8794AB has been used to demonstrate that the XRD8794, the clock timing, and the analog support circuits are acceptable, the design must be successfully transferred to the user's system. A close copy of the proven layout is recommended as is the use of identical support devices. Where this is not possible, the following advice should be heeded:

1. Be generous with analog and digital ground planes. Mirror the ground plane with the supply planes. Use a 5 mil power / ground plane separation if a four layer board can be used.

2. Keep high frequency decoupling capacitors very close to the A/D pins and minimize the loop area included so less flux will induce less noise. Use decoupling capacitors in the same locations as on the XRD8794AB.

3. Coupling between logic signals and analog circuitry can easily change a 12-bit system into an 8-bit system or worse. Completely separate them. Watch for coupling opportunities from other sources not immediately associated with the A/D. Don't use switching power supplies in adjacent locations for example.

4. Slow down the rising and falling edge of the input CLOCK signal to minimize clock energy feedthrough.

5. Use support devices equivalent to those used on the evaluation board. Use the application board to verify these devices up front, i.e. use very linear passive components in the signal path.

6. Select a driving op amp whose noise, speed, and linearity fits the application.

7. Decoupling capacitors on pins R1, R2 and R3 do not improve the ADC's performance.

Termination of Input Coax Cables		
Jumper	**Description**	**Default**
JP2	Connecting adds 50 Ω from A_{IN} to AGND	IN
JP1	Connecting adds 50 Ω from DITHER to AGND	OUT
JP4	Connecting adds 50 Ω from V_{RT} to AGND	OUT
JP3	Connecting adds 50 Ω from V_{RB} to AGND	OUT
Reference Amplifier/Buffer Bypass (2.)		
JP7	Connecting shorts coax V_{RT} Jack to V_{RT} pin of ADC	OUT
JP5	Connecting shorts coax V_{RB} Jack to V_{RB} pin of ADC	OUT
JP6	Connecting shorts V_{RB} (at pin of ADC) to AGND	OUT
JP8	Connecting shorts V_{RT} (at pin of ADC) to AV_{DD}	OUT
Logic and Clock Jumpers (1)		
JP9	(2,3) Binary Output Format (1,2) MSB Inverted	(2,3)
JP10	Connects Aperture Delay Sync to $\overline{OE}$	OUT

Notes:
1. Jx (a, b) means short pin a and pin b of jumper x.
2. When using the amplifier bypass jumpers, remove the op amps from the sockets.

Table 1. Jumper Options

TP1	A_{IN} of XRD8794
TP2	V_{RB} of XRD8794
TP3	V_{RT} of XRD8794
TP4	Crossplot Output

Table 2. Test Points

Qty	Value	Ref Designators
1	XRD8794	U1
1	AD843	U2
1	EL2224	U3
2	74ACQ377	U4, U5
9	Open	C31, C32, C33, C34, C36, C39, C40, C41, C42
7	0.01 uF	C12, C15, C6, C9, C37, C43, C48
9	0.1 uF	C13, C16, C7, C10, C29, C35, C19, C18, C45
14	10 uF	C8, C11, C14, C17, C21, C20, C30, C36, C44, C1, C2, C3, C4, C5
9	50 Ω	R2, R1, R4, R6, R13, R7, R12, R8, R14
1	150K Ω	R3
1	7.5K Ω	R5
2	SHORT	R11, R9
1	5.1K Ω	R19
1	10K Ω	R18
1	20K Ω	R17
1	40K Ω	R16
1	1K Ω	R15
12	100 Ω	R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33
5	BNC Connectors	A_{IN}, CLOCK, DITHER, V_{RT}, V_{RB}
4	Testpoints	TP1, TP2, TP3, TP4
1	3 Pin Jumper	JP9
9	2 Pin Jumpers	JP1 - JP8, JP10
2	8 Pin DIP Socket	SU2, SU3
1	28 Pin DIP Socket	SU1
7	Banana Connectors	-15V, +15V, AGND, DUT AV_{DD}, DUT DV_{DD}, DGND, +5V DIGITAL
1	28 Pin Header Connector	CON1
1	PCB	EXAR CORPORATION 8791 / 8794 Evaluation Board

Table 3. List of Components

PCB LAYOUT

A set of drawings showing the details of the electrical circuit and board layout are given in figures 11 through 16.

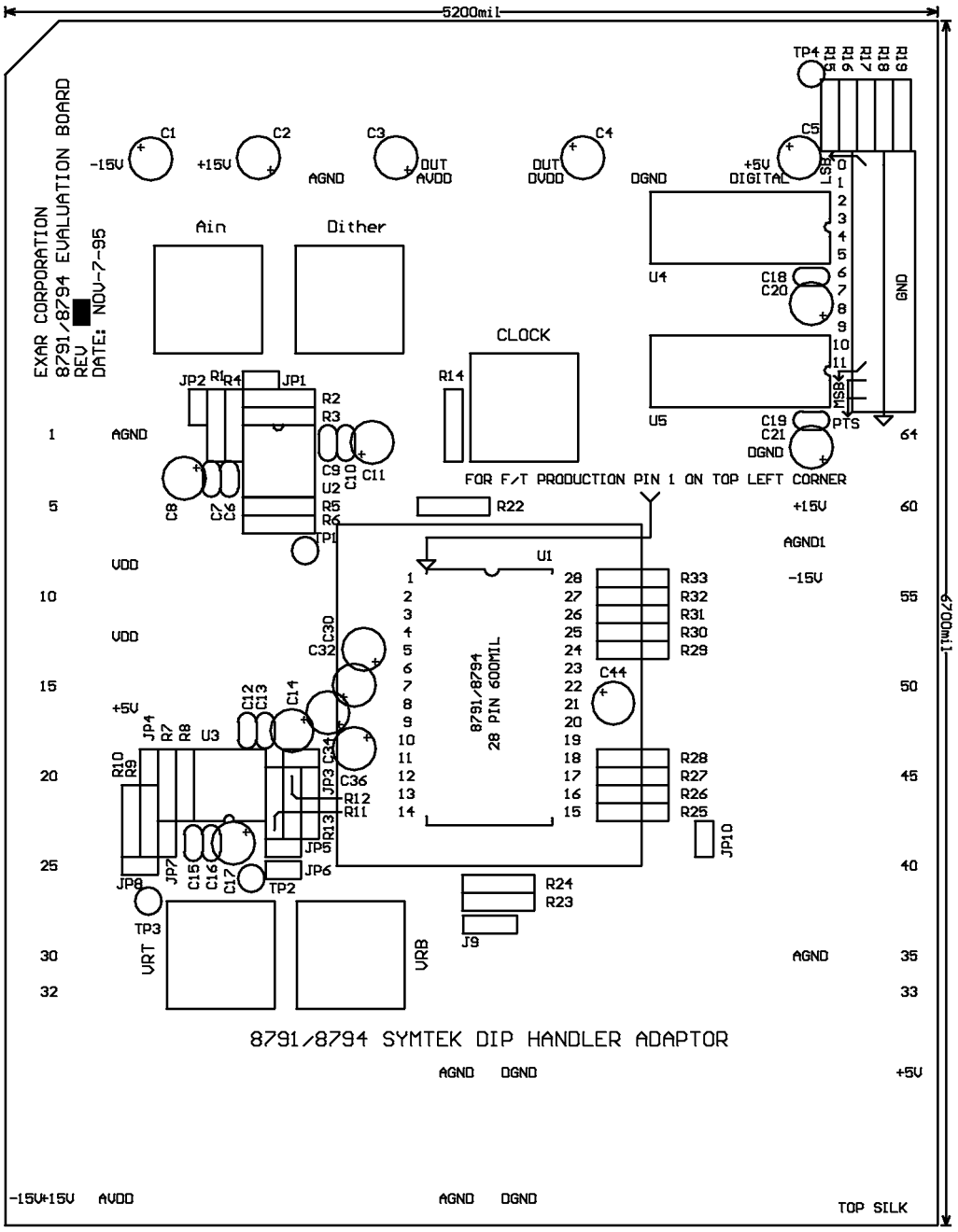

Figure 11. Top Silk

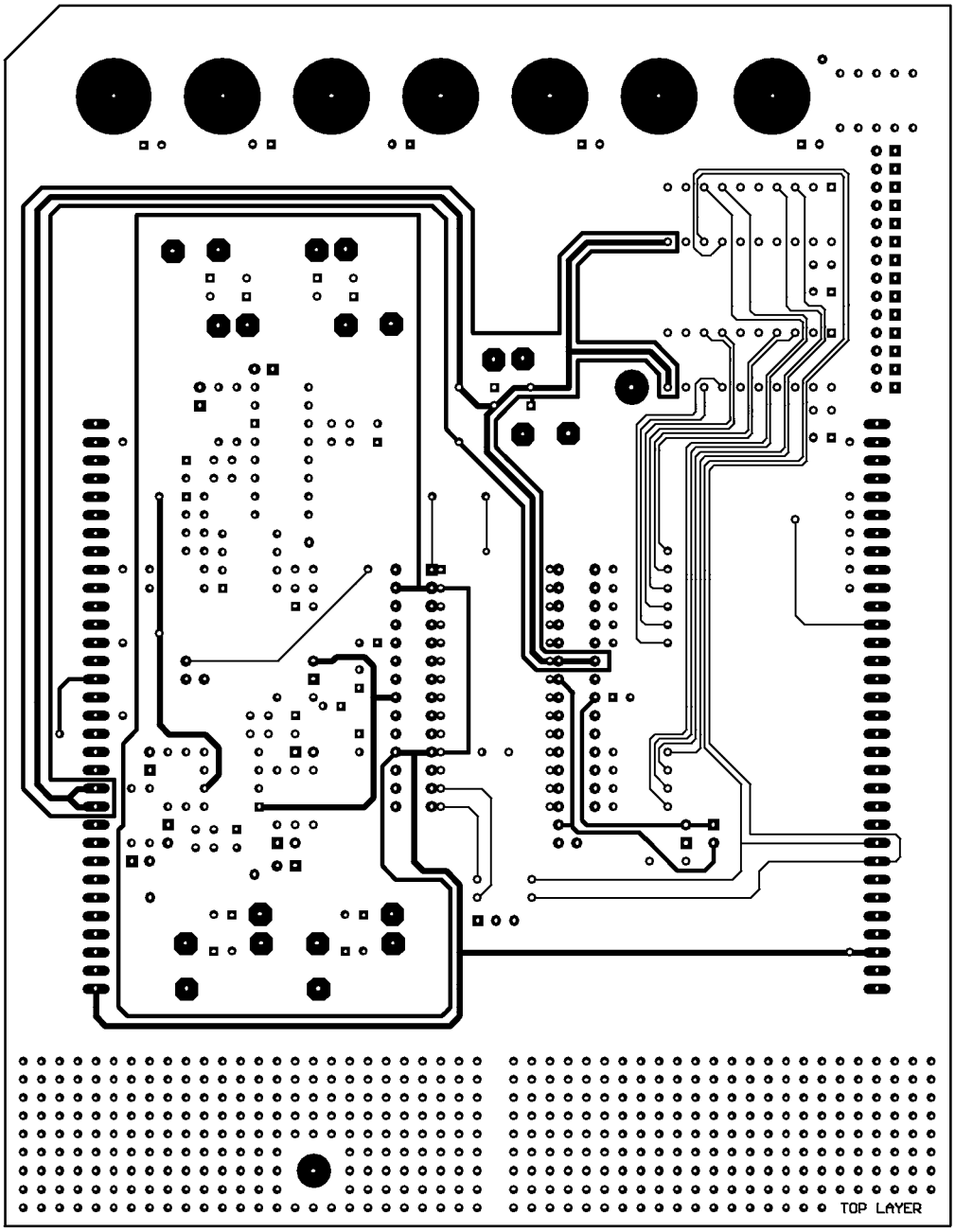

Figure 12. Top Trace

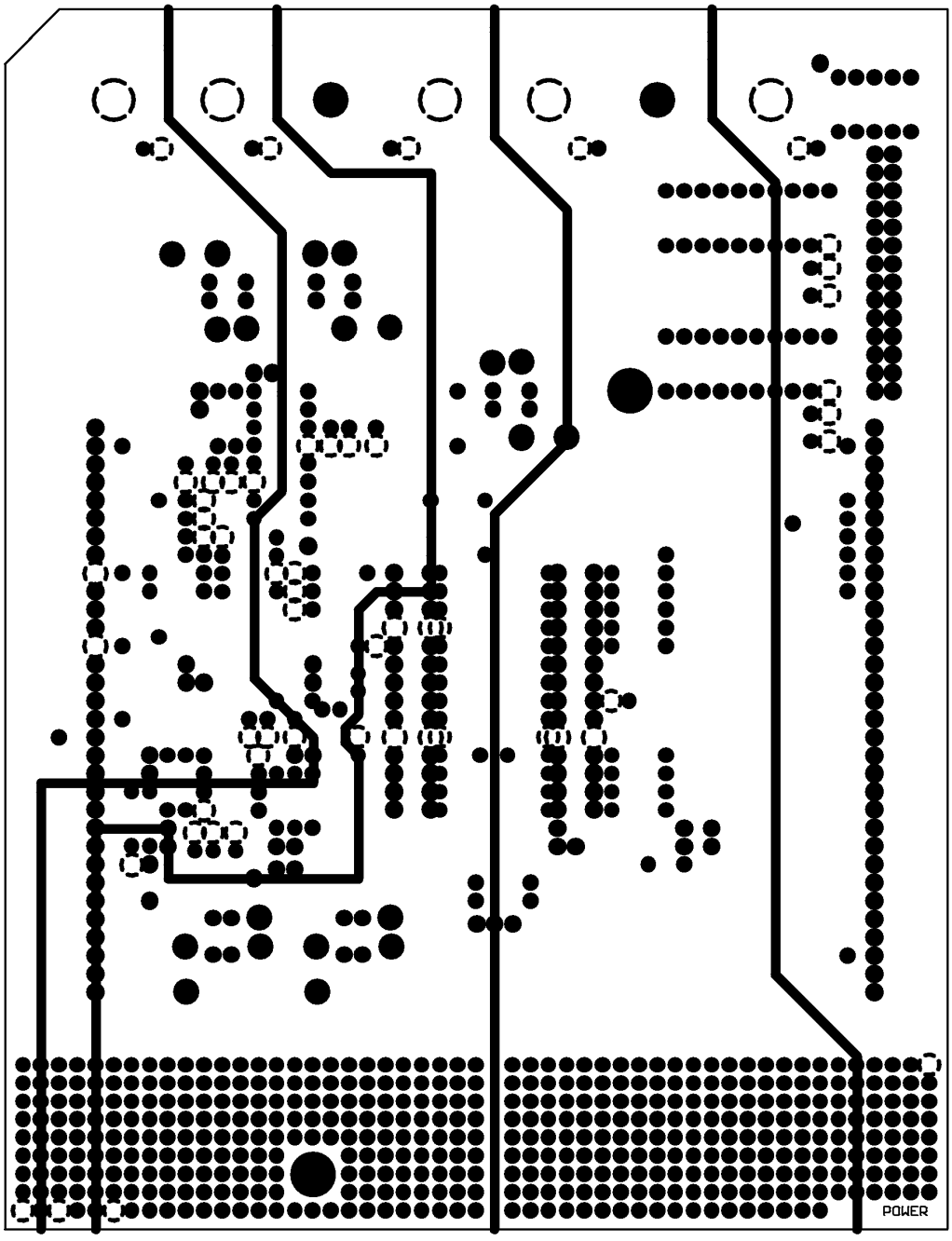

Figure 13. Power Plane

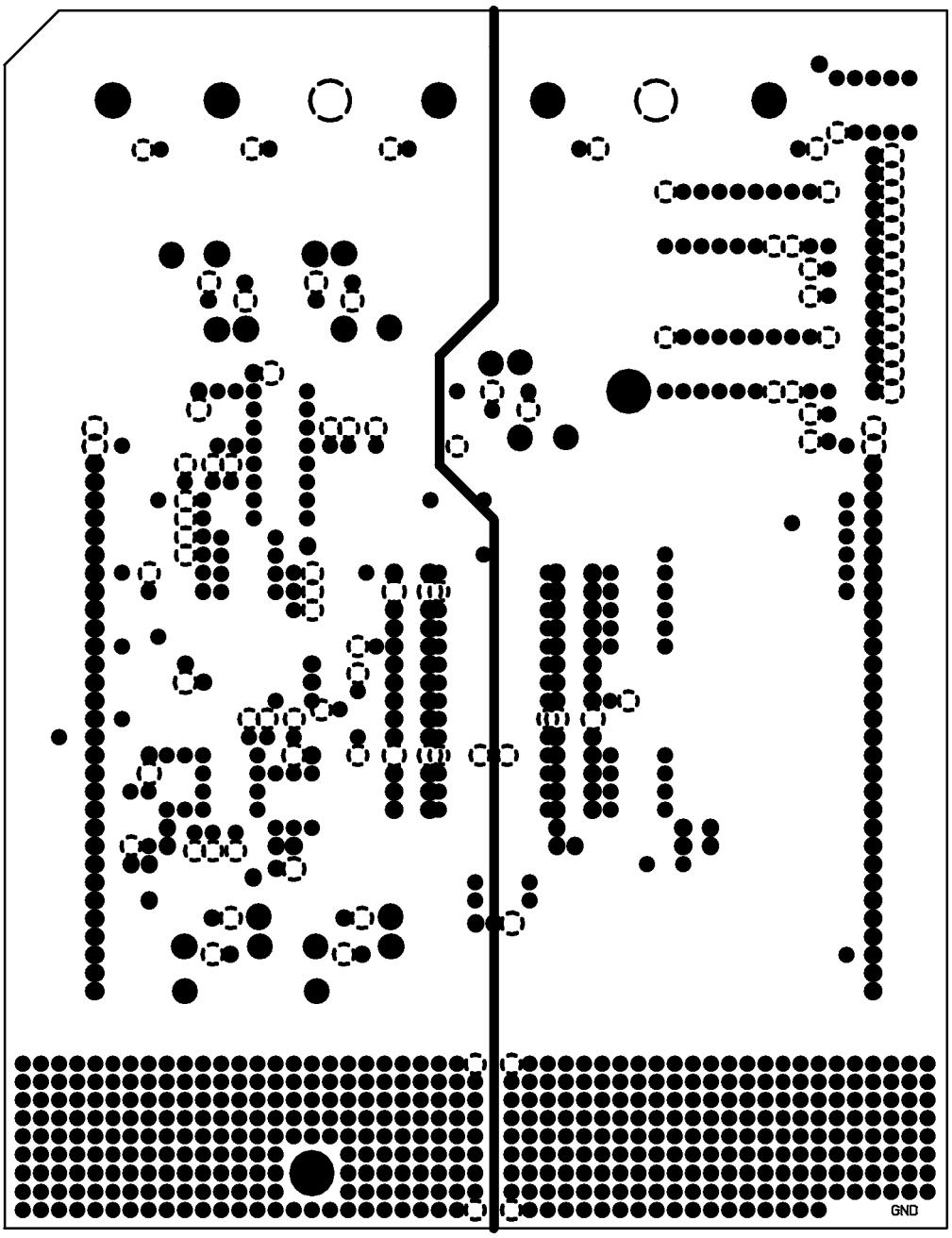

Figure 14. Ground Plane

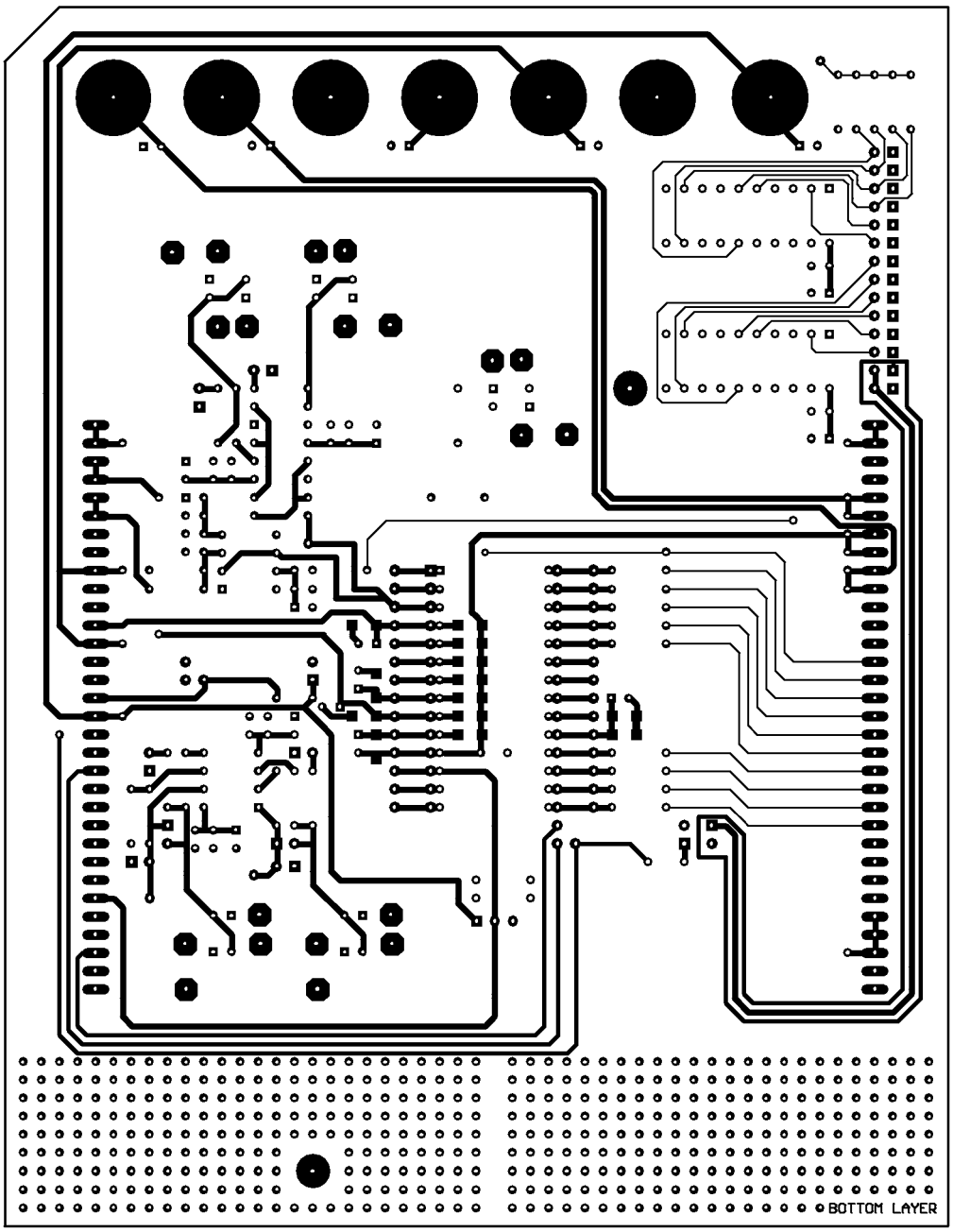

Figure 15. Bottom Trace

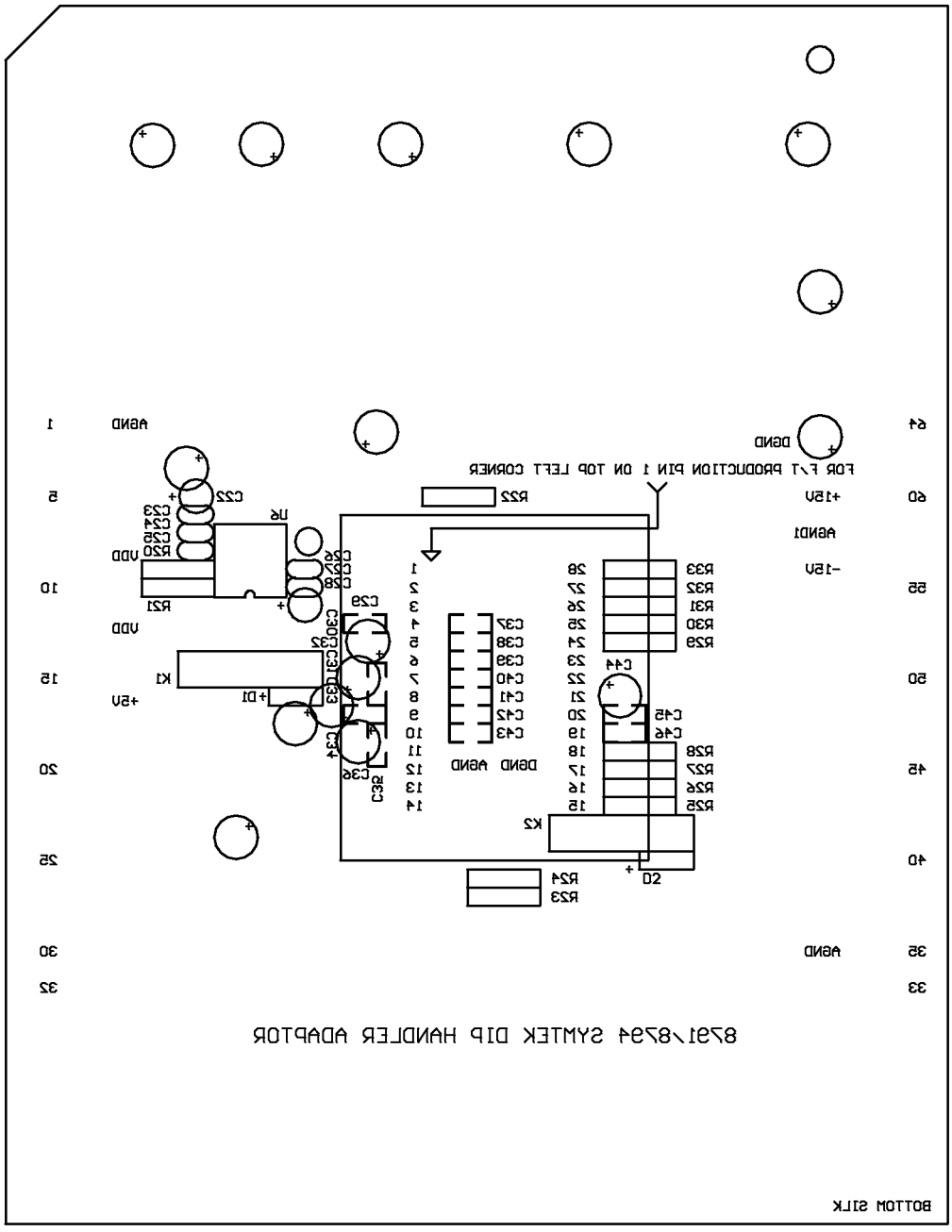

Figure 16. Bottom Silk

Notes

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