

FEATURES

- Internal R/C Oscillator
- Provides Seven Filters In One 14-pin Package
- Dual Inputs for Summing Left and Right Channels
- Provides 30dB of Gain
- Two Auxiliary Inputs
- Microprocessor Bus Interface
- On Chip A/D Converter

APPLICATIONS

- Graphic Equalizers
- Tape Recorders
- Receivers
- Portable Systems

GENERAL DESCRIPTION

The XR-1097 is a 7-point switched capacitor filter dedicated for use in audio applications. The 7 filters are spaced 1 1/2 octaves apart starting at 63Hz. The two filter inputs allow the left and right channels to be summed. This reduces the display space and prevents redundant audio information from being displayed. The 7 filter outputs, along with the peak value of all filters each go into a peak hold circuit with a slow decay time constant

(330ms). The eight filter outputs and 2 auxiliary inputs are multiplexed into an A/D converter which produces the digital output that is used by the system microprocessor.

The XR-1097 is fabricated in a low noise 2 micron double poly-silicon CMOS process and comes in a 14-pin plastic package. The device may be operated off of either $\pm 5V$ or $\pm 6V$ supplies. The chip oscillator operates at 400kHz and requires only an external resistor and capacitor.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-1097CP	14 Lead 300 Mil PDIP	-30°C to +75°C

BLOCK DIAGRAM

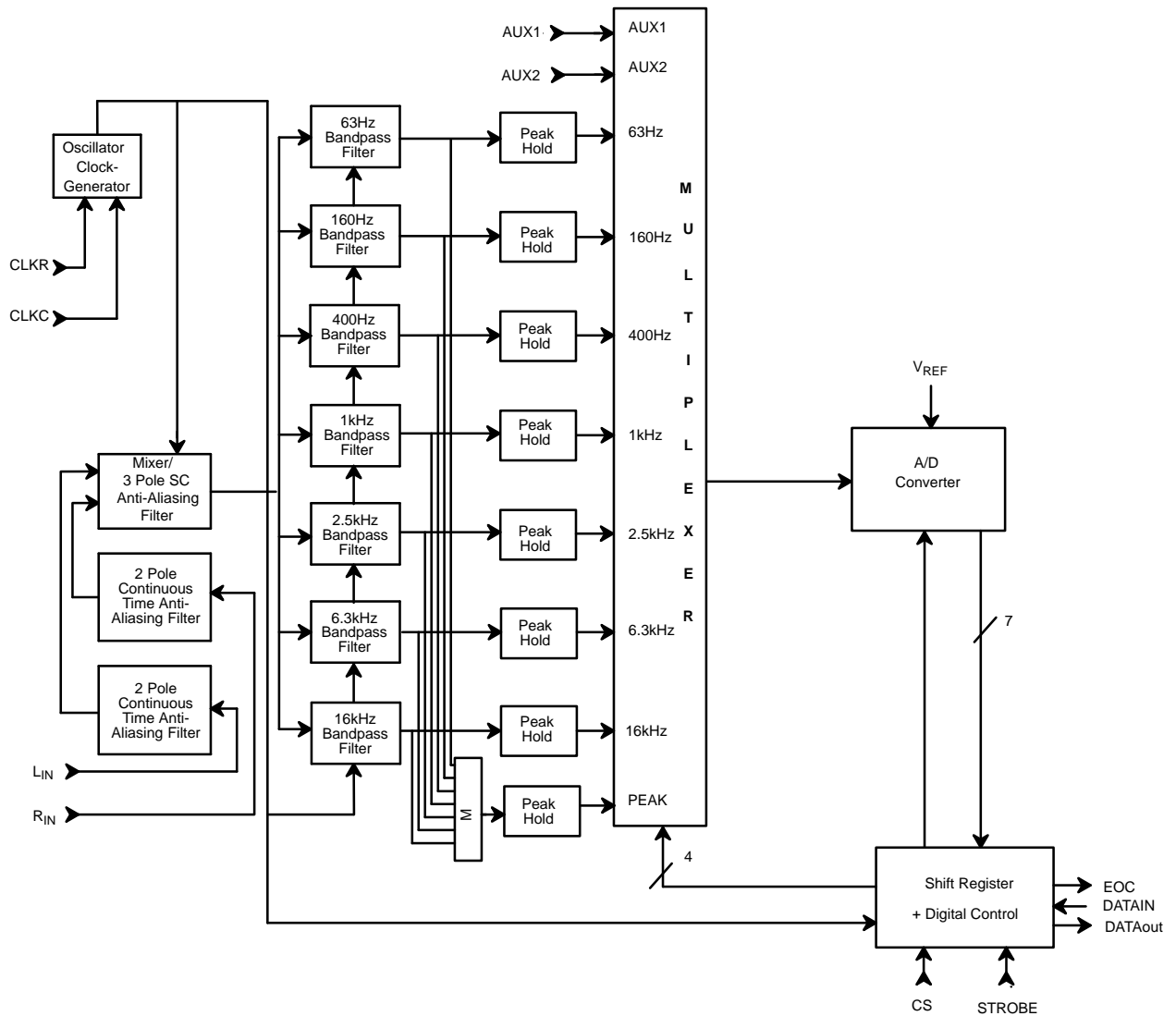
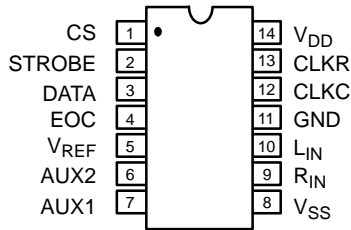


Figure 1. 7-Band Graphic Equalizer Display Filter with A/D Converter

PIN CONFIGURATION



14 Lead PDIP (0.300")

PIN DESCRIPTION

Pin #	Symbol	Description
1	CSB	Chip Select Pin
2	STROBE	Clock Pin To Shift In/Out Data Through the Serial Port
3	DATA	Serial Port For Digital Signals to and from Microprocessor
4	EOC	(A/D) End of Conversion Pin
5	V _{REF}	A/D Converter Reference Voltage Input
6	AUX2	Auxiliary Input 2
7	AUX1	Auxiliary Input 1
8	V _{SS}	Negative Supply Voltage
9	R _{IN}	Right Channel Input
10	L _{IN}	Left Channel Input
11	GND	Ground
12	CLKC	Clock Capacitor from this Pin to GND (C _{nom} = 1nF)
13	CLKR	Clock Resistor from this Pin to CLCC (R _{nom} = 14.6 kΩ)
14	V _{DD}	Positive Supply Voltage

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{DD} = +5V$, $V_{SS} = -5V$, $V_{REF} = 2.55V$, $T_A = 25^\circ C$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
General Characteristics						
V_{DD}	Positive Supply	4.75		6	V	
V_{SS}	Negative Supply	-6		-4.75	V	
I_{DD5}	Supply Current		8	15	mA	
Digital Pins						
V_{IL}	Input Voltage Low			0.5	V	
V_{IH}	Input Voltage High	4.5			V	
V_{OL}	Output Voltage Low			0.5	V	
V_{OH}	Output Voltage High	4.5			V	
Analog and Digital Inputs						
I_{IL}	Input Leakage Current	-2.0		+2.0	μA	
Oscillator Characteristics						
$TCLKRP$	Clock Frequency	380	400	420	kHz	$R=1.46k\Omega$ $C=1nF$
A/D Characteristics						
	Accuracy Error			8 ± 1	bit LSB	
V_{REF}	Reference Voltage		2.5		V	
$TCONV$	Conversion Time	400	80	440	μS	
Filter Characteristics						
FOS	Filter Offset	0		+200	mV	
FG63	Filter Gain 63Hz	1.08	1.28	1.52	V	INPUT=40mVpk
		28.5	30.0	31.5	dB	f _{IN} =63Hz
		2.15	2.55	2.55	V	INPUT=80mVpk
FG160	Filter Gain 160Hz	1.08	1.28	1.52	V	INPUT=40mVpk
		28.5	30.0	31.5	dB	f _{IN} =160Hz
		2.15	2.55	2.55	V	INPUT=80mVpk
FG400	Filter Gain 400Hz	1.08	1.28	1.52	V	INPUT=40mVpk
		28.5	30.0	31.5	dB	f _{IN} =400Hz
		2.15	2.55	2.55	V	INPUT=80mVpk
FG1K	Filter Gain 1kHz	1.08	1.28	1.52	V	INPUT=40mVpk
		28.5	30.0	31.5	dB	f _{IN} =1kHz
		2.15	2.55	2.55	V	INPUT=80mVpk
FG2.5K	Filter Gain 2.5kHz	1.08	1.28	1.52	V	INPUT=40mVpk
		28.5	30.0	31.5	dB	f _{IN} =2.5kHz
		2.15	2.55	2.55	V	INPUT=80mVpk
FG6.3K	Filter Gain 6.3kHz	1.08	1.28	1.52	V	INPUT=40mVpk
		28.5	30.0	31.5	dB	f _{IN} =6.3kHz
		2.15	2.55	2.55	V	INPUT=80mVpk

ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
FG16K	Filter Gain 16kHz	1.08	1.28	1.52	V	INPUT=40mVpk
		28.5	30.0	31.5	dB	fIN=16kHz
		2.15	2.55	2.55	V	INPUT=80mVpk
GPK	Peak Gain	1.08	1.28	1.52	V	INPUT=40mVpk
		28.5	30.0	31.5	dB	fIN=1kHz
		2.15	2.55	2.55	V	INPUT=80mVpk

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage $\pm 7V$

Storage Temperature -60 to +150°C

SYSTEM DESCRIPTION

The XR-1097 generates its clocks with an internal oscillator and does not require an external clock source. This allows the designer to place the XR-1097 on any application where an active filter design is in place. The XR-1097 provides bandpass filters with center frequencies at 63Hz, 160Hz, 400Hz, 1kHz, 2.5kHz, 6.3kHz, and 16kHz. These frequencies are standards in the consumer audio industry. The peak detector outputs referenced to 0V are multiplexed into an A/D converter.

The digital interface allows the system microprocessor to control the multiplexer and the A/D externally. All digital I/O (including A/D output) goes through a serial port. All digital inputs are TTL compatible, and all digital outputs swing from GND to V_{DD} .

The XR-1097 contains a continuous time anti-aliasing filter with a corner frequency of 80kHz. This prevents most signals from affecting the performance of the filters.

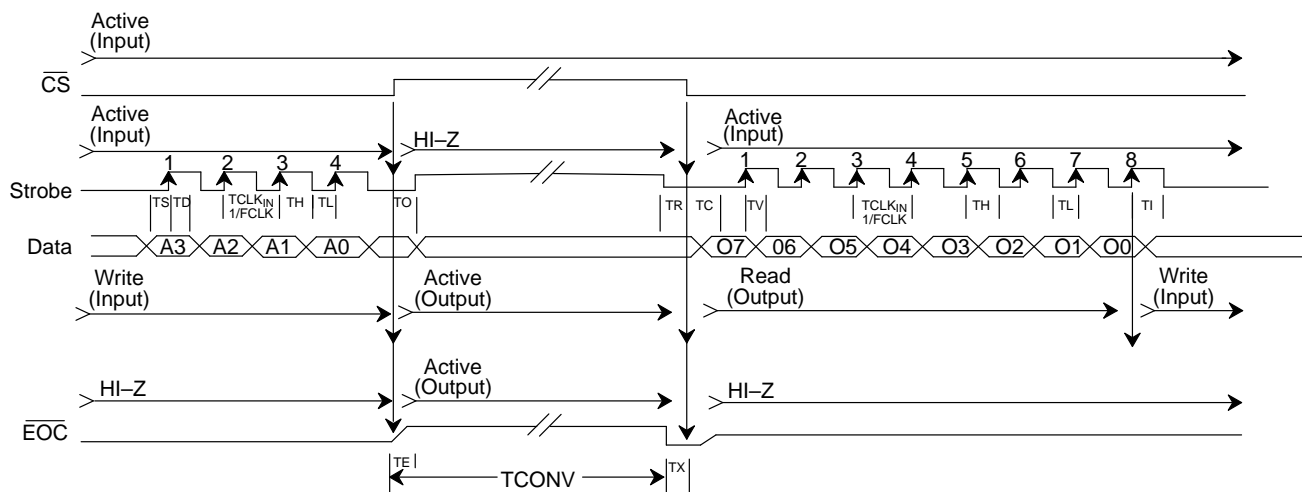


Figure 2. Microprocessor Interface Timing Diagram

Symbol	Parameter	Min.	Max.	Units
FCLK	STROBE Frequency ¹		2.5	MHz
TH	STROBE High Pulse Width	160		ns
TL	STROBE Low Pulse Width	160		ns
TS	DATA Set-Up Time	100		ns
TD	DATA Hold Time	100		ns
TO	STROBE Hold Time ²	100		ns
TE	EOC Delay Time ³	100		ns
TCONV	A/D Conversion Time ⁴	400	440	μs
TR	STROBE Set-Up Time ⁵	100		ns
TK	EOC to CSB	100		ns
TC	CSB to Q7	150		ns
TV	STROBE to Q6-Q0	150		ns
TI	STROBE to DATA Write Mode ⁶	150		ns

Table 1. Timing Characteristics

Notes

¹ TCLK=400ns. minimum.

² STROBE needs to be held low for TO after CSB goes high. After TO, STROBE becomes hi-z and DATA becomes an output port.

³ After TE, EOC becomes a logical high.

⁴ After TCONV, EOC goes low, signaling the end of conversion.

⁵ STROBE needs to be held low for TR before CSB goes low.

⁶ After TI, DATA goes back to an input port.

A3	A2	A1	A0	SELECTION
0	0	0	0	63Hz
0	0	0	1	160Hz
0	0	1	0	400Hz
0	0	1	1	1kHz
0	1	0	0	2.5kHz
0	1	0	1	6.3kHz
0	1	1	0	16kHz
0	1	1	1	PEAK
1	0	0	0	AUX1
1	0	0	1	AUX2
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

Table 2. Multiplexer Selection

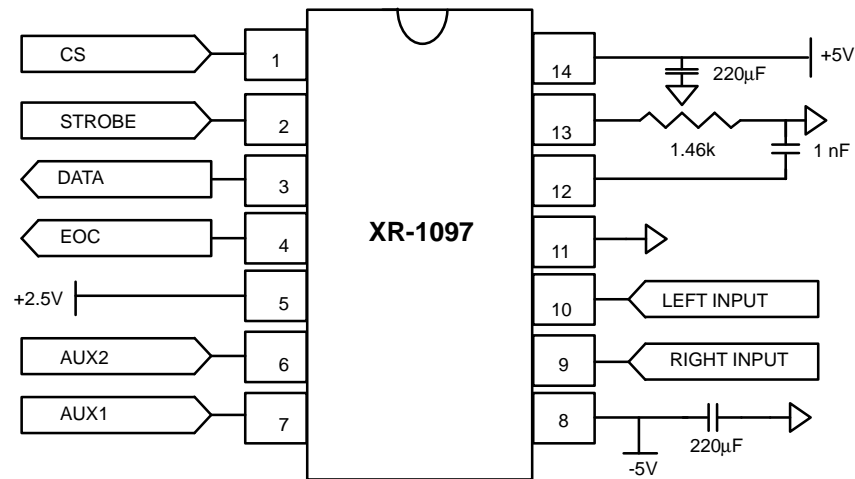
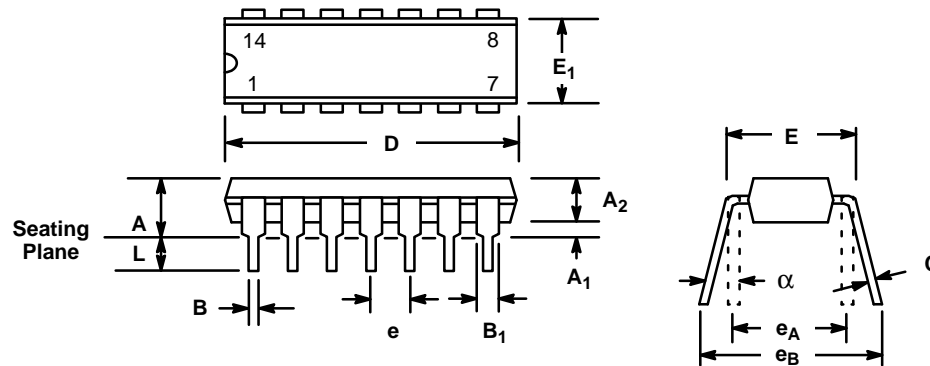


Figure 3. Typical Application Schematic

14 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A ₁	0.015	0.070	0.38	1.78
A ₂	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B ₁	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.725	0.795	18.42	20.19
E	0.300	0.325	7.62	8.26
E ₁	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e _A	0.300 BSC		7.62 BSC	
e _B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

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