XR-1090A

Graphic Equalizer Display
Filter Detector

...the analog plus company™

September 1996-4

FEATURES

- Internal R/C Oscillator
- Provides Seven Filters in one 14-pin Package
- Dual Inputs for Summing Left and Right Channels
- Provides 32dB of Gain
- Low Noise CMOS
- Electrostatic Discharge (ESD) Protection

APPLICATIONS

- Graphic Equalizers
- Tape Recorders
- Receivers
- Portable Systems

GENERAL DESCRIPTION

The XR-1090A is a single output switched-capacitor band pass filter dedicated for use in audio applications. XR-1090A has one output, with the ability to switch to one of seven different center frequencies. The output provides a peak hold for use with most display circuits. The two inputs allow the left and right channels to be summed. This reduces the display space and prevents redundant audio information from being displayed.

The XR-1090A is available in a 14-pin plastic DIP. The XR-1090A is fabricated in 2-micron double polysilicon CMOS for low noise and low clock feedthrough. The nominal operating voltages are ±5 VDC to ±6 VDC. The self-contained oscillator is designed to operate at 400 kHz with an external resistor and capacitor.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-1090ACP	14 Lead 300 Mil PDIP	-30°C to +75°C

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

BLOCK DIAGRAM

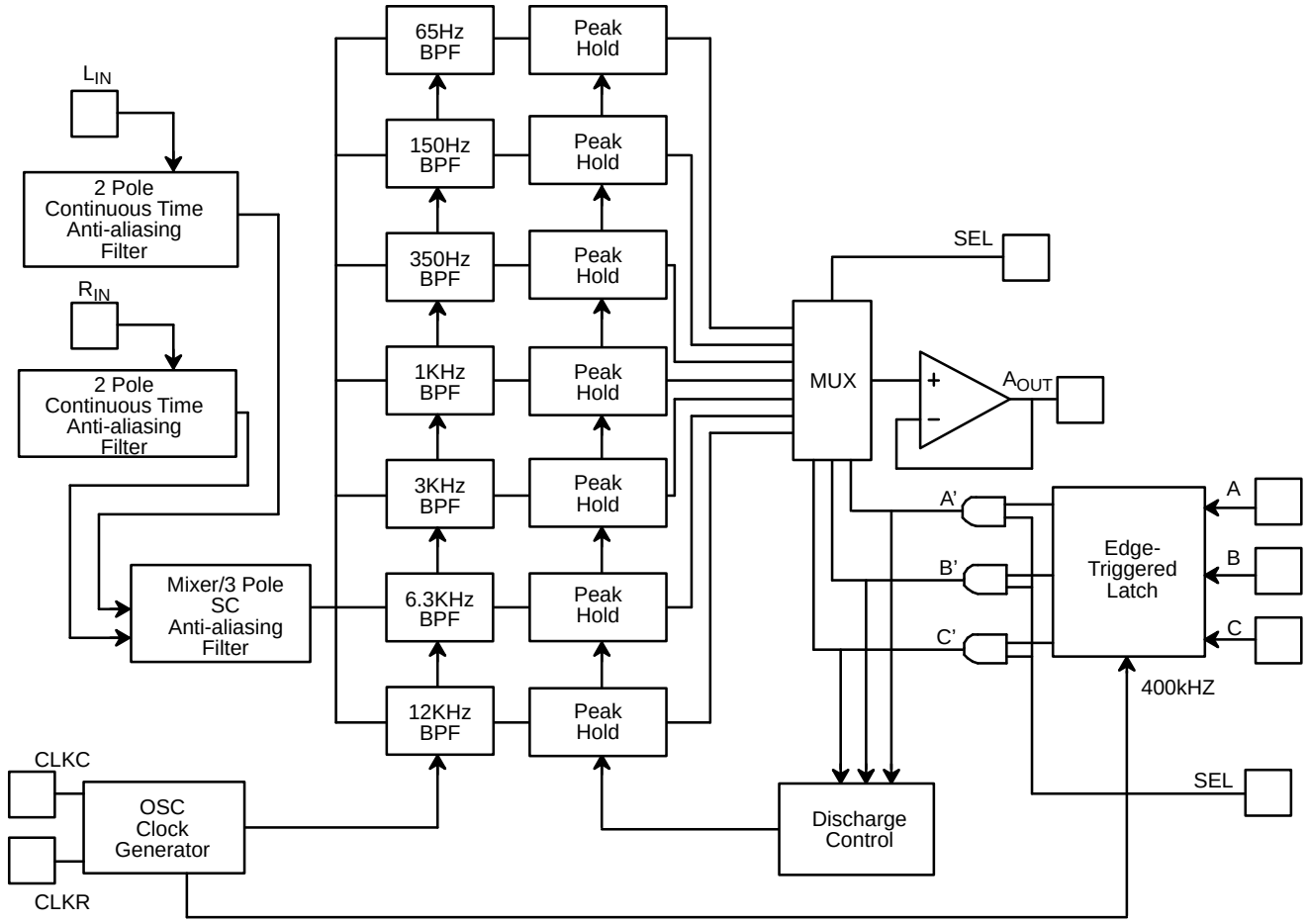
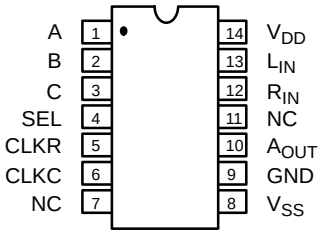


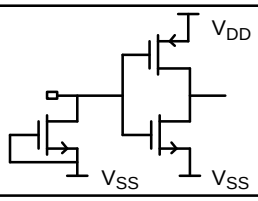
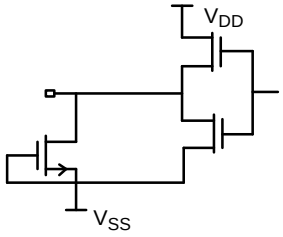
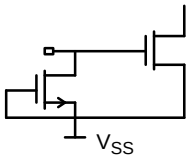
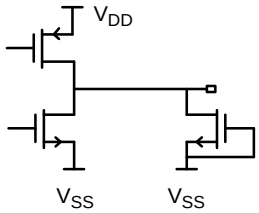
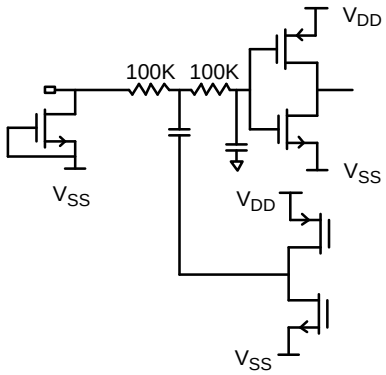
Figure 1. XR-1090A Functional Block Diagram
Graphic Equalizer Display Filter Detector

PIN CONFIGURATION



14 Lead PDIP (0.300")

PIN DESCRIPTION

Pin #	Symbol	I/O	Equivalent Circuit	Description
1 2 3 4	A B C SEL	I		Multiplexer Control A Multiplexer Control B Multiplexer Control C Select
5	CLKR	O		Clock Resistor. The timing resistor would be tied from this pin to pin CLKC.
6	CLKC	I		Clock Capacitor. The timing capacitor should be tied to this pin to ground.
7	NC			No Connection
8	V_{SS}			Nominally -6 VDC. This should be decoupled with at least a 0.47µF capacitor to ground located as close as possible to this pin.
9	GND			Ground for both Digital and Analog
10	A_{OUT}	O		Peak Hold Output
12 13	R_{IN} L_{IN}	I		Right Channel Input. The input impedance of this pin is greater than $1 \times 10^6\ \Omega$. Left Channel Input. The input impedance of this pin is greater than $1 \times 10^6\ \Omega$.
14	V_{DD}	I		Nominally tied to +6 VDC. This pin should be decoupled with a 0.47µF capacitor to ground located as close as possible to this pin.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = +6 VDC, V_{SS} = -6 VDC, T_A = 25°C, S_1, S_2 to ground, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$I_{DD}5$	Supply Current		10.0		mA	V_{DD} = +5 VDC, V_{SS} = -5 VDC
$I_{DD}6$	Supply Current		10.7	18.0	mA	V_{DD} = +6 VDC, V_{SS} = -6 VDC
I_{IL}	Input Leakage	-10		+10	µA	
TCLKRP (R-C)	Clock Freq	385	400	415	KHz	R = 1.46 KΩ, C = 1 nF
ECLKR	External Clock Voltage	5			Vpp	$V_{CLK\ IN}$ = ± 2.5 Vpk
V_{OS}	Output Offset	-100	125	300	mV	L_{IN} = R_{IN} = 0, SEL = 1
A_{OUT}6K3R	6.3 KHz Output, R_{IN}	4.19	4.98	5.91	V	S_2 to signal source = 125 mVpk f_{IN}=6.3 KHz,
		30.5	32.0	33.5	dB	A=1, B=1, C=0, SEL=1
A_{OUT}65	65 Hz Output, L_{IN}	4.19	4.98	5.91	V	S_1 to signal source = 125 mVpk f_{IN} = 65 Hz
		30.5	32.0	33.5	dB	A=0, B=0, C=1, SEL=1
A_{OUT}150	150 Hz Output, L_{IN}	4.19	4.98	5.91	V	S_1 to signal source = 125 mVpk f_{IN} = 150 Hz
		30.5	32.0	33.5	dB	A=0, B=1, C=0, SEL=1
A_{OUT}350	350 Hz Output, L_{IN}	4.19	4.98	5.91	V	S_1 to signal source = 125 mVpk f_{IN} = 350 Hz
		30.5	32.0	33.5	dB	A=0, B=1, C=1, SEL=1
V_{OUT}1K	1 KHz Output, L_{IN}	4.19	4.98	5.91	V	S_1 to signal source = 125 mVpk f_{IN} = 1 KHz
		30.5	32.0	33.5	dB	A=1, B=0, C=0, SEL=1
A_{OUT}3K	3 KHz Output, L_{IN}	4.19	4.98	5.92	V	S_1 to signal source = 125 mVpk f_{IN} = 3 KHz
		30.5	32.0	33.5	dB	A=1, B=0, C=1, SEL=1
A_{OUT}6K3	6.3 KHz Output, L_{IN}	4.19	4.98	5.92	V	S_1 to signal source = 125 mVpk f_{IN} = 6.3 KHz
		30.5	32.0	33.5	dB	A=1, B=1, C=0, SEL=1
A_{OUT}12K	12 KHz Output, L_{IN}	4.19	4.98	5.92	V	S_1 to signal source = 125 mVpk f_{IN} = 12 KHz
		30.5	32.0	33.5	dB	A=1, B=1, C=1, SEL=1
T1	Output Valid			3.5	µs	Time from A, B, C select to A_{OUT} valid
T2	Filter Discharge			100	µs	Filter discharge time (3dB or below)
V_{IH}	Logical “1” Input Voltage	70% V_{DD}			V	
V_{IL}	Logical ”0” Input Voltage			30% V_{DD}	V	

Notes

Recommended power on sequence: V_{SS} first, followed by V_{DD}. When only 1 channel input is used, then the other input has to be grounded.

ABSOLUTE MAXIMUM RATINGS

V_{DD} . . . . . +7 VDC

V_{SS} . . . . . -7 VDC

Power Dissipation

14-Pin Plastic Dip . . . . . 650 mW

derate above 25°C . . . . . 5 mW/°C

Storage Temperature . . . . . -60°C to +150°C

SYSTEM DESCRIPTION

The XR-1090A, unlike most switched-capacitor filters, does not require an external clock source in order to provide the sampling clocks. This allows the designer to place the XR-1090A in any application where an active filter design is in place. The XR-1090A provides band-pass filters with center frequencies at 65 Hz, 150 Hz, 350 Hz, 1 kHz, 3 kHz, 6.3 kHz, and 12 kHz. These frequencies are standards in the consumer audio market. One of these outputs will be displayed at a time, depending on the filter selected. Digital inputs are CMOS levels.

The XR-1090A contains a continuous time anti-aliasing filter with a corner frequency of 80 kHz. This prevents most signals from affecting the performance of the filters.

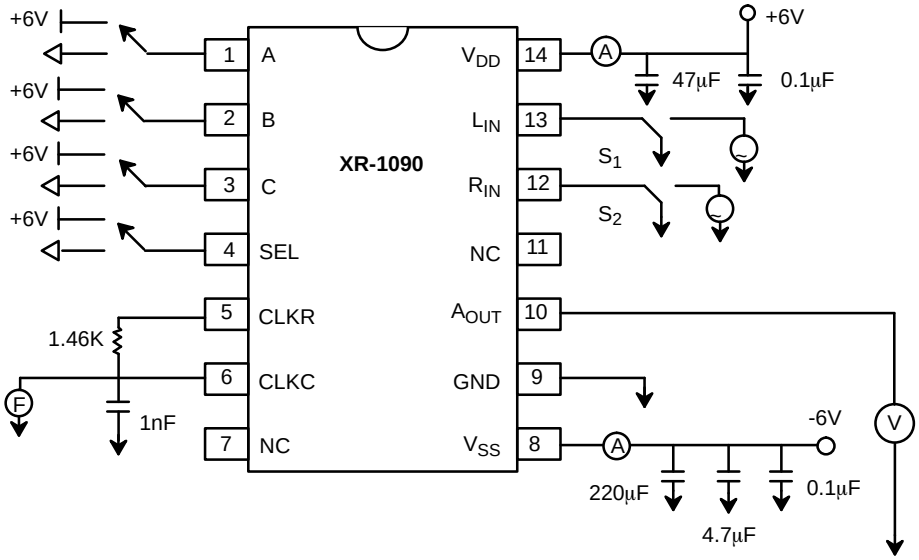


Figure 2. Test Circuit

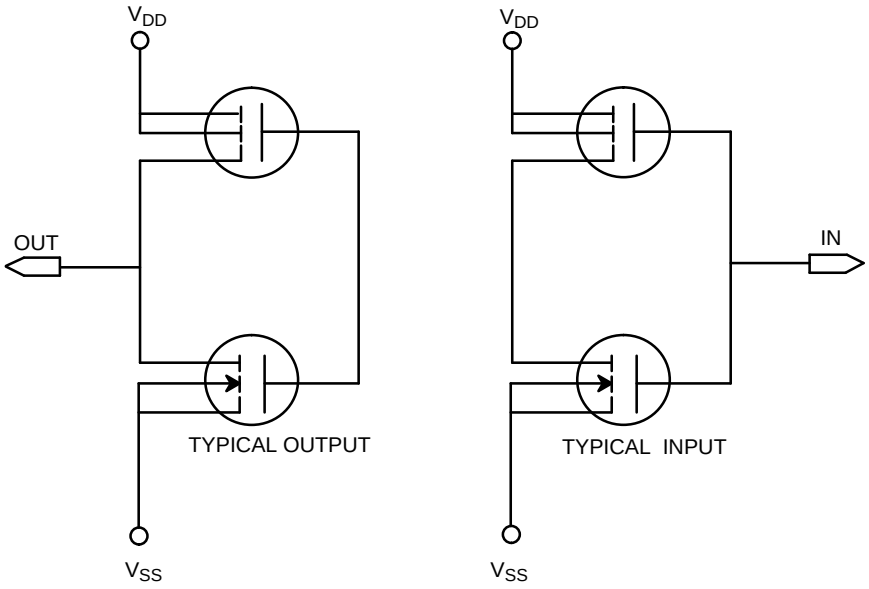


Figure 3. Input/Output Structure

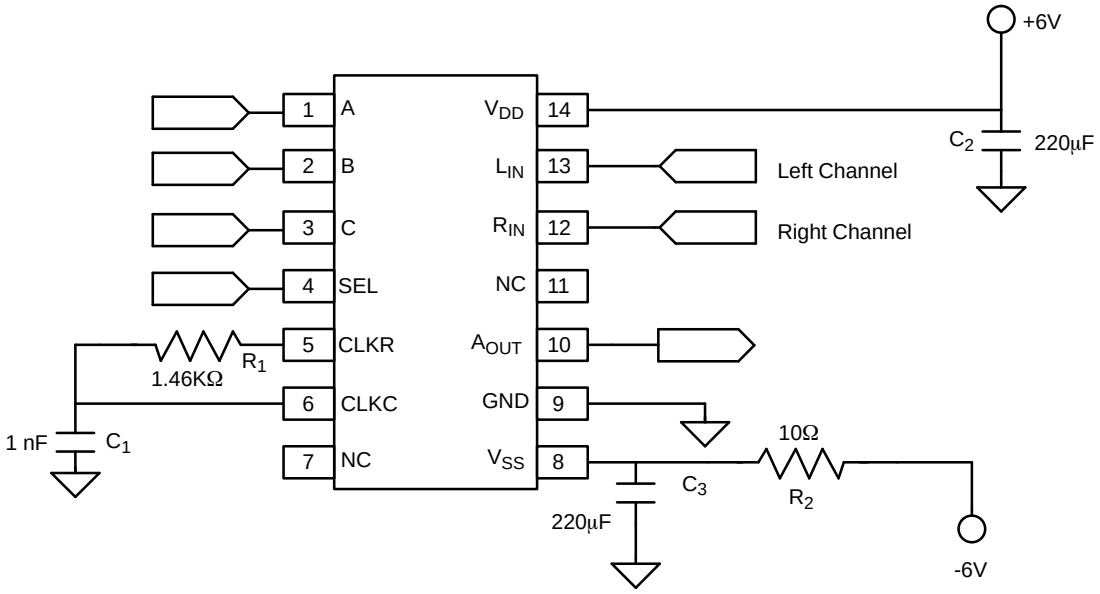
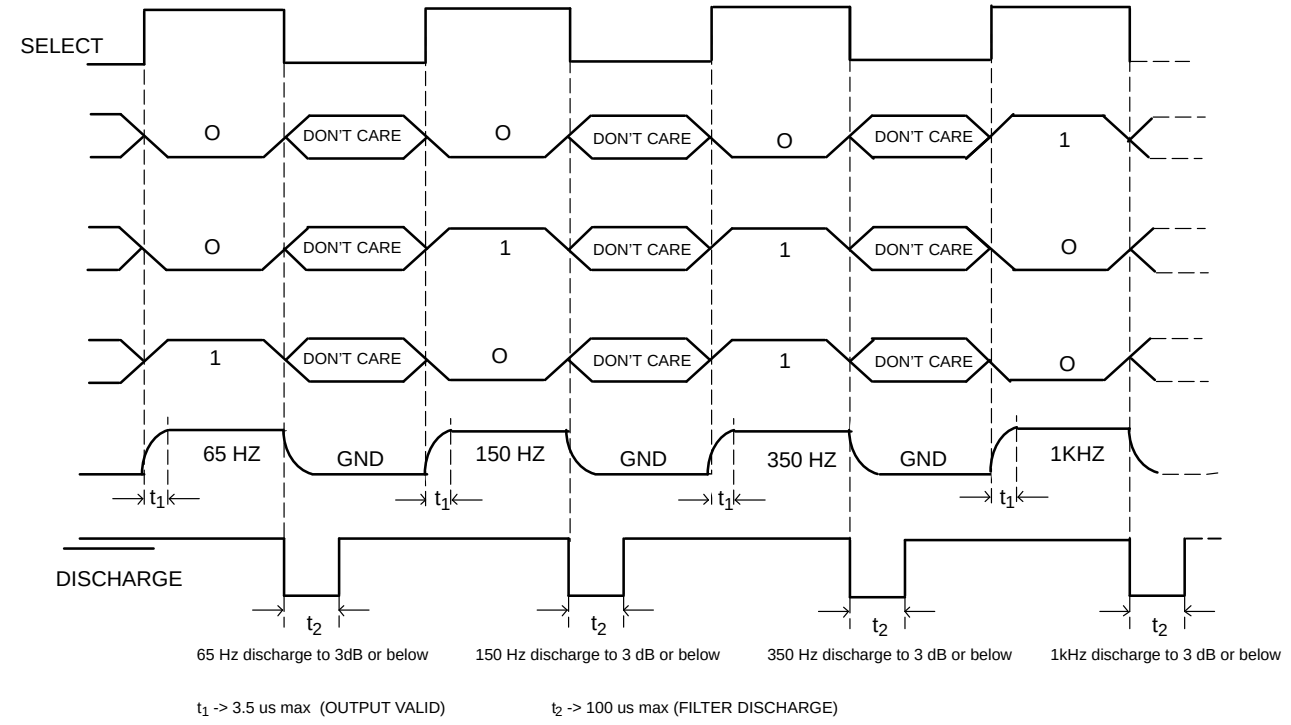


Figure 4. Typical Applications Circuit

SEL	A	B	C	A_{OUT}
0	X	X	X	GND
1	0	0	1	65Hz
1	0	1	0	150Hz
1	0	1	1	350Hz
1	1	0	0	1kHz
1	1	0	1	3kHz
1	1	1	0	6.3kHz
1	1	1	1	12kHz
1	0	0	0	GND

Figure 5. Filter Selection



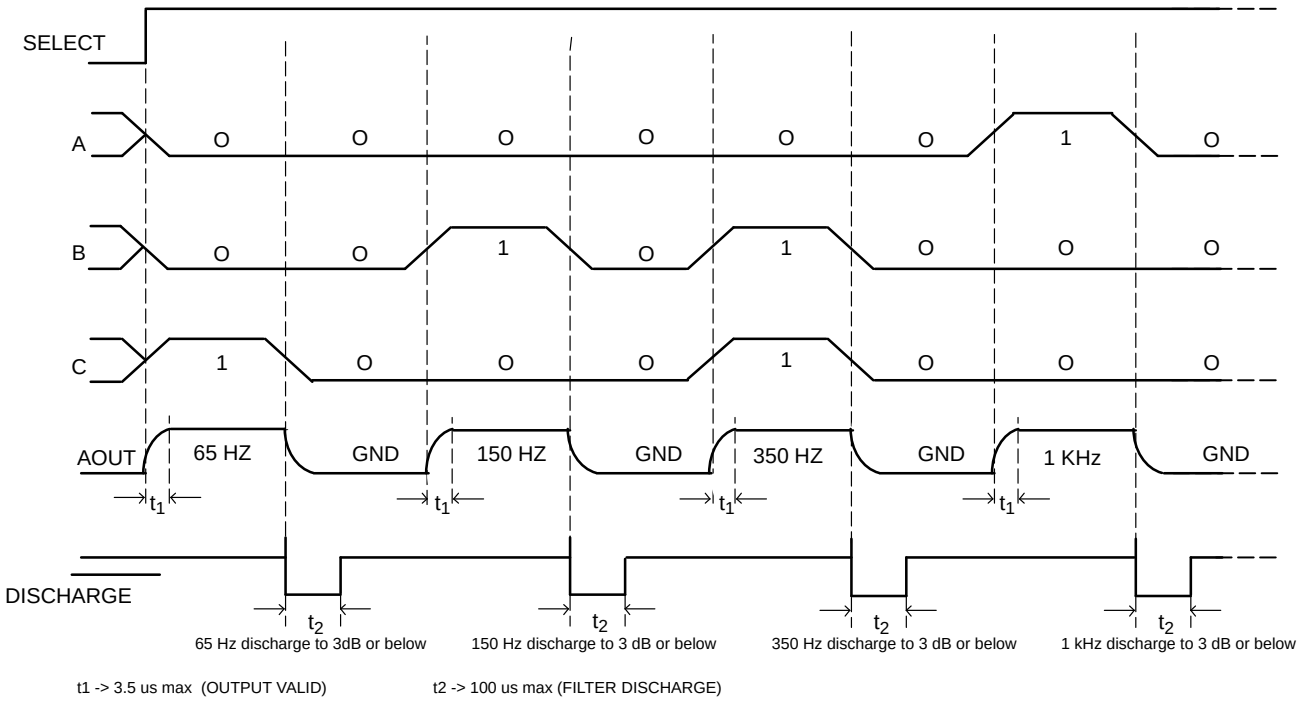


Figure 6. Timing Diagram

Notes

Notes

Notes

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Datasheet September 1996