XR-1085

3.3V
8mm VTR ATF

October 1996-1

FEATURES

- Mixed Analog/Digital Integration to Reduce Discrete Components
- Pilot Signal Generator and Detector on the Same Chip
- On Chip Video Signal GCA Amplifier and Detector
- Accurate Switched-Capacitor Filters
- Low Noise, Low Power Dissipation CMOS

APPLICATIONS

- Automatic Track Finding (ATF) for 8mm Video Tape Recorders

GENERAL DESCRIPTION

The XR-1085 is a mixed analog/digital IC dedicated for use in Automatic Track Finding (ATF) for 8mm Video Tape Recorder applications. The XR-1085 contains three major functional modules: the ATF record pilot signal generator, the ATF pilot signal detector, and the video signal detector. The device is fabricated using EXAR's CMOS process providing low noise, high speed, and low power, and is available in 32 pin PQFP version for use over the -30°C to 80°C temperature range.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-1085CQ	32 Lead Plastic QFP (7 x 7 x 1.4 mm)	-30°C to + 80°C

BLOCK DIAGRAM

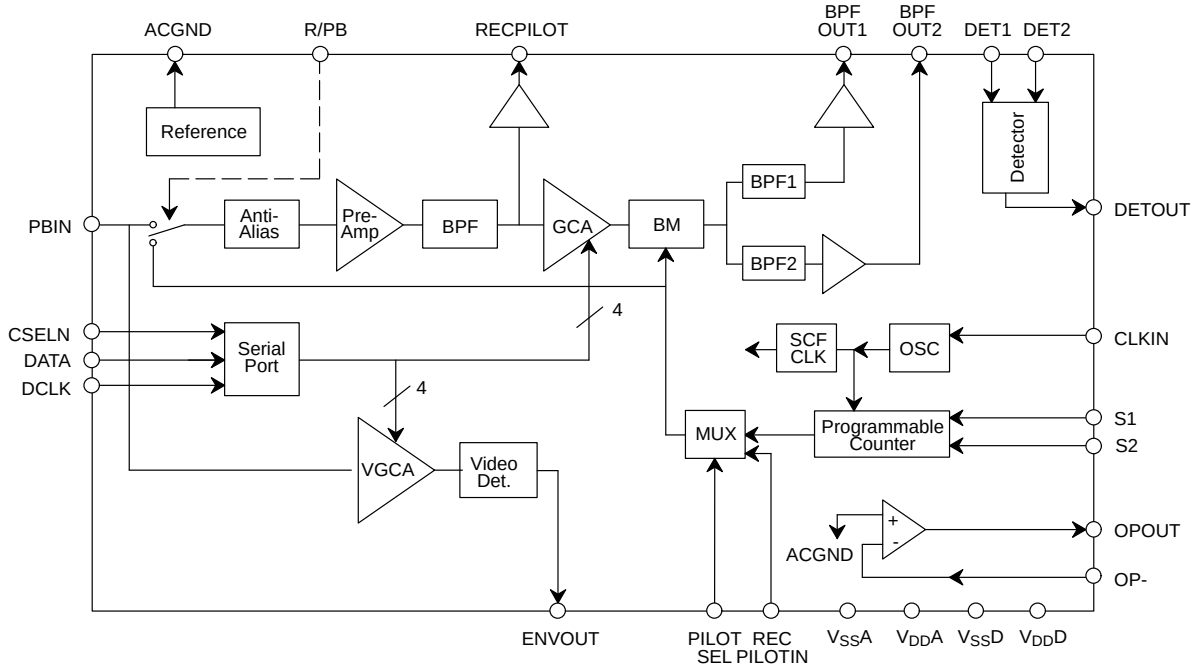
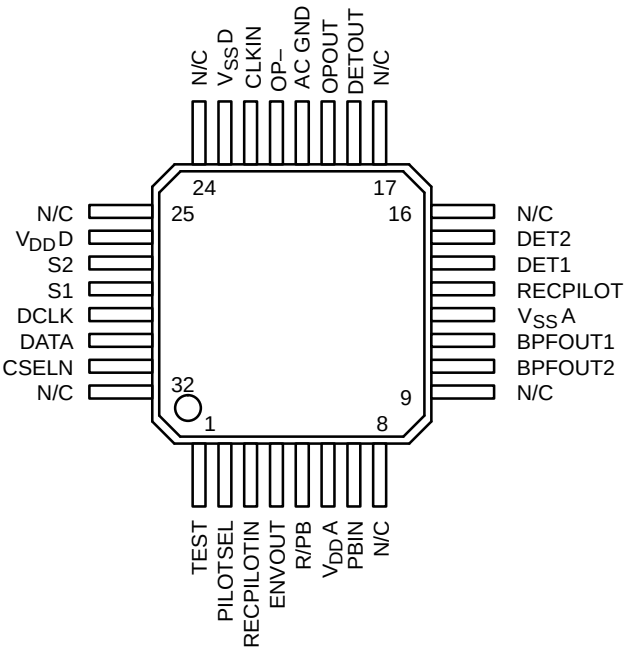


Figure 1. Block Diagram

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

PIN CONFIGURATION



32 Lead PQFP (EIAJ, 7 x 7 x 1.4 mm)

PIN DESCRIPTION

Pin #	Symbol	Description
1	TEST	Factory Use Only; No Connect
2	PILOTSEL	Record Pilot Select
3	RECPILOTIN	External Record Pilot Signal
4	ENVOUT	Video Detected Output
5	R/PB	Record Playback Selection Control
6	V_{DD}A	Analog V_{DD}
7	PBIN	Composite Video Input
8	N/C	No Connect
9	N/C	No Connect
10	BPFOUT2	Output of 16kHz Bandpass Filter
11	BPFOUT1	Output of 47kHz Bandpass Filter
12	V_{SS}A	Analog V_{SS}
13	RECPILOT	Sine Wave Output in Record Mode
14	DET1	Input for 16kHz Detector
15	DET2	Input for 47kHz Detector
16	N/C	No Connect
17	N/C	No Connect

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Description
18	DETOUT	Detector Output Signal
19	OPOUT	Op Amp Output
20	ACGND	AC Grounding
21	OP-	Op Amp Negative Input
22	CLKIN	Clock Input, External
23	$V_{SS}D$	Digital Ground
24	N/C	No Connect
25	N/C	No Connect
26	$V_{DD}D$	Digital V_{DD}
27	S2	F1-F4 Frequency Control
28	S1	F1-F4 Frequency Control
29	DCLK	Clock in Serial Port Mode
30	DATA	Data in Serial Port Mode
31	CSELN	Serial Port Enabled When Low
32	N/C	No Connect

OPERATING CONDITIONS
Supply Voltage (V_{DD}) = 3.0 to 3.6 V, Operating Temp. (T_{OPE}) = –30 to +80°C

ELECTRICAL CHARACTERISTICS
Test Conditions: T_A = 25°C, V_{DD} = 3.3V, CLKIN = 11.9 MHz, 500 mV_{PP}.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Meas. Pin #	Condition	Test Ckt.
$I_{DD}R$	Power Supply Current	2.0	5	9.00	mA	6,26	R/PB = H, Gain = 0	
$I_{DD}PB$		2.0	7	12.0	mA	6,26	R/PB = L, Gain = 0	
V_{IH}	Input Voltage Range, Hi	2.1			V	5,27, 28,29, 30,31		
V_{IL}	Input Voltage Range, Lo			0.8	V	5,27, 28,29, 30,31		
PBIN	Input Pilot Signal Level	10	40	70	mV_{PP}			
	Input Composite Signal Level	150	800	1000	mV_{PP}			
	Recpilot Output DC Level		1.65		V			
RF1	Recpilot Output AC Level	0.7	1.0	1.3	V_{PP}	13	S1 = H, S2 = H, R/PB = H, PILOTSEL=H	*Figure 3.*
RF2		0.7	1.0	1.3	V_{PP}	13	S1 = L, S2 = H, R/PB = H, PILOTSEL=H	*Figure 3.*
RF3		0.7	1.0	1.3	V_{PP}	13	S1 = H, S2 = L, R/PB = H, PILOTSEL=H	*Figure 3.*
RF4		0.7	1.0	1.3	V_{PP}	13	S1 = L, S2 = L, R/PB = H PILOTSEL=H	*Figure 3.*
RFX		0.7	1.0	1.3	V_{PP}	13	R/PB=H, PILOTSEL = L RECPILOTIN=3.3V_{PP}	*Figure 4.*
ΔRF	Recpilot Amplitude Difference	-1.5	0.5	1.5	dB		20 Log RF_{MAX}/RF_{MIN}	
	Recpilot Output Impedence		1		KΩ		Referenced to ACGND	
PBF1	Passband Response		32		dB		PBIN = 10m V_{PP}, 103 kHz R/PB = L, GCA = 0 dB	
PBF2			32		dB		PBIN =10m V_{PP}, 119 kHz R/PB = L, GCA = 0 dB	
PBF3			32		dB		PBIN = 10m V_{PP}, 165 kHz R/PB = L, GCA = 0 dB	
PBF4			32		dB		PBIN = 10m V_{PP}, 149 kHz R/PB = L, GCA = 0 dB	
ΔRF	Passband Ripple		0.5		dB		PBF_{MAX} - PBF_{MIN}	
RPBIN	PBIN Impedance		50		KΩ	7	R/PB=L	
SB10K	Stopband Response		6		dB		PBIN=100m V_{PP}, 10 kHz R/PB=L, GCA=0dB	
SB500K			-30		dB		PBIN=100m V_{PP}, 500 kHz R/PB=L, GCA=0dB	

ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Meas. Pin #	Condition	Test Ckt.
GBP2M	BPF2 Gain (16kHz Filter)	30.5	33	36.5	dB	10	PBIN = 10m V_{PP}, 165kHz, GCA = 0dB, S1 = S2 = L, R/PB = L	*Figure 5.*
GBP1M	BPF1 Gain (46kHz Filter)	30.5	33	36.5	dB	11	PBIN = 10m V_{PP}, 165kHz GCA = 0dB, S1 = L, S2 = H,R/PB = L	*Figure 5.*
ΔGBP	Gain Difference	-2	0	2	dB		Diff. of GBP1M-GBP2M	*Figure 5.*
GBPF21	BPF2 Rejection @ 9 kHz		-23	-20	dB	10	PBIN = 10m V_{PP}, 139kHz GCA = 0dB, S1 = S2 = L, R/PB = L	*Figure 5.*
GBPF22	BPF2 Rejection @28 kHz		-22	-20	dB	10	PBIN = 10m V_{PP}, 120kHz GCA = 0dB, S1 = S2 = L, R/PB = L	*Figure 5.*
GBPF11	BPF1 Rejection @16 kHz		-36	-26	dB	11	PBIN = 10m V_{PP}, 132kHz GCA = 0dB, S1 = S2 = L, R/PB = L	*Figure 5.*
GBPF12	BPF1 Rejection @33 kHz		-25	-20	dB	11	PBIN = 10m V_{PP}, 115kHz GCA = 0dB, S1 = S2 = L, R/PB = L	*Figure 5.*
GBPF13	BPF1 Rejection @60 kHz		-23	-20	dB	11	PBIN = 10m V_{PP}, 88kHz GCA = 0dB, S1 = S2 = L, R/PB = L	*Figure 5.*
GCA1	GCA1 Gain from GCA 0 Gain	0.9	1.1	1.4	dB	10	PBIN = 10m V_{PP}, 149kHz 1dB (BIT 0 = H), S=H, S2=L, R/PB= L	*Figure 6.*
GCA2	GCA2 Gain from GCA 0 Gain	1.8	2.2	2.5	dB	10	PBIN = 10m V_{PP}, 149kHz, 2dB (BIT 1 = H), S=H, S2=L, R/PB= L	*Figure 6.*
GCA4	GCA4 Gain from GCA 0 Gain	3.8	4.3	4.8	dB	10	PBIN = 10m V_{PP}, 149kkz, 4dB (BIT 2 = H), S=H, S2=L, R/PB= L	*Figure 6.*
GCA8	GCA8 Gain from GCA 0 Gain	7.7	8.5	9.4	dB	10	PBIN = 10m V_{PP}, 149kHz, 8dB (BIT 3 = H), S=H, S2=L, R/PB= L	*Figure 6.*
DET0	Detector Output (DC)	1.49	1.65	1.81	V	18,20	DET1 = DET2=ACGND	*Figure 7.*
DETOS0	Detector Offset	-60	0	60	mV	18,20	DET1 = DET2 = ACGND	*Figure 7.*
DETOS1		-60	0	60	mV	18,20	DET1 = DET2 = 0.5V_{PP}, f = 46.2kHz	*Figure 7.*
DET1	Detector Output	-450	-350	-250	mV	18,20	DET1 = 0.5V_{PP}, f = 46.2kHz DET2 = ACGND	*Figure 8.*
DET2		250	350	450	mV	18,20	DET2 = 0.5V_{PP}, f = 46.2kHz DET1 = ACGND	*Figure 8.*
ACGND	AC Ground Output	1.55	1.65	1.75	V	20	V_{DD} = 3.3V, R/PB = L	*Figure 8.*
VOSOP	Opamp Offset	-60	0	60	mV	19	V_{IN} = V_{OUT}	*Figure 9.*
VOHOP	Opamp Output High	2.5			V	19	100µA Source	

ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Meas. Pin #	Condition	Test Ckt.
VOLOP	Opamp Output Low			0.8	V	19	100µA Sink	
BWOP	Opamp Bandwidth		2		MHz			
AOP	Gain		70		dB			
IO	Output Drive		2.0		mA			
R_{OUT}	Output Impedance		50.0		Ω			
VGCA0	VGCA Gain (0dB)	1.5	3.5	5.5	dB	4	PBIN = 1.0V_{PP}, 3.2MHz, VGCA=0dB, R/PB = L	*Figure 10.*
VGCA1	VGCA1 Gain From VGCA0	0.7	1.0	1.7	dB	4	PBIN = 1.0V_{PP}, 3.2MHz, VGCA=1dB (BIT4 = H), R/PB = L	*Figure 10.*
VGCA2	VGCA2 Gain From VGCA0	1.8	2.0	3.0	dB	4	PBIN = 1.0V_{PP}, 3.2MHz, VGCA=2dB (BIT 5 = H), R/PB = L	*Figure 10.*
VGCA4	VGCA4 Gain From VGCA0	3.5	4.0	5.2	dB	4	PBIN = 1.0V_{PP}, 3.2MHz, VGCA=4dB (BIT 6 = H), R/PB = L	*Figure 10.*
VGCA8	VGCA8 Gain From VGCA0	7.0	8.0	10.5	dB	4	PBIN = 0.5V_{PP}, 3.2MHz, VGCA=8dB (BIT 7 = H), R/PB = L	*Figure 10.*
BWVGCA	VGCA Bandwidth		5.0		MHz		3dB Bandwidth	
ENVOUT	ENVOUT DC Level	0.4	0.55	0.7	V	4	PBIN = 0V, VGCA = 0dB, R/PB = L	*Figure 11.*
VCLK	Clock Input	0.3	0.5	V_{DD}	V_{PP}	22	CLOCKIN=11.9 MHz	
DCLK	Duty Cycle	30	50	70	%			

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

V_{DD} . . . . . -0.4 to 7V
V_{IN} . . . . . -0.4 to 7V
VO . . . . . -0.4 to 7V

Storage Temperature . . . . . -40 to +125°C
Power Dissipation (Package Limitation) 0.5W

SYSTEM DESCRIPTION

The XR-1085 is designed to reduce the part count for implementing ATF functions in 8mm VTR's. The XR-1085 contains an ATF record pilot signal generator, an ATF pilot signal detector, and a video signal detector.

The record pilot signal generator consists of an oscillator, a programmable frequency divider and a sine wave generator circuit. The oscillator generates the master clock signal for the entire chip. The clock frequency is 11.9 MHZ (NTSC). Two digital control lines (S1,S2) program the internal frequency divider chain to produce one of the four possible pilot signals (4f control). The pilot signal can also be fed in externally through the REC PILOTIN pin. PILOTSEL pin controls a multiplexer to determine internal vs. external pilot signal generation. The selected pilot frequency is filtered by a band-pass filter to produce the sine wave output pilot signal.

The pilot signal detector consists of a pre-amplifier, band-pass filter, gain control amplifier (GCA), balanced modulator, reference pilot filters, tracking signal detectors, and a tracking error amplifier. The input signal is amplified by the pre-amplifier first, it has a gain of 20dB. Then the band-pass filter passes the four different pilot frequencies and adds an extra 10dB of gain. It rejects video and chroma signals above 170kHz. After the larger video and chroma signals have been removed, the pilot signal is amplified by the GCA for improved signal to noise ratio in the balanced modulator. The gain of the GCA is controlled by a 4-bit digital word from the serial port. The balanced modulator mixes the incoming pilot signals with the reference clock selected by the digital inputs (S1, S2) to produce two tones, one at approximately 16 kHz, and another at approximately 46 kHz. These signals are then filtered by the reference pilot filters to remove the unwanted balanced modulator output products. The reference pilot signals are then converted into a DC level through the peak detectors. The detector outputs are compared and the error signal is amplified before being brought off the chip. The error signal is used to determine the tracking errors in the system.

The video signal detector consists of a video gain control amplifier (VGCA) and a video signal peak detector. The input video signal is amplified by the VGCA, and its gain is selected by a 4-bit digital word from the serial port. Then the envelope of the video signal is detected by a video detector.

DIGITAL CONTROL INPUTS

S2	S1	f	F1-F4 Frequency (NTSC)	f0/N
0	0	f4	148689 Hz	40
0	1	f3	165210 Hz	36
1	0	f2	118951 Hz	50
1	1	f1	102544 Hz	58

Table 1. Pilot Frequency Control

OTHER CONTROL SIGNALS

R/PB	Operation Mode
0	Playback
1	Record

Table 2.

PILOTSEL	Pilot Signal
0	External (RECPILOTIN)
1	Internal (F1-F4)

Table 3.

SERIAL PORT CONTROL SIGNALS

$B_3B_2B_1B_0$	GAIN(dB)	$B_3B_2B_1B_0$	GAIN(dB)	$B_3B_2B_1B_0$	GAIN(dB)	$B_3B_2B_1B_0$	GAIN(dB)
0 0 0 0	0	0 1 0 0	4.27	1 0 0 0	8.53	1 1 0 0	12.8
0 0 0 1	1.07	0 1 0 1	5.33	1 0 0 1	9.60	1 1 0 1	13.9
0 0 1 0	2.13	0 1 1 0	6.40	1 0 1 0	10.7	1 1 1 0	14.9
0 0 1 1	3.20	0 1 1 1	7.47	1 0 1 1	11.7	1 1 1 1	16.0

Table 4. GCA Control Signal

$B_7B_6B_5B_4$	GAIN(dB)	$B_7B_6B_5B_4$	GAIN(dB)	$B_7B_6B_5B_4$	GAIN(dB)	$B_7B_6B_5B_4$	GAIN(dB)
0 0 0 0	0	0 1 0 0	4.0	1 0 0 0	8.0	1 1 0 0	12.0
0 0 0 1	1.0	0 1 0 1	5.0	1 0 0 1	9.0	1 1 0 1	13.0
0 0 1 0	2.0	0 1 1 0	6.0	1 0 1 0	10.0	1 1 1 0	14.0
0 0 1 1	3.0	0 1 1 1	7.0	1 0 1 1	11.0	1 1 1 1	15.0

Table 5. VGCA Control Signal

B9	B8	Function
0	0	Normal
0	1	Test
1	0	Test
1	1	Test

Note
In all applications, both Bit 8 and Bit 9 should be set to 0.

Table 6.

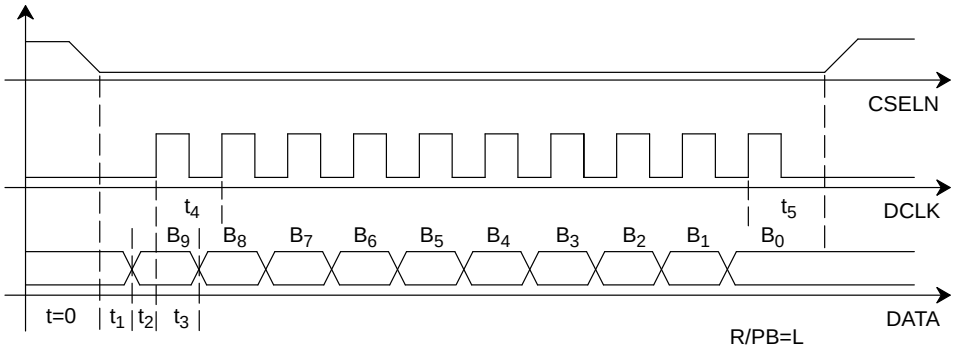


Figure 2. Serial Port Timing Diagram

Name	Time	Unit
t_1	500	ns
t_2	200	ns
t_3	200	ns
t_4	1000	ns
t_5	500	ns

Table 7. Serial Port Minimum Timing Requirement

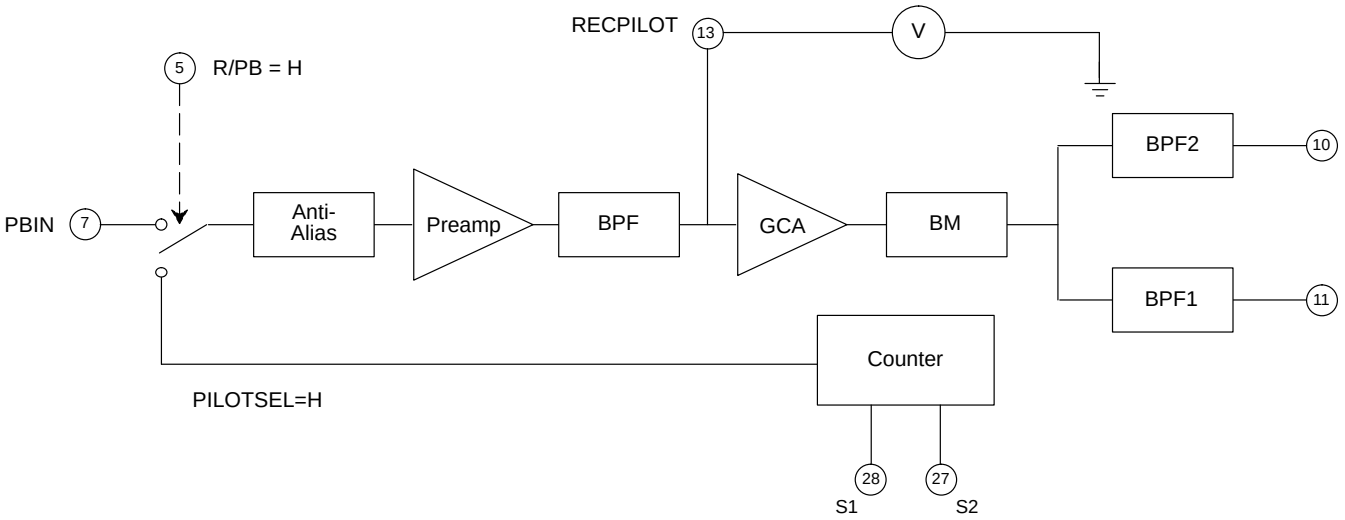


Figure 3. Tests: RF_1, RF_2, RF_3, RF_4

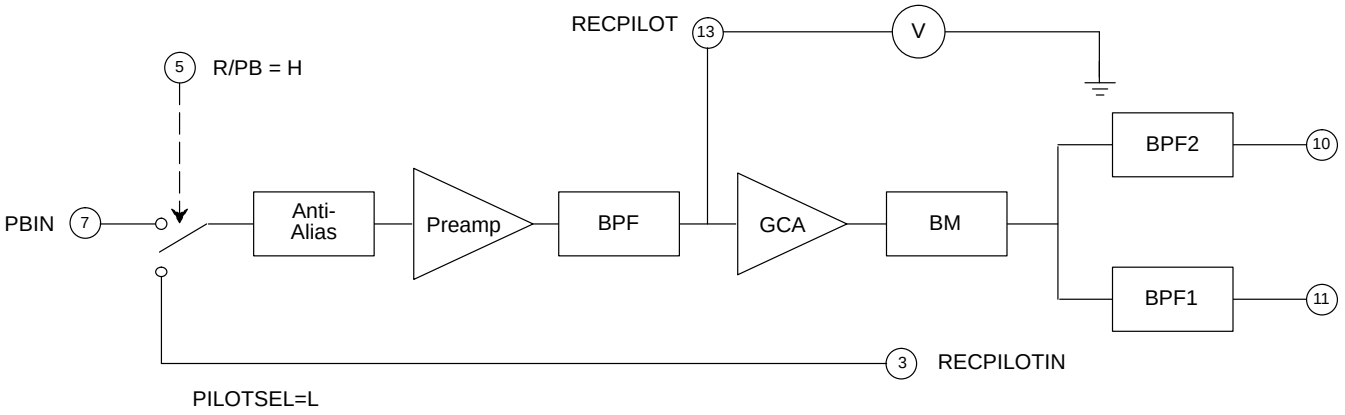


Figure 4. Test: RFX

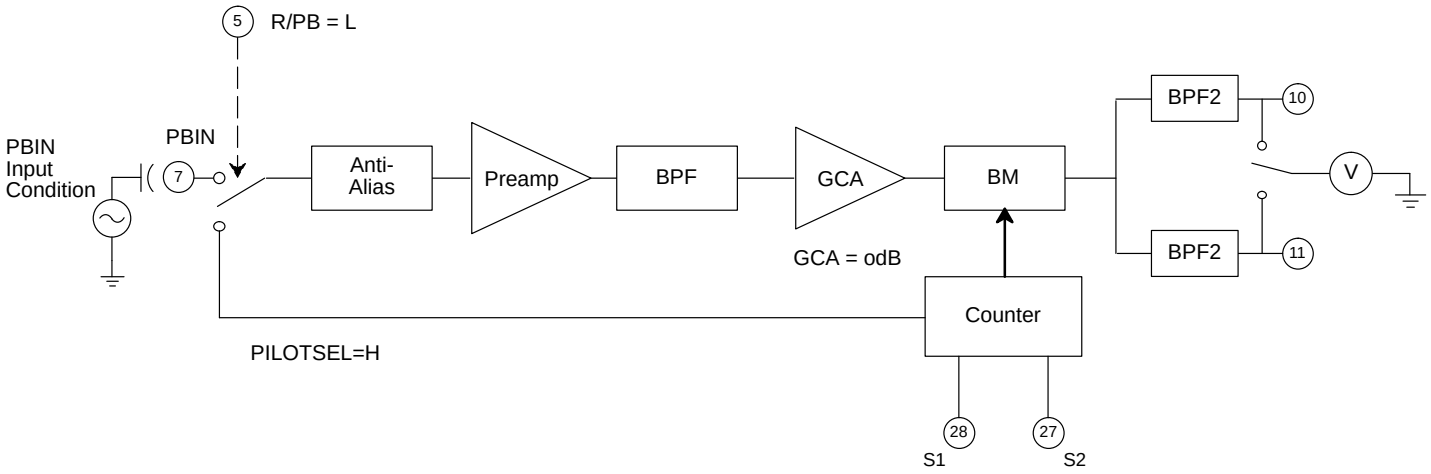
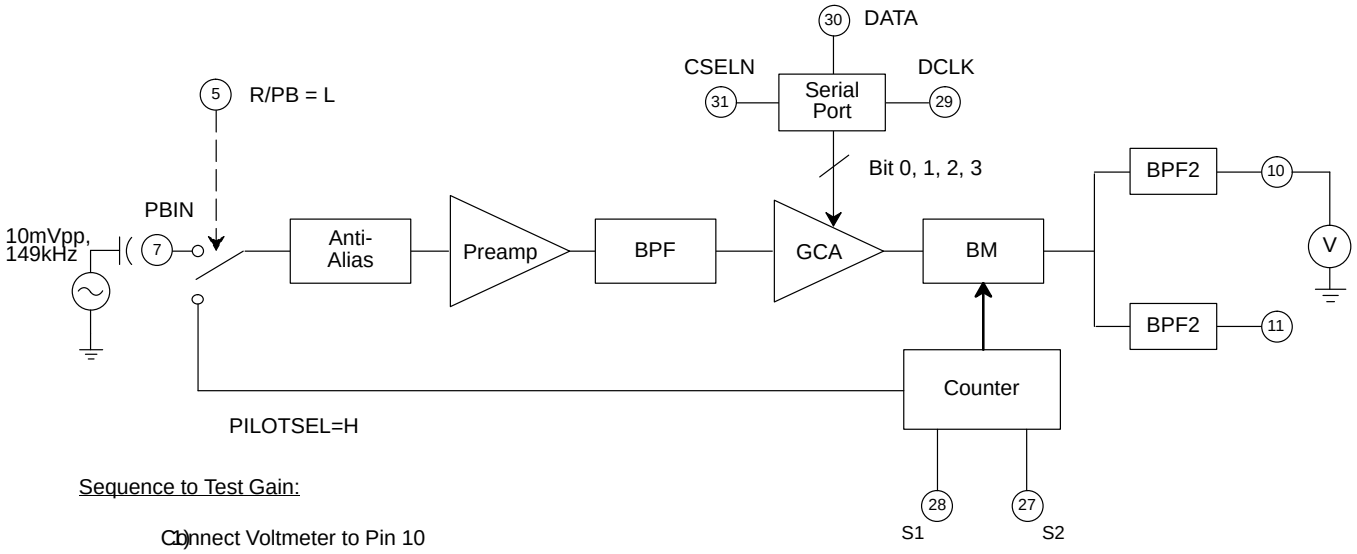


Figure 5. Tests: PBF_1, PBF_2, PBF_3, PBF_4, SB10K, SB500K

Symbol	PBIN Input Condition	S1	S2	Measurement Pin
GBP2M	10mVpp, 165kHz	L	L	10
GBP1M	10mVpp, 165kHz	L	H	11
GBP21	10mVpp, 139kHz	L	L	10
GBP22	10mVpp, 120kHz	L	L	10
GBP11	10mVpp, 132kHz	L	L	11
GBP12	10mVpp, 115kHz	L	L	11
GBP13	10mVpp, 88kHz	L	L	11

Table 8.



Sequence to Test Gain:

1) Connect Voltmeter to Pin 10

2) Input to Pin 7 = 10mVpp @ 149kHz
   S1 = H and S2 = L (to get 16kHz signal)

3) Follow Timing Diagram
   CSEL Low --> Set Data --> Then Clock --> CSEL High

4) GCA # Gain = 20 log $(\frac{V_{OUT}}{V_{IN}})$ - GCA(0)

5) GCA(0) = 20 log $(\frac{V_{OUT}}{V_{IN}})$ with Bits 0,1,2,3 = Low

Figure 6. Test: GCA # Gain

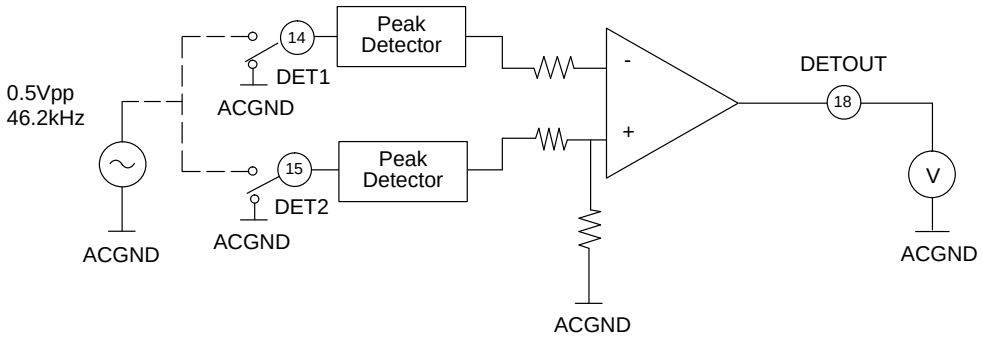


Figure 7. Tests: DETOSØ (As Shown)
DETOS1 (Connect Dashed CKT and MEAS)

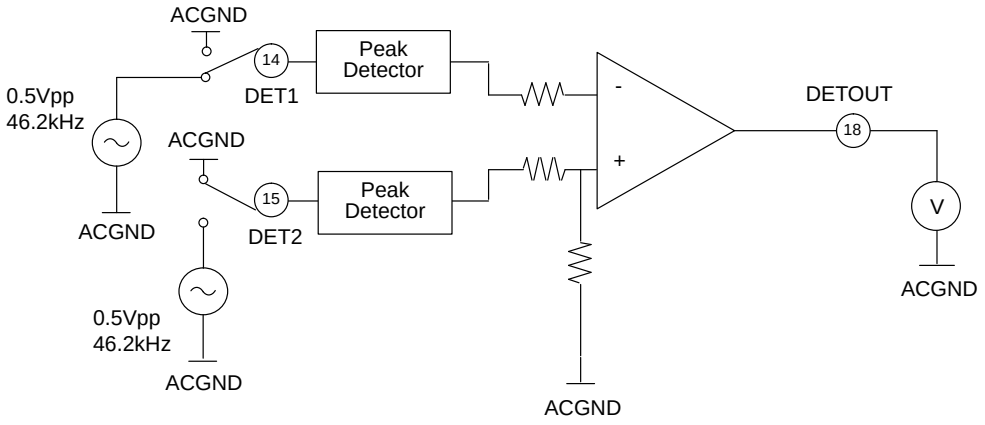


Figure 8. Test: DET1 (As Shown)
DET2 (Switches Turned The Other Way)

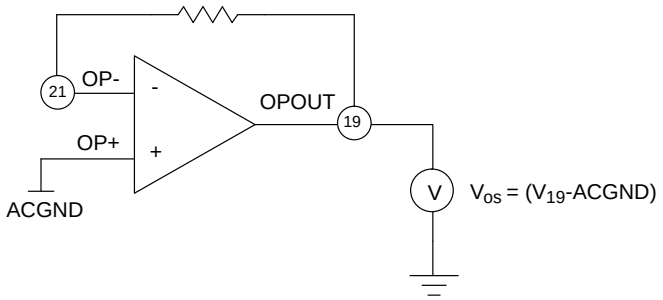
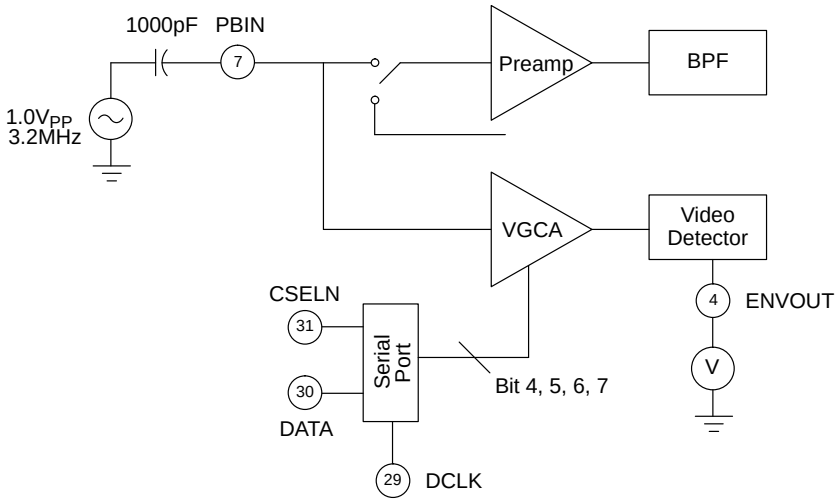


Figure 9. Test: VOSOP



*Follow Timing Diagram
CSEL Low → Set Data → Then Clock → CSEL High

Figure 10. Test: VGCA GAIN #

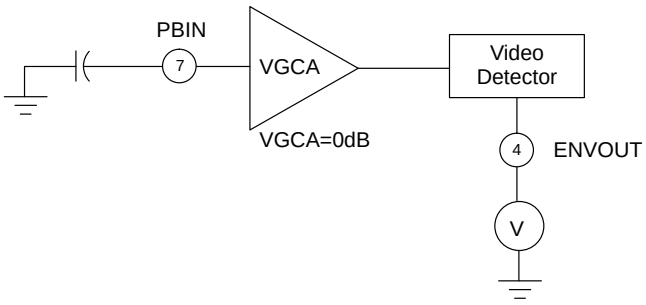
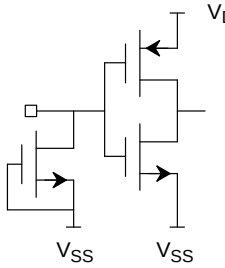
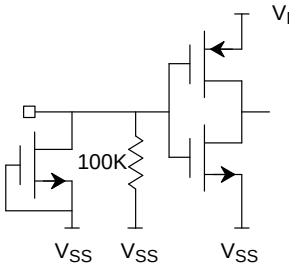
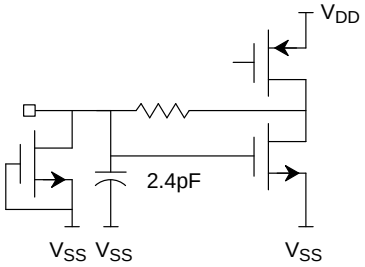
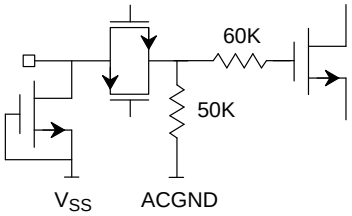
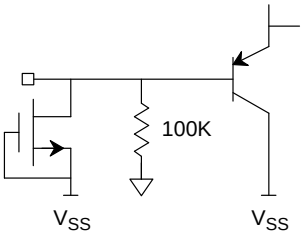
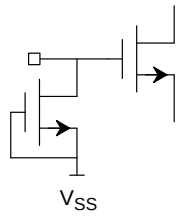
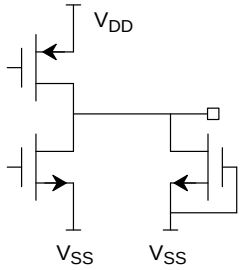
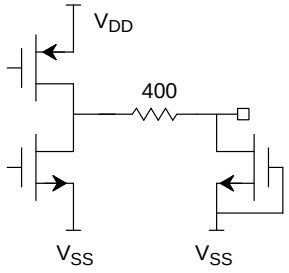
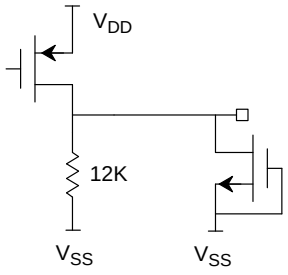


Figure 11. Test: ENVOUT

PIN #	SYMBOL	I/O	EQUIVALENT CIRCUIT	DESCRIPTION
5 28 27 29 30 3 2	R/PB S1 S2 DCLK DATA RECPILOTIN PILOTSEL	I		Record Playback Select Control F1-F4 Frequency Control F1-F4 Frequency Control Clock in Serial Port Data in Serial Port External Record Pilot Signal Record Pilot Select
31	CSELN	I		Serial Port Enable
22	CLKIN	I		Clock Input
7	PBIN	I		Composite Video Input
15 14	DET2 DET1	I		Input for 47 kHz Detector Input for 16 kHz Detector

PIN #	SYMBOL	I/O	EQUIVALENT CIRCUIT	DESCRIPTION
21	OP-	I		Op Amp Negative Input
10 11 18 19 20	BPFOUT2 BPFOUT1 DETOUT OPOUT ACGND	O		Output of 16 kHz Bandpass Filter Output of 47 kHz Bandpass Filter Detector Output Op Amp Output AC Ground Output
13	RECPILOT	O		Sine Wave Output in Record Mode
4	ENVOUT	O		Video Detected Output

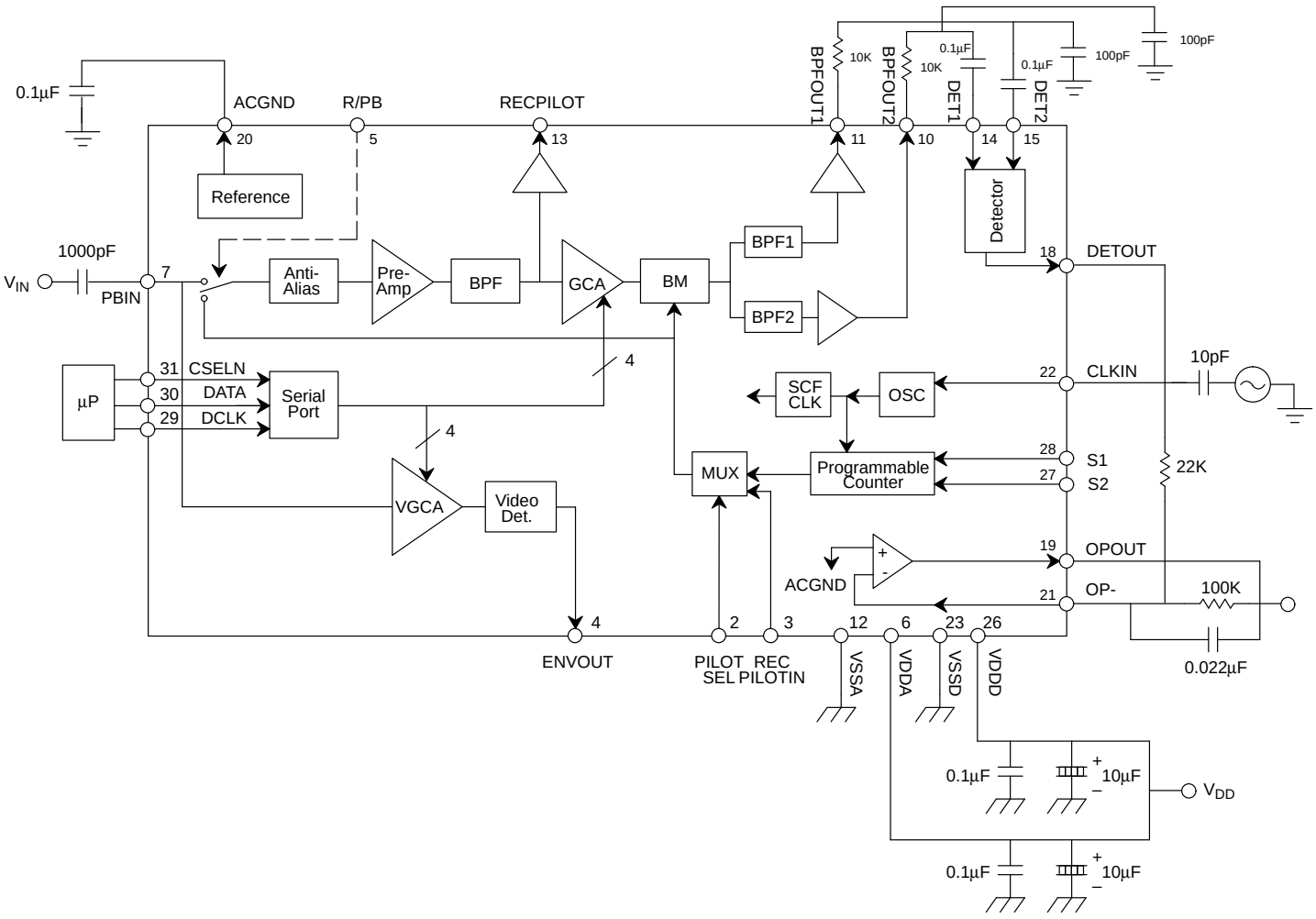
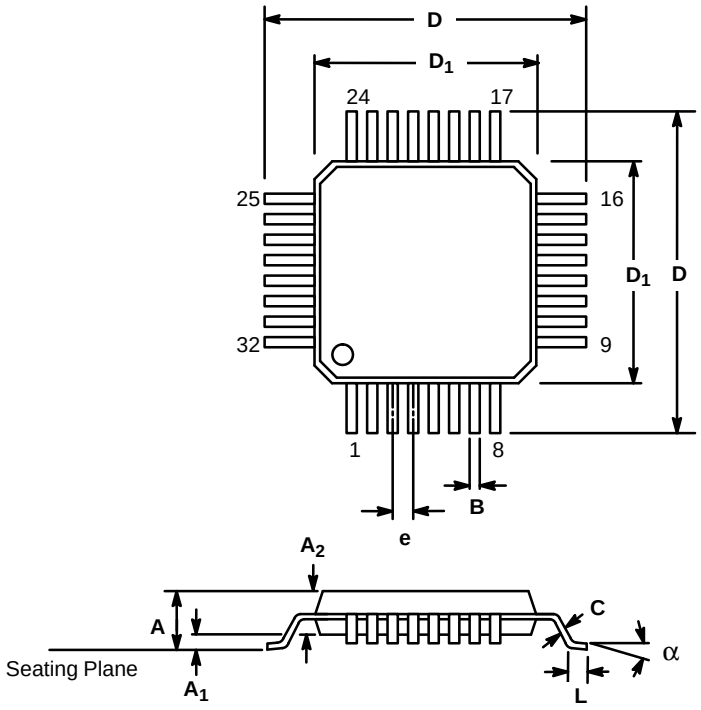


Figure 12. XR–1085CQ Application Diagram

32 LEAD PLASTIC QUAD FLAT PACK
(7 x 7 x 1.4 mm QFP)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.012	0.018	0.30	0.45
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.0315 BSC		0.80 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

Notes

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Datasheet October 1996