FEATURES

- Mixed Analog/Digital Integration to Reduce Discrete Components
- Pilot Signal Generator and Detector on the Same Chip
- On Chip Video Signal GCA Amplifier and Detectors
- Accurate Switched-Capacitor Filters
- Low Noise, Low Power Dissipation CMOS

GENERAL DESCRIPTION

The XR-10823 is a mixed analog/digital IC dedicated for use in Automatic Track Finding (ATF) for 8mm Video Tape Recorder applications. The XR-10823 contains three major functional modules: the ATF record pilot signal generator, the ATF pilot signal detector, and the video signal detector. The device is fabricated using EXAR's CMOS process providing low noise, high speed, and low power, and is available in 32 pin QFP version for use over the -30°C to 75°C temperature range.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-10823CQ	32 Lead Plastic QFP (7 x 7 x 1.4 mm)	-30°C to +75°C

BLOCK DIAGRAM

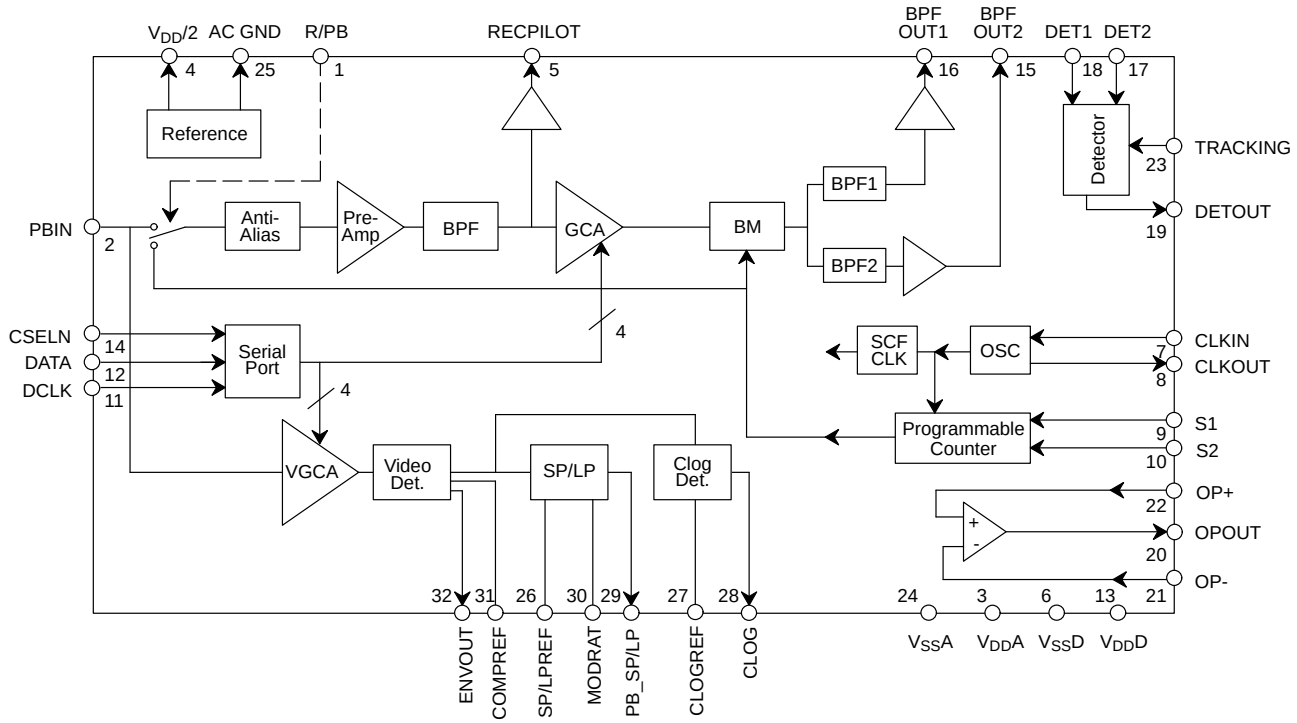
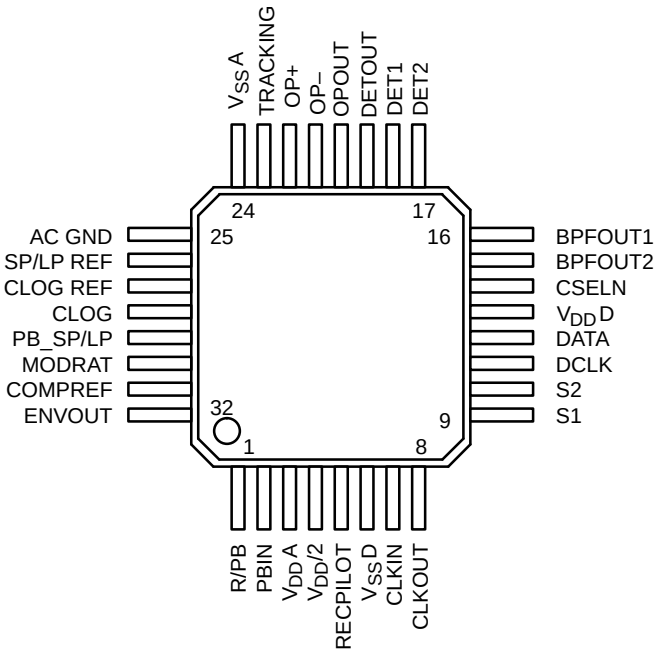


Figure 1. Block Diagram

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

PIN CONFIGURATION



32 Lead PQFP (EIAJ, 7 x 7 x 1.4 mm)

PIN DESCRIPTION

Pin #	Symbol	Description
1	R/PB	Record playback selection control
2	PBIN	Composite video input
3	$V_{DD}A$	Analog V_{DD}
4	$V_{DD}/2$	Analog reference filter point
5	RECPILOT	Sinewave output in record mode
6	$V_{SS}D$	Digital ground
7	CLKIN	Clock input, crystal or external
8	CLKOUT	Clock output to crystal
9	S1	F1-F4 frequency control
10	S2	F1-F4 frequency control
11	DCLK	Clock in serial port mode
12	DATA	Data in serial port mode
13	$V_{DD}D$	Digital V_{DD}
14	CSELN	Serial port enabled when low
15	BPFOUT2	Output of 16kHz bandpass filter
16	BPFOUT1	Output of 47kHz bandpass filter
17	DET2	Input for 47kHz detector

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Description
18	DET1	Input for 16kHz detector
19	DETOUT	Detector output signal
20	OPOUT	Op amp output
21	OP-	Op amp negative input
22	OP+	Op amp positive input
23	TRACKING	DC reference for detector, 2V to 3V OK
24	$V_{SS}A$	Analog V_{SS}
25	AC GND	AC grounding
26	SP/LP REF	SP/LP trip point reference
27	CLOG REF	Clog trip point reference
28	CLOG	Clog output
29	PB_SP/LP	PB_SP/LP output
30	MODRAT	Modulation ratio control
31	COMPREF	Video DC reference
32	ENVOUT	Video detected output

DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{DD} = 5.0V, XTAL = 11.9 MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit	Meas. Pin #	Condition	Test Ckt.
$I_{DD}R$	Power Supply Current	2.0	5	9.00	mA	3&13	R/PB = H, Gain = 0	
$I_{DD}PB$		2.0	7	12.0	mA	3&13	R/PB = L, Gain = 0	
V_{IH}	Input Voltage Range	3.5			V	1,9,10, 11,12,14		
V_{IL}				1.5	V	1,9,10, 11,12,14		
V_{OH}	Output Voltage Range	4.5			V	28,29		
V_{OL}				0.5	V	28,29		
PBIN	Input Pilot Signal Level	10	40	70	mV_{PP}			
	Input Composite Signal Level	150	800	1000	mV_{PP}			
	Recpilot Output DC Level		2.5		V			
RF1	Recpilot Output AC Level	2.1	2.5	2.9	V_{PP}	5	S1 = H, S2 = H, R/PB = H	*Figure 3.*
RF2		2.1	2.5	2.9	V_{PP}	5	S1 = L, S2 = H, R/PB = H	*Figure 3.*
RF3		2.1	2.5	2.9	V_{PP}	5	S1 = H, S2 = L, R/PB = H	*Figure 3.*
RF4		2.1	2.5	2.9	V_{PP}	5	S1 = L, S2 = L, R/PB = H	*Figure 3.*
ΔRF	Recpilot Amplitude Difference	-1.5	0.5	1.5	dB		20 Log RF_{MAX}/RF_{MIN}	
	Recpilot Output Impedence		1		kΩ		Referenced to AC GND	
PBF1	Passband Response		32		dB		PBIN = 10mVpp, 103 kHz R/PB = L, GCA = 0 dB	
PBF2			32		dB		PBIN =10mVpp, 119 kHz R/PB = L, GCA = 0 dB	
PBF3			32		dB		PBIN = 10mVpp, 165 kHz R/PB = L, GCA = 0 dB	
PBF4			32		dB		PBIN = 10mVpp, 149 kHz R/PB = L, GCA = 0 dB	
ΔRF	Passband Ripple		0.5		dB		PBF_{MAX} - PBF_{MIN}	
RPBIN	PBIN Impedance		50		KΩ	2	R/PB=L	
SB10K	Stopband Response		6		dB		PBIN=100mVpp, 10kHz R/PB=L, GCA=0dB	
SB500K			-30		dB		PBIN=100mVpp, 500kHz R/PB=L, G CA=0dB	
GBP2M	BPF2 Gain (16kHz Filter)	30.5	33	36.5	dB	15	PBIN = 10mVpp, 165kHz, GCA = 0dB, S1 = S2 = L, R/PB = L	*Figure 4.*
GBP1M	BPF1 Gain (46kHz Filter)	30.5	33	36.5	dB	16	PBIN = 10mVpp, 165kHz GCA = 0dB, S1 = L, S2 = H, R/PB = L	*Figure 4.*
ΔGBP	Gain Difference	-2	0	2	dB		Diff. of GBP1M-GBP2M	

DC ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Meas. Pin #	Condition	Test Ckt.
GBPF21	BPF2 Rejection @ 9kHz		-23	-20	dB	15	PBIN = 10mVpp, 139kHz GCA = 0dB, S1 = S2 = L, R/PB = L	*Figure 4.*
GBPF22	BPF2 Rejection @28kHz		-22	-20	dB	15	PBIN = 10mVpp, 120kHz GCA = 0dB, S1 = S2 = L, R/PB = L	*Figure 4.*
GBPF11	BPF1 Rejection @16kHz		-36	-26	dB	16	PBIN = 10mVpp, 132kHz GCA = 0dB, S1 = S2 = L, R/PB = L	*Figure 4.*
GBPF12	BPF1 Rejection @33kHz		-25	-20	dB	16	PBIN = 10mVpp, 115kHz GCA = 0dB, S1 = S2 = L, R/PB = L	*Figure 4.*
GBPF13	BPF1 Rejection @60kHz		-23	-20	dB	16	PBIN = 10mVpp, 88kHz GCA = 0dB, S1 = S2 = L, R/PB = L	*Figure 4.*
GCA1	GCA1 Gain from GCA 0 Gain	0.9	1.1	1.4	dB	15	PBIN = 10mVpp, 149kHz, 1dB (BIT 0 = H), S=H, S2=L, R/PB= L	*Figure 5.*
GCA2	GCA2 Gain from GCA 0 Gain	1.8	2.2	2.5	dB	15	PBIN = 10mVpp, 149kHz, 2dB (BIT 1 = H), S=H, S2=L, R/PB= L	*Figure 5.*
GCA4	GCA4 Gain from GCA 0 Gain	3.8	4.3	4.8	dB	15	PBIN = 10mVpp, 149kHz, 4dB (BIT 2 = H), S=H, S2=L, R/PB= L	*Figure 5.*
GCA8	GCA8 Gain from GCA 0 Gain	7.7	8.5	9.4	dB	15	PBIN = 10mVpp, 149kHz, 8dB (BIT 3 = H), S=H, S2=L, R/PB= L	*Figure 5.*
DETOS0	Detector Offset	-60	0	60	mV	19, 25	Det1 = Det2 = ACGND	*Figure 6.*
DETOS1		-60	0	60	mV	19, 25	Det1 = Det2 = 0.5Vpp, f = 46.2kHz	*Figure 6.*
DET1	Detector Output	-450	-350	-250	mV	19, 25	Det1 = 0.5Vpp, f = 46.2kHz, Det2 = ACGND	*Figure 7.*
DET2		250	350	450	mV	19, 25	Det2 = 0.5Vpp, f = 46.2kHz, Det1 = ACGND	*Figure 7.*
V_{DD}HLF	Analog Reference Filter Point	2.4	2.5	2.6	V	4	V_{DD} = 5.0V	
ACGND	AC Ground Output	2.4	2.5	2.6	V	25	V_{DD} = 5.0V, R/PB= L	
VOSOP	Op Amp Offset	-60	0	60	mV	20	V_{IN} = V_{OUT}	*Figure 8.*
VOHOP	Op Amp Output High	4.0			V	20	100µA Source	
VOLOP	Op Amp Output Low			1.0	V	20	100µA Sink	
BWOP	Op Amp Bandwidth		2		MHz			
AOP	Gain		70		dB			
IO	Output Drive		2.0		mA			
R_{OUT}	Output Impedance		50.0		Ω			

DC ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Meas. Pin #	Condition	Test Ckt.
VGCA0	VGCA Gain (0dB)	1.5	3.5	5.5	dB	32	PBIN = 1.0Vpp, 3.2MHz, VGCA=0dB, R/PB = L	*Figure 9.*
VGCA1	VGCA1 Gain From VGCA0	0.7	1.0	1.7	dB	32	PBIN = 1.0Vpp, 3.2MHz, VGCA=1dB (BIT4=H), R/PB = L	*Figure 9.*
VGCA2	VGCA2 Gain From VGCA0	1.8	2.0	3.0	dB	32	PBIN = 1.0Vpp, 3.2MHz, VGCA=2dB (BIT 5 = H), R/PB = L	*Figure 9.*
VGCA4	VGCA4 Gain From VGCA0	3.5	4.0	5.2	dB	32	PBIN = 1.0Vpp,3.2MHz, VGCA=4dB (BIT 6 = H), R/PB = L	*Figure 9.*
VGCA8	VGCA8 Gain From VGCA0	7.0	8.0	10.5	dB	32	PBIN = 1.0Vpp,3.2MHz, VGCA=8dB (BIT 7 = H), R/PB = L	*Figure 9.*
BWVGCA	VGCA Bandwidth		5.0		MHz		3dB Bandwidth	
ENVOUT	ENVOUT DC Level	0.4	0.7	1.0	V	32	PBIN = 0V, VGCA = 0dB R/PB=L	*Figure 10.*
COM-PREF	COMPREF DC Level	0.4	0.7	1.0	V	31	PBIN=0V, VGCA=0dB, R/PB=L	*Figure 10.*
ENVOS	ENVOUT Offset (ENVOUT – COMPREF)	-200	0	200	mV		PBIN = 0V, VGCA = 0dB, R/PB = L	

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

V_{DD} . . . . . -0.4 to 7V
V_{IN} . . . . . -0.4 to 7V
VO . . . . . -0.4 to 7V
Storage Temperature . . . . . -40°C to +125°C
Power Dissipation (Package Limitation) 0.5W

SYSTEM DESCRIPTION

The XR-10823 is designed to reduce the part count for implementing ATF functions in 8mm VTR's. The XR-10823 contains an ATF record pilot signal generator, an ATF pilot signal detector, and a video signal detector.

The record pilot signal generator consists of an oscillator, a programmable frequency divider and a sine wave generator circuit. The oscillator generates the master clock signal for the entire chip. The clock frequency is 11.9 MHZ (NTSC). Two digital control lines (S1, S2) program the internal frequency divider chain to produce one of the four possible pilot signals (4f control). The selected pilot frequency is filtered by a band-pass filter to produce the sine wave output pilot signal.

The pilot signal detector consists of a pre-amplifier, band-pass filter, gain control amplifier (GCA), balanced modulator, reference pilot filters, tracking signal detectors, and a tracking error amplifier. The input signal is amplified by the pre-amplifier first, it has a gain of 20dB. Then the band-pass filter passes the four different pilot frequencies and adds an extra 10dB of gain. It rejects video and chroma signals above 170kHz. After the larger video and chroma signals have been removed, the pilot signal is amplified by the GCA for improved signal to noise ratio in the balanced modulator. The gain of the GCA is controlled by a 4-bit digital word from the serial port.

The balanced modulator mixes the incoming pilot signals with the reference clock selected by the digital inputs (S1, S2) to produce two tones, one at approximately 16 kHz, and another at approximately 46 kHz. These signals are then filtered by the reference pilot filters to remove the unwanted balanced modulator output products. The reference pilot signals are then converted into a DC level through the peak detectors. The detector outputs are compared and the error signal is amplified before being brought off the chip. The DC reference is determined by the tracking input. The error signal is used to determine the tracking errors in the system.

The video signal detector consists of a video gain control amplifier (VGCA), a video signal peak detector, SPLP and CLOG detector.The input video signal is amplified by the VGCA, and its gain is selected by a 4-bit digital word from the serial port. Then the envelope of the video signal is detected by a video detector, which is followed by the detection of the SP/LP and CLOG status.

DIGITAL CONTROL INPUTS

S2	S1	f	F1-F4 Frequency (NTSC)	f0/N
0	0	f_4	148689 Hz	40
0	1	f_3	165210 Hz	36
1	0	f_2	118951 Hz	50
1	1	f_1	102544 Hz	58

Table 1. Pilot Frequency Control

OTHER CONTROL SIGNALS

R/PB	Operation Mode
0	Playback
1	Record

Table 2.

SERIAL PORT CONTROL SIGNALS

B_3	B_2	B_1	B_0	Gain (dB)	B_3	B_2	B_1	B_0	Gain (dB)	B_3	B_2	B_1	B_0	Gain (dB)	B_3	B_2	B_1	B_0	Gain (dB)
0	0	0	0	0	0	1	0	0	4.27	1	0	0	0	8.53	1	1	0	0	12.8
0	0	0	1	1.07	0	1	0	1	5.33	1	0	0	1	9.60	1	1	0	1	13.9
0	0	1	0	2.13	0	1	1	0	6.40	1	0	1	0	10.7	1	1	1	0	14.9
0	0	1	1	3.20	0	1	1	1	7.47	1	0	1	1	11.7	1	1	1	1	16.0

Table 3. GCA Control Signal

B_7	B_6	B_5	B_4	Gain (dB)	B_7	B_6	B_5	B_4	Gain (dB)	B_7	B_6	B_5	B_4	Gain (dB)	B_7	B_6	B_5	B_4	Gain (dB)
0	0	0	0	0	0	1	0	0	4.0	1	0	0	0	8.0	1	1	0	0	12.0
0	0	0	1	1.0	0	1	0	1	5.0	1	0	0	1	9.0	1	1	0	1	13.0
0	0	1	0	2.0	0	1	1	0	6.0	1	0	1	0	10.0	1	1	1	0	14.0
0	0	1	1	3.0	0	1	1	1	7.0	1	0	1	1	11.0	1	1	1	1	15.0

Table 4. VGCA Control Signal

B9	B8	Function
0	0	Normal
0	1	Test
1	0	Test
1	1	Test

Note
In all applications, both Bit 8 and Bit 9 should be set to 0.
Test Pin not available in 32 QFP Package.

Table 5.

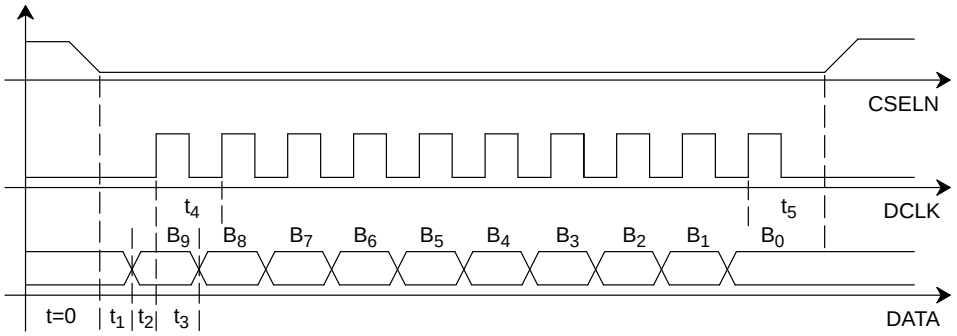


Figure 2. ATF Serial Port Timing Diagram

Name	Time	Unit
t_1	500	ns
t_2	200	ns
t_3	200	ns
t_4	1000	ns
t_5	500	ns

Table 6. Serial Port Minimum Timing Requirement

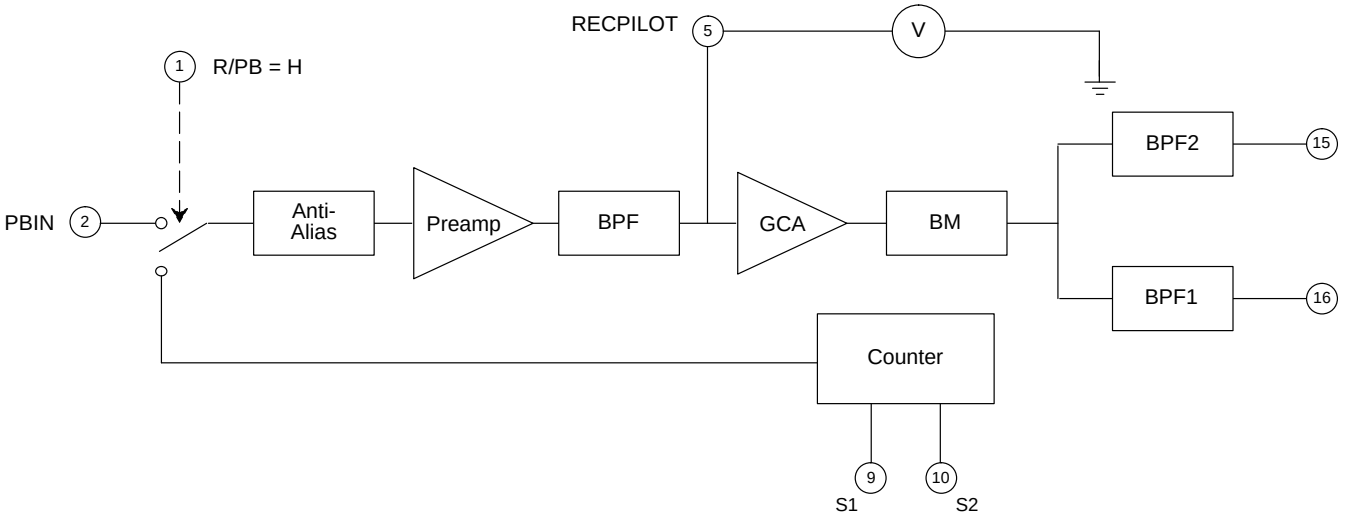


Figure 3. Tests: RF_1, RF_2, RF_3, RF_4

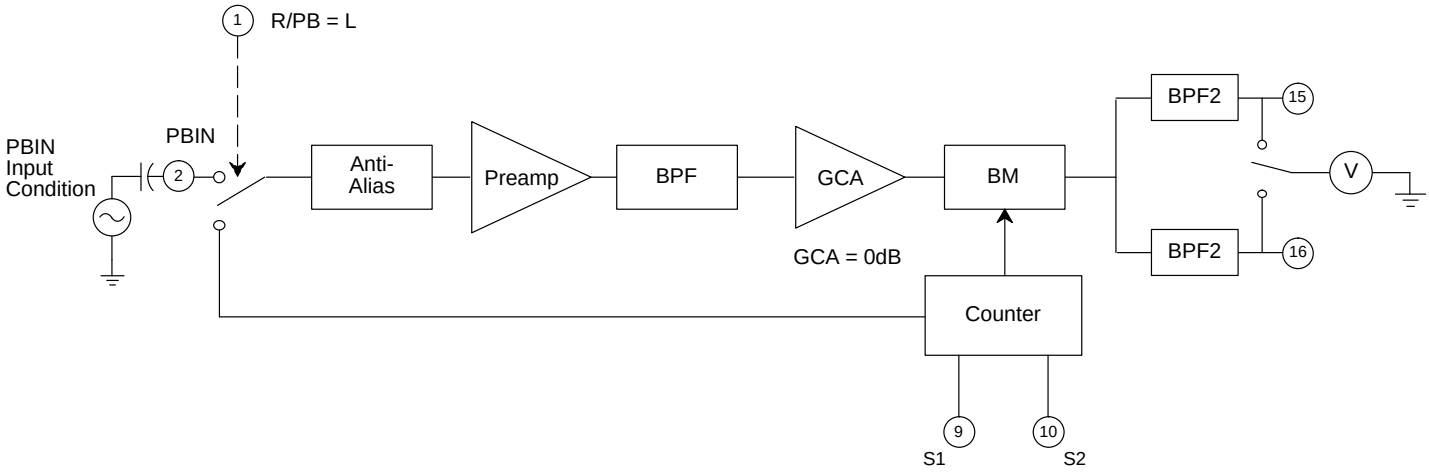
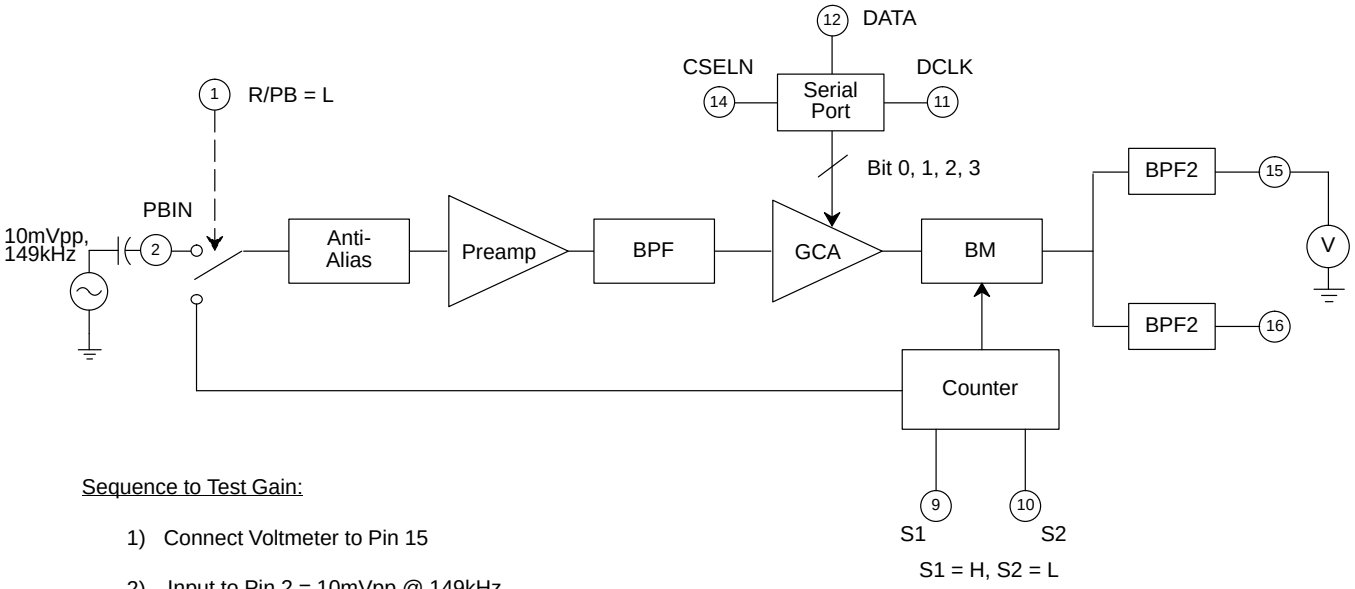


Figure 4. Tests: PBF_1, PBF_2, PBF_3, PBF_4, SB10K, SB500K

Symbol	PBIN Input Condition	S1	S2	Measurement Pin
GBP2M	10mVpp, 165kHz	L	L	15
GBP1M	10mVpp, 165kHz	L	H	16
GBP21	10mVpp, 139kHz	L	L	15
GBP22	10mVpp, 120kHz	L	L	15
GBP11	10mVpp, 132kHz	L	L	16
GBP12	10mVpp, 115kHz	L	L	16
GBP13	10mVpp, 88kHz	L	L	16

Table 7.



Sequence to Test Gain:

1) Connect Voltmeter to Pin 15

2) Input to Pin 2 = 10mVpp @ 149kHz
S1 = H and S2 = L (to get 16kHz signal)

3) Follow Timing Diagram
CSEL Low --> Set Data --> Then Clock --> CSEL High

4) GCA # Gain = 20 log $(\frac{V_{OUT}}{V_{IN}})$ - GCA(0)

5) GCA(0) = 20 log $(\frac{V_{OUT}}{V_{IN}})$ with Bits 0,1,2,3 = Low

Figure 5. Test: GCA # Gain

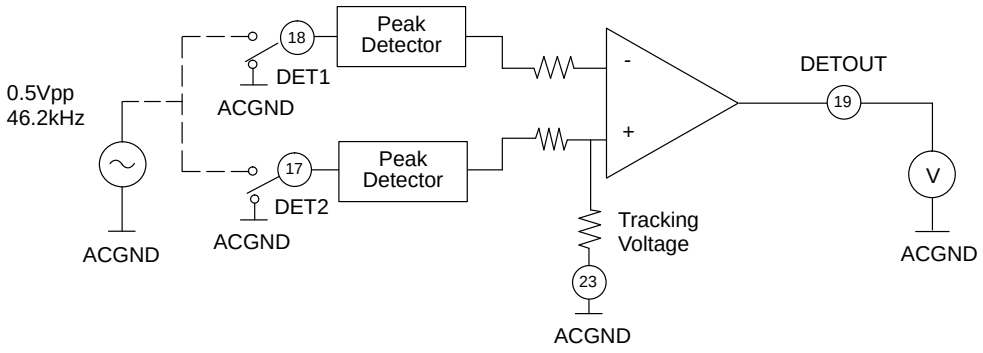


Figure 6. Tests: DETOSØ (As Shown)
DETOS1 (Connect dashed CKT and MEAS)

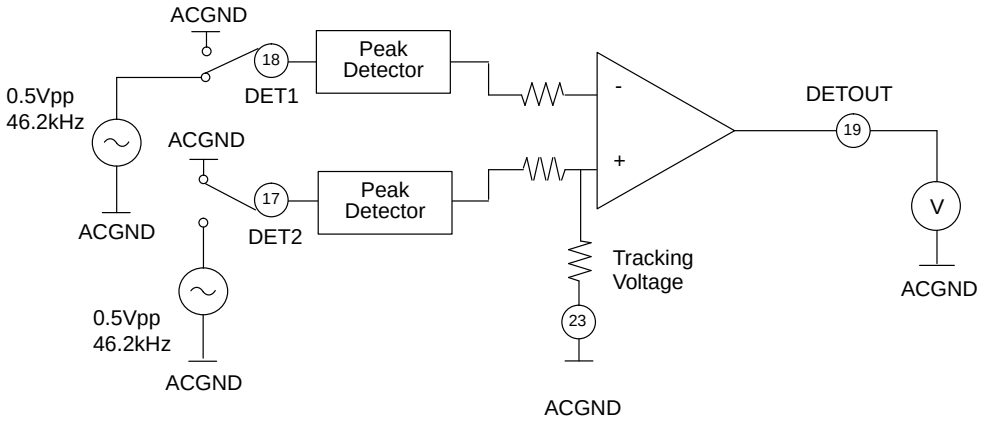


Figure 7. Test: DET1 (As Shown)
DET2 (Switches Turned The Other Way)

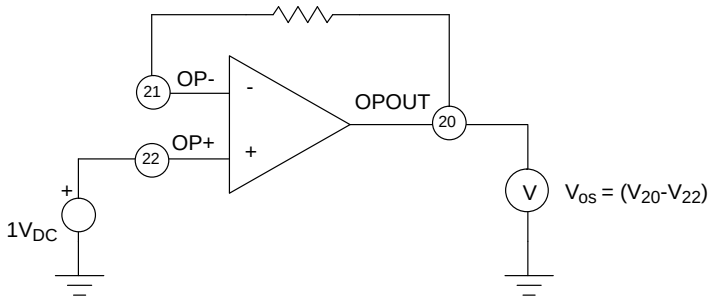
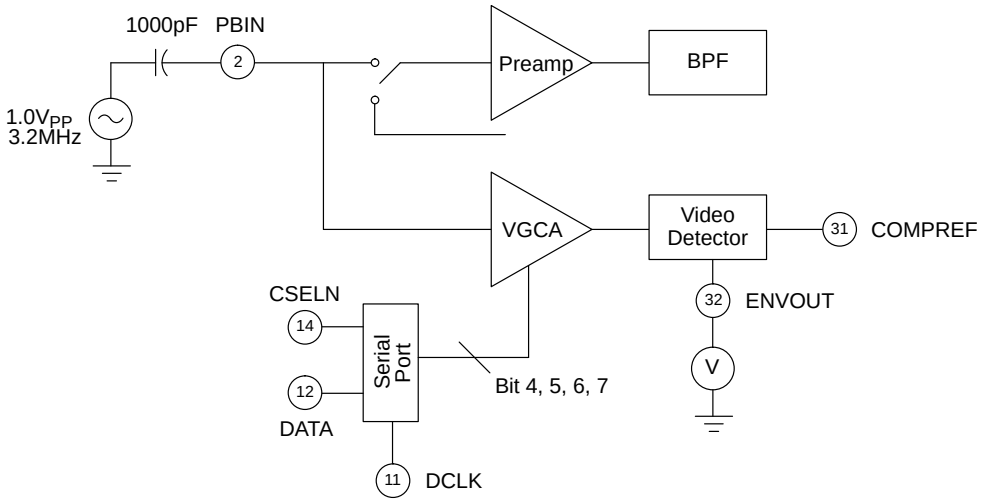


Figure 8. Test: VOSOP



*Follow Timing Diagram
CSEL Low → Set Data → Then Clock → CSEL High

Figure 9. Test: VGCA GAIN #

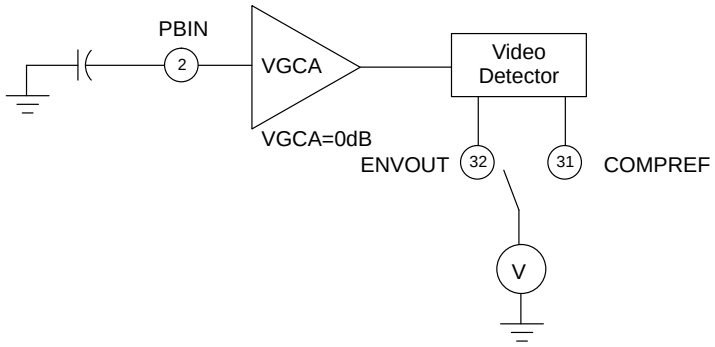
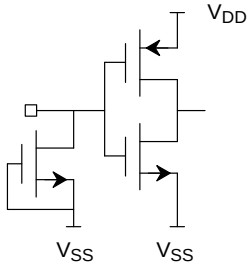
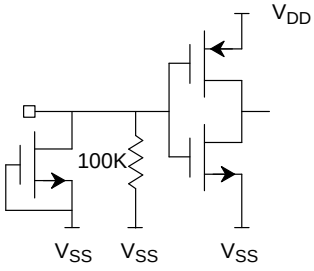
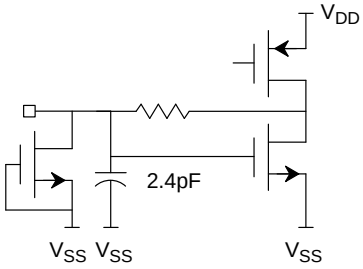
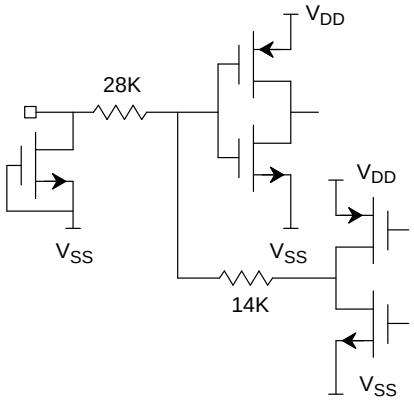
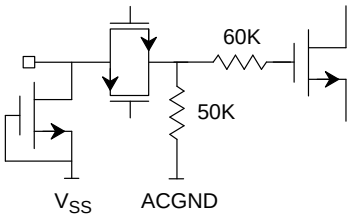
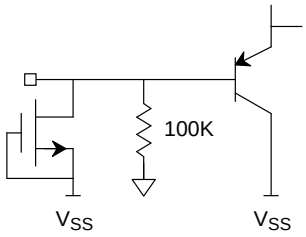
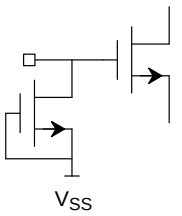
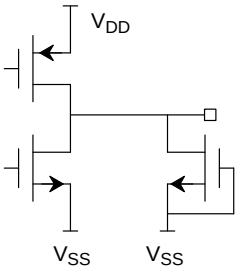
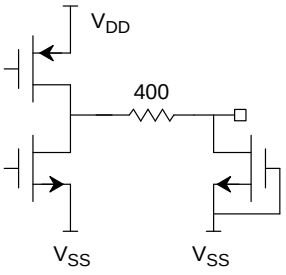
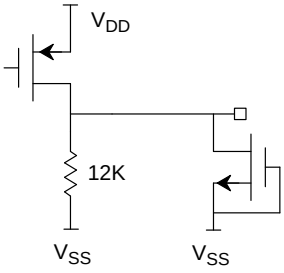
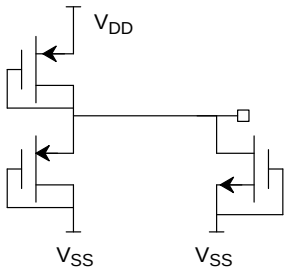
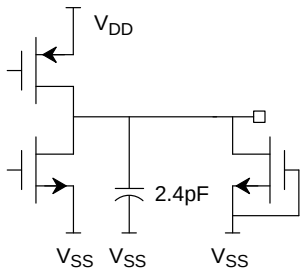


Figure 10. Tests: ENVOUT and COMPREF

Pin #	Symbol	I/O	Equivalent Circuit	Description
1 9 10 11 12	R/PB S1 S2 DCLK DATA	I		Record Playback Select Control F1-F4 Frequency Control F1-F4 Frequency Control Clock in Serial Port Data in Serial Port
14	CSELN	I		Serial Port Enable
7	CLKIN	I		Clock Input
23	TRACKING	I		DC Reference for Detector
2	PBIN	I		Composite Video Input

Pin #	Symbol	I/O	Equivalent Circuit	Description
17 18	DET2 DET1	I		Input for 47 kHz Detector Input for 16 kHz Detector
26 30 21 22 27	SP/LP MODRAT OP– OP+ CLOGREF	I		SP/LP Trip Point Reference Modulation Ratio Control Op Amp Negative Input Op Amp Positive Input CLOG Trip Point Reference
15 16 19 20 25 28 29	BPFOUT2 BPFOUT1 DETOUT OPOUT ACGND CLOG PB_SP/LP	O		Output of 16 kHz Bandpass Filter Output of 47 kHz Bandpass Filter Detector Output Op Amp Output AC Ground Output CLOG Output PB_SP/LP
5	RECPILOT	O		Sinewave Output in Record Mode
31 32	COMPREF ENVOUT	O		Video DC Reference Video Detected Output

Pin #	Symbol	I/O	Equivalent Circuit	Description
4	$V_{DD}/2$	O		Analog Reference Filter Point
8	CLKOUT	O		Clock Output

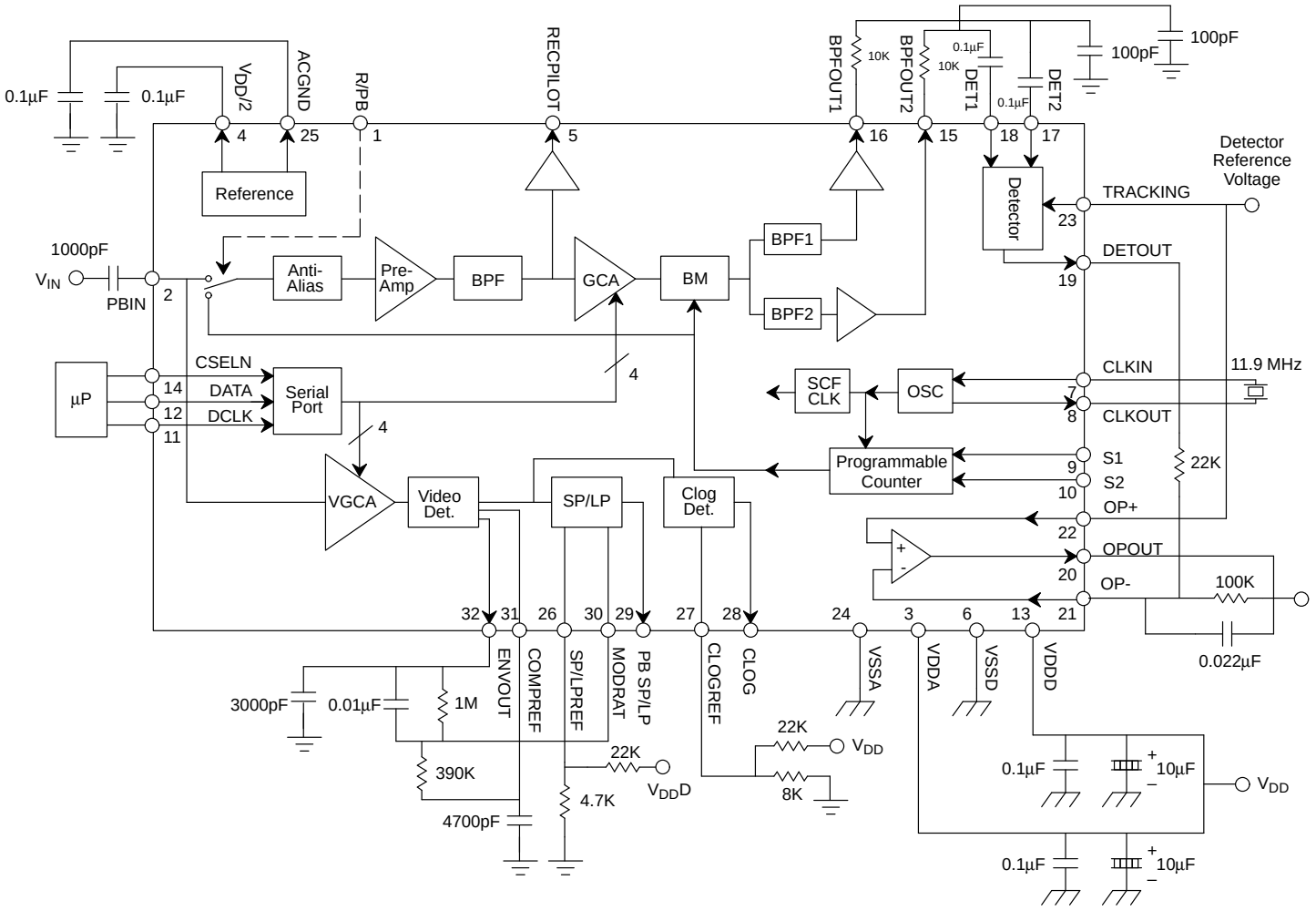
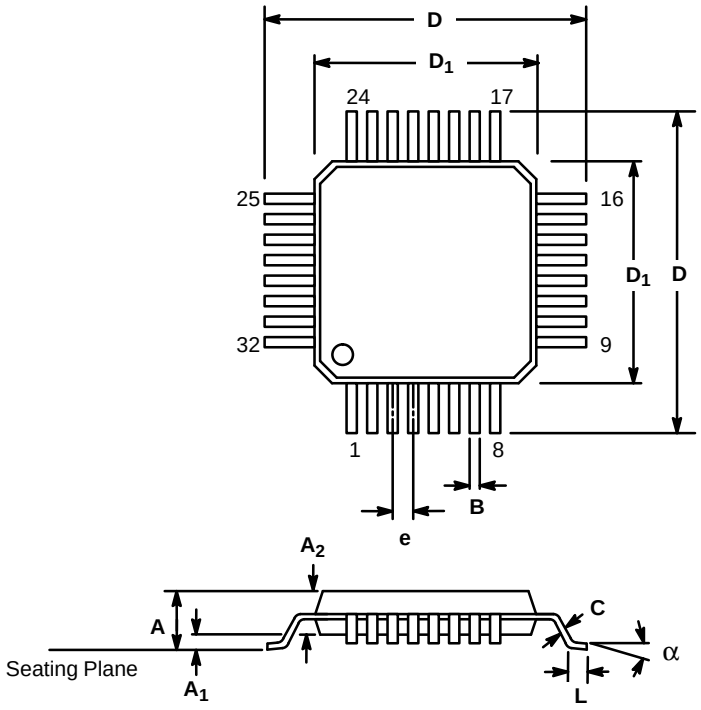


Figure 11. Application Diagram

32 LEAD PLASTIC QUAD FLAT PACK (7 x 7 x 1.4 mm QFP)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.012	0.018	0.30	0.45
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.0315 BSC		0.80 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

Notes

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