8K X 8 CMOS Electrically Erasable PROM
6ms Nonvolatile Write Cycle

FEATURES

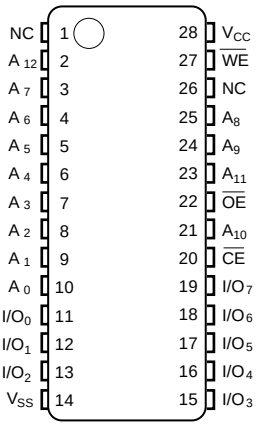
- **Fast Read Access Times**
  - **— 150ns, 200ns and 250ns**
- **Low CMOS Power Consumption**
  - **— 60mA (Active)**
  - **— 200μA (Standby)**
- **5 Volt-only Operation**
  - **— Including write**
- **Fast Nonvolatile Write Cycle**
  - **— Internally latched data and address**
  - **— 120ns byte-load cycle**
  - **— 10ms (max.) nonvolatile write cycle**
  - **— Automatic erase before write**
- **Software Mode Control**
- **On-chip Inadvertent Write Protection**
- **Unlimited Read Cycle Endurance**
- **100,000 Erase/Write Cycles Typical**
- **100 Year Secure Data Retention**
- **$\overline{\text{DATA}}$ Polling to Minimize Write Cycle Time**
- **Automatic Page Write**
  - **— 1 to 64 Bytes in 6ms (max.)**
- **ESD Protected to 2000V**

OVERVIEW

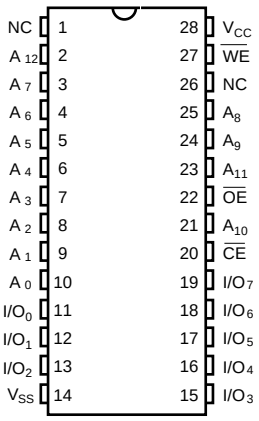
The XL28C64B is a full-featured, 8K x 8 bit CMOS E^2PROM (Electrically Erasable Programmable Read Only Memory). Operationally, it is compatible with industry standard 64K devices, but offers improved speed and power efficiency. Read access times can be as low as 150ns; standby current, less than 200μA. It features a page-wide input buffer and improved protection against inadvertent writes. The XL28C64B is manufactured with EXEL's proven double-metal, CMOS process.

PIN CONFIGURATIONS

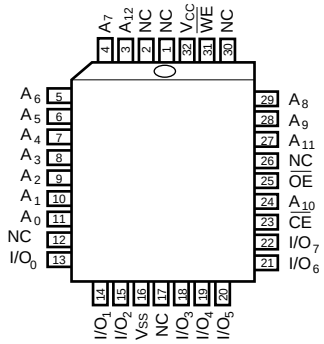
28 pin SOIC
Type "J" Package



28 pin Plastic DIP
Type "P" Package



32 pin PLCC
Type "D" Package



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PIN NAMES

A_0-A_{12}	Address Inputs
I/O_0- I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Power and Signal Ground
NC	No Connect

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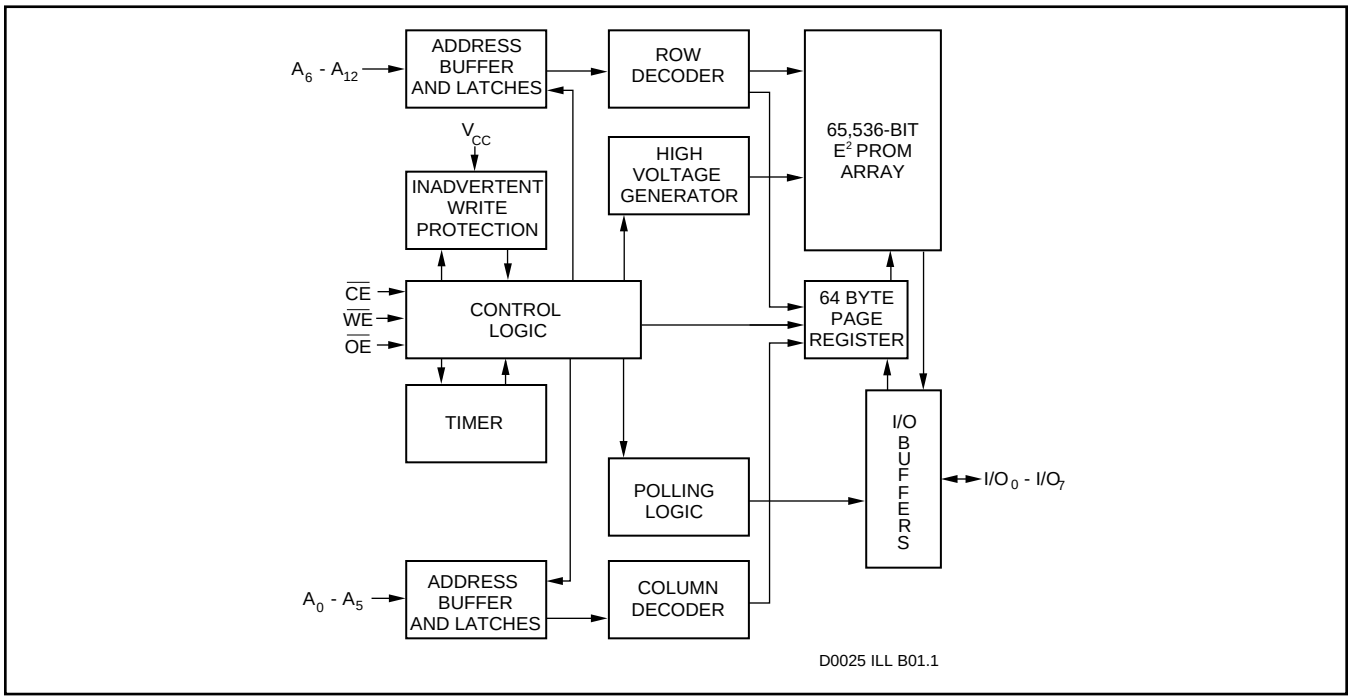
BLOCK DIAGRAM



The sophisticated architecture of this device provides complete and automatic control of the nonvolatile write cycle, eliminating the need for external timers, latches, high voltage generators and supplemental inadvertent write protection circuitry. It fits into standard SRAM sockets and responds to typical SRAM write commands.

The fully-automatic, 64-byte, page-write allows the entire memory to be programmed in less than 0.65 sec. Internal latches, for address and data, free the system bus during the 6ms self-timed, nonvolatile write period. Moreover, the byte-load cycle time matches the read access time, adding to system performance.

Inadvertent writes are inhibited by a wide range of protections built into the XL28C64B. A low V_{CC} lockout feature disables nonvolatile write cycles when V_{CC} drops below 3.5V (V_{WI}) (typical). Additionally, the XL28C64B features power-on reset and noise protected $\overline{WE}$.

The XL28C64B is compatible with existing 64K E^2PROMs—both pinout and operating modes conform to industry standards. This compatibility extends to higher and lower density E^2PROMs as well.

APPLICATIONS

The nonvolatile storage in the XL28C64B can deliver firmware for booting up systems, and for operating industrial and process controllers, traffic controllers, robotics and telemetry, measuring instruments and appliance controls. It can retain phone numbers and messages in telephones and facsimile machines. The XL28C64B is ideal in applications that are self-adapting, such as video games and systems that require automatic re-calibration, as well as those that are subject to power failures.

ENDURANCE and DATA RETENTION

The XL28C64B is designed for applications requiring up to 100,000 data changes. It provides 100 years of secure data retention, with or without power applied after the data is written.

DEVICE OPERATION-NORMAL MODE

Three control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$) select all standard user-operating modes for the XL28C64B. Chip erase (typically executed during test procedures) requires a higher supply voltage on the $\overline{OE}$ input pin. This conforms with existing E^2PROM standards. (Contact EXEL for details on the Chip Erase Mode).

Read Mode
Data is read from the XL28C64B by bringing both $\overline{CE}$ and $\overline{OE}$ LOW while keeping $\overline{WE}$ HIGH. (See Figure 3). With the read mode selected, address lines can be changed at any time, in any order to read data at various locations in the E^2PROM array. Read access time is measured from the time when the final controlling line ($\overline{CE}$ or $\overline{OE}$) goes LOW (t_{CE} or t_{OE}), or the time when the address is established (t_{AA}).

The device can be read an unlimited number of times, because the stored charge that defines the bit state is not affected by a read cycle.

Write Mode
The XL28C64B uses a two-step process to store new data. Byte-load cycles fill latches in a volatile page buffer. A subsequent nonvolatile write cycle transfers this data in the page-buffer to the E^2PROM array without user intervention.

The XL28C64B contains (128) 64-byte pages. Address lines A_6-A_{12} identify the page; lines A_0-A_5 identify the byte within the page. All bytes written within one nonvolatile write cycle must be on the same page (A_6-A_{12} must remain unchanged). Any number of the 64 bytes in the page can be written or re-written, in any order; the last data written to any given byte when the nonvolatile write cycle begins is retained. An internal byte flag set for each corresponding byte flag written, identifying the newly written byte in a page.

Either $\overline{WE}$ or $\overline{CE}$ can be used to initiate the byte-load cycle. The address is latched into internal address latches upon the last falling edge of $\overline{WE}$ or $\overline{CE}$. An internal byte-load timer is started on the falling edge of the controlling line. The timer provides a 100µs window for initiating the next byte-load cycle. Byte-loading can continue indefinitely if each new load cycle is started within the timeout period. Please note that all write cycles require $\overline{OE}$ to be held HIGH (see Figure 4, 5, and 6).

When the byte-load timer times out, additional external byte-load cycles are ignored and data is automatically transferred from the page buffer to the E^2PROM array through an internally managed nonvolatile write cycle. Byte flags ensure that high voltage is applied only to newly written bytes. By avoiding the unnecessary cycling of unwritten bytes, the overall endurance of the array can be extended.

An internal write-flag is set on the first byte-load of each write cycle. Data pins remain in a high impedance state except during a byte-load (when they contain the forced input data) or during a $\overline{DATA}$ polling read (see below). When the high voltage cycle is completed, the write-flag is reset and the operating mode is again determined by the control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$).

Output Disable Mode
While in the read mode, if $\overline{OE}$ is brought HIGH, the device remains in the read mode, but with the outputs disabled. (I/O pins are in a highimpedance state.)

Standby Mode
Whenever $\overline{CE}$ is brought HIGH, the device operates in standby mode, with the I/O pins in a high impedance state. Standby power dissipation is less than 200µA with CMOS level inputs. While $\overline{CE}$ remains HIGH, all other input pins are disabled, insulating the device from any activity on the system bus.

Chip Erase — High Voltage Mode
The chip erase mode allows the user to erase the entire E^2PROM array with a single command. The method requires the application of high voltage (V_H) on the $\overline{OE}$ pin, with $\overline{CE}$ at a logical "0." Chip erase is initiated by a standard byte write command, but in this case, the data on the I/O pins is ignored. A byte containing all "1's" is automatically written to all locations in the E^2PROM array. (Refer to the Mode Selection chart.)

DEVICE OPERATION - Software Data Protection

The XL28C64B offers software data protection (SDP) a JEDEC standard method of protecting the contents of the memory. During power transitions the control inputs to the XL28C64B could possibly produce the conditions necessary for initiating an unwanted write cycle. This is called an inadvertent write and can generally be eliminated through careful external circuit design. The best assurance for protecting against an inadvertent write is SDP. Once this feature is enabled, the XL28C64B will be protected during device operation and during power transitions.

Set Software Data Protect

To enable software data protect the XL28C64B must be written with a three byte command sequence as shown in Figure 1. The system can immediately exit from the routine after writing the three bytes and the XL28C64B will be protected after t_{WC}. That is, any attempts to write to the device will be ignored.

Data can still be written to the device but only under a controlled sequence of events. First the set data protect command sequence is issued; then, within t_{BLC} data may be written in the normal manner (either single or multiple bytes) to the device.

Disable Data Protect

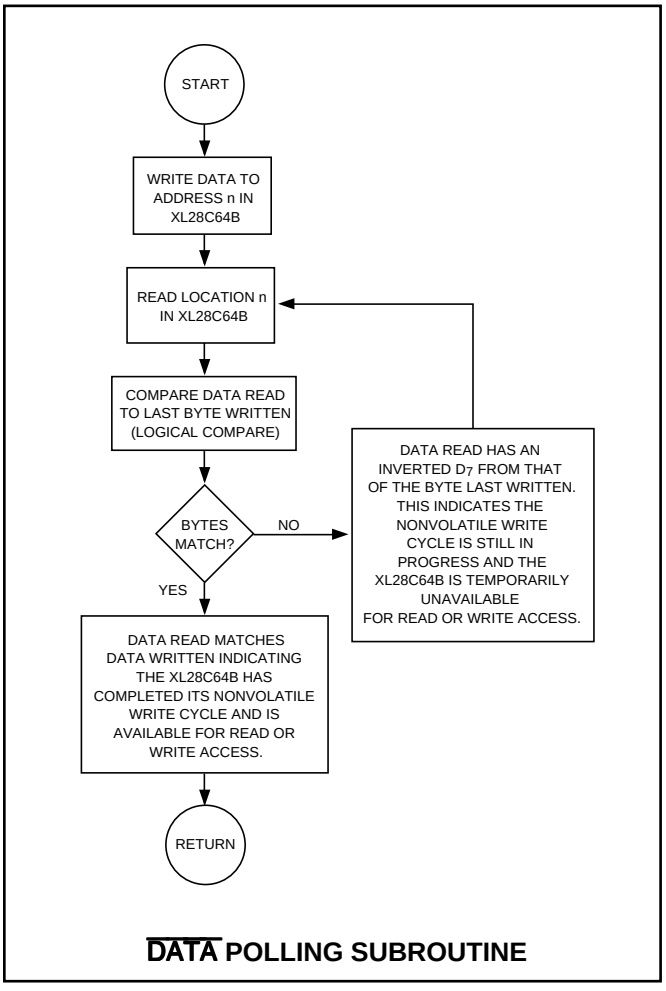
Even though the need for disabling SDP is rare the six byte command sequence, illustrated in Figure 2, will disable the feature.

SDP Notes: The addresses used in the command sequence can be written with data. All write operations within the command sequence and any subsequent data writes must conform to the page write timing limits.

$\overline{\text{DATA}}$ Polling

The XL28C64B provides DATA polling as a means to detect the early completion of a write cycle. The write cycle is specified as a max 5ms but it is generally faster. The host system can take advantage of the faster typical write cycle by implementing a $\overline{\text{DATA}}$ polling routine.

After a write operation and before the completion of the internal write cycle, any attempt to read the XL28C64B will return the complement of the last data written on I/O7. That is if the data written on I/O7 was a logic “1,” any attempt to read the last address written would return a logic “0” on I/O7. Likewise, if the data written on I/O7 was a logic “0,” any attempt to read the last address would return a logic “1” on I/O7. Once the data reads true, the internal write cycle is complete and a valid read or write operation may be initiated.



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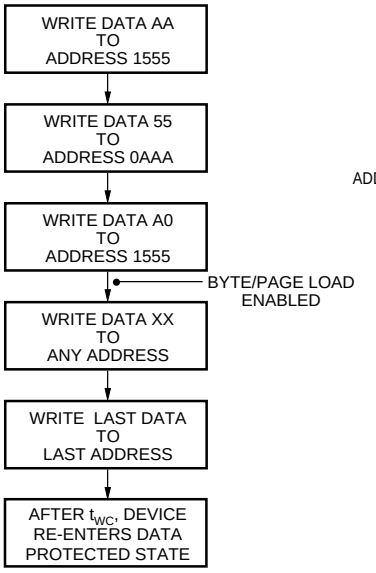
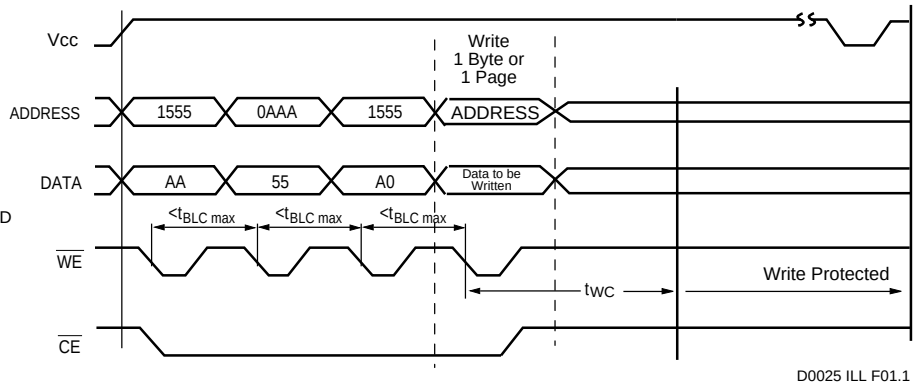
Write Sequence for **Setting** Software Data Protection

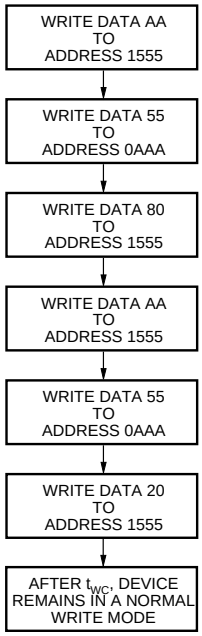


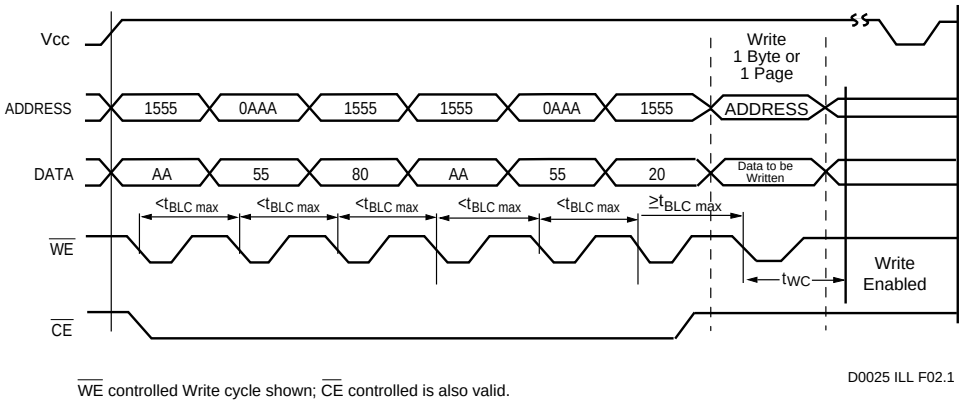


WE controlled Write cycle shown; CE controlled is also valid.

FIGURE 1. WRITE SEQUENCE FOR SETTING SOFTWARE DATA PROTECTION

Write Sequence for **Disabling** Software Data Protection





WE controlled Write cycle shown; CE controlled is also valid.

FIGURE 2. WRITE SEQUENCE FOR DISABLING SOFTWARE DATA PROTECTION

WRITE PROTECT MECHANISMS

The XL28C64B features several integrated mechanisms to protect it from inadvertent writes that might occur during system power supply transitions or periods of system noise.

$\overline{OE}$ Write Inhibit

If $\overline{OE}$ is brought LOW before the $\overline{CE}$ and $\overline{WE}$ write command sequence, the internal nonvolatile write cycle will not occur, (See the Mode Selection Table below). In addition to the user-controlled protection mechanisms, the following specialized circuits are built in.

V_{CC} Lockout

The XL28C64B has a specialized power supply monitor circuit integrated to protect the device from inadvertent write commands asserted by the system during low V_{CC} conditions. This circuitry constantly evaluates the power supply voltage level applied to the XL28C64B and actively inhibits the initiation of nonvolatile write cycles if the applied supply voltage falls below V_{WI}. This circuitry does not abort nor affect nonvolatile write cycles already in progress, but inhibits new cycles from being initiated.

Power-Up Write Enable Delay

At power on, operation is inhibited until V_{CC} is stable and sufficiently high. Write operations are inhibited until 20ms after V_{CC} reaches 3.0V to allow the system to stabilize while blocking potential inadvertent write commands.

Noise Protection

Write pulses of less than 10ns duration on the $\overline{WE}$ pin will not initiate nonvolatile write cycles.

Data Protection Mode (Software Controlled)

The XL28C64B can be placed in a write-disabled mode through software control.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⌐└─┘	Byte Write ($\overline{WE}$ Controlled)	D_{IN}	Active
⌐└─┘	V_{IH}	V_{IL}	Byte Write ($\overline{CE}$ Controlled)	D_{IN}	Active
V_{IL}	V_H	V_{IL}	Chip Erase*	Data In = X	Active
V_{IH}	X	X	Standby	HIGH Z	Standby
X	V_{IL}	X	Write Inhibit	X	Active

*Contact EXEL for details.

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ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias XLS28C64B ..... 0°C to +70°C
XLE28C64B ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin* ..... -0.3 to V_{CC} +0.3
Voltage on $\overline{OE}$ Pin* ..... -0.3 to +13V
ESD Rating 2000V
*With respect to ground

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability. Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to avoid any voltages higher than the rated maxima.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS28C64B, V_{CC} = 5V ±10%
T_A = -40°C to +85°C for the XLE28C64B, V_{CC} = 5V ±10%

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{CC}	V_{CC} Current — Active (TTL)	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH} I/O's = open A_0-A_{12} toggling at 5MHz		60	mA
I_{SB}	V_{CC} Current — Standby (TTL)	$\overline{CE}$ = $\overline{WE}$ = V_{IH} $\overline{OE}$ = V_{IL} I/O's = open A_0-A_{12} = V_{CC}		2	mA
I_{SBC}	V_{CC} Current — Standby (CMOS)	$\overline{CE}$ = $\overline{WE}$ ≥ V_{CC}-.2V $\overline{OE}$ = ≤V_{SS}+0.2V I/O's = open A_0-A_{12} = V_{CC}		200	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to Vcc		10	µA
I_{LO}	Output Leakage — Standby	V_{OUT} = GND to Vcc $\overline{CE}$ = V_{IH}		10	µA
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2.0	Vcc + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA I_{OH} = -10µA	2.4 Vcc-0.1		V
V_{IOI}	Write Lockout Voltage		3.2	4.4	V

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CAPACITANCE

T_A = 25°C, f = 1.0MHz

Symbol	Test	Test Conditions	Max.	Units
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF

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AC OPERATING CHARACTERISTICS READ CYCLE (See Figure 3)
T_A= 0°C to +70°C for the XLS28C64B, V_{CC}=5V±10%
T_A= -40°C to +85°C for the XLE28C64B, V_{CC}=5V±10%

Symbol	Test	XLS28C64B-150 ONLY		XLS28C64B-200 / XLE28C64B-200		XLS28C64B-250 / XLE28C64B-250		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	150		200		250		ns
t_{AA}	Address Access Time		150		200		250	ns
t_{CE}	Chip Enable Access Time		150		200		250	ns
t_{OE}	Output Enable Access Time		60		75		100	ns
t_{LZ}	Chip Enable to Output in Low Z	0		0		0		ns
t_{HZ}	Chip Disable to Output in High Z	0	50	0	50	0	50	ns
t_{OLZ}	Output Enable to Output in Low Z	0		0		0		ns
t_{OHZ}	Output Disable to Output in High Z	0	50	0	50	0	50	ns
t_{OH}	Output Hold from Address Change	15		15		15		ns

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WRITE CYCLE (See Figures 4, 5 and 6)
T_A= 0°C to +70°C for the XLS28C64B, V_{CC}=5V±10%
T_A= -40°C to +85°C for the XLE28C64B, V_{CC}=5V±10%

Symbol	Test	Min.	Max.	Units
t_{WC}	Write Cycle Time		10	ms
t_{BLC}	Byte Load Cycle	.120	150	µs
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	35		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	Chip Enable Pulse Width	50		ns
t_{OES}	Output Enable Setup Time	5		ns
t_{OEH}	Output Enable Hold Time	5		ns
t_{WP}	Write Enable Pulse Width	70		ns
t_{WPH}	Write Pulse Width High	50		ns
t_{DS}	Data Setup Time	30		ns
t_{DH}	Data Hold Time	0		ns
t_{DV}	Data Valid Time		1	µs
t_{INIT}	Power-up Initialization Period		20	ms

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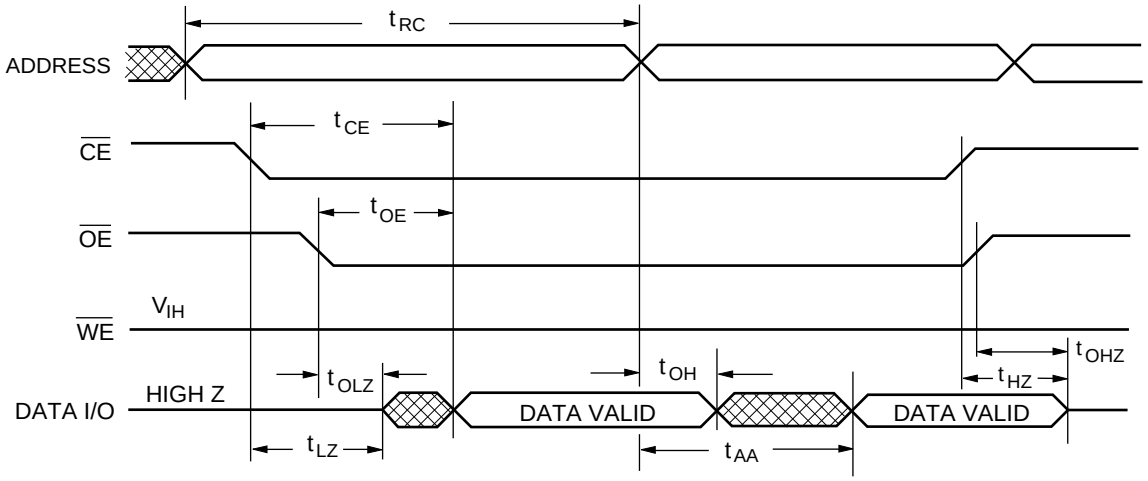

FIGURE 3. READ CYCLE TIMING

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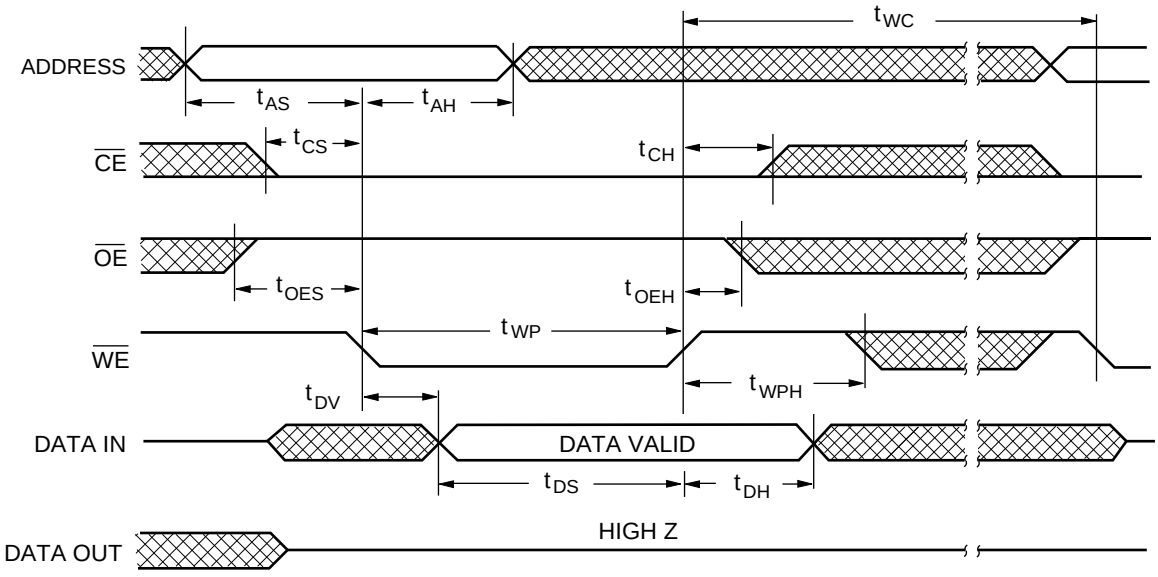

FIGURE 4. $\overline{WE}$ CONTROLLED WRITE CYCLE TIMING

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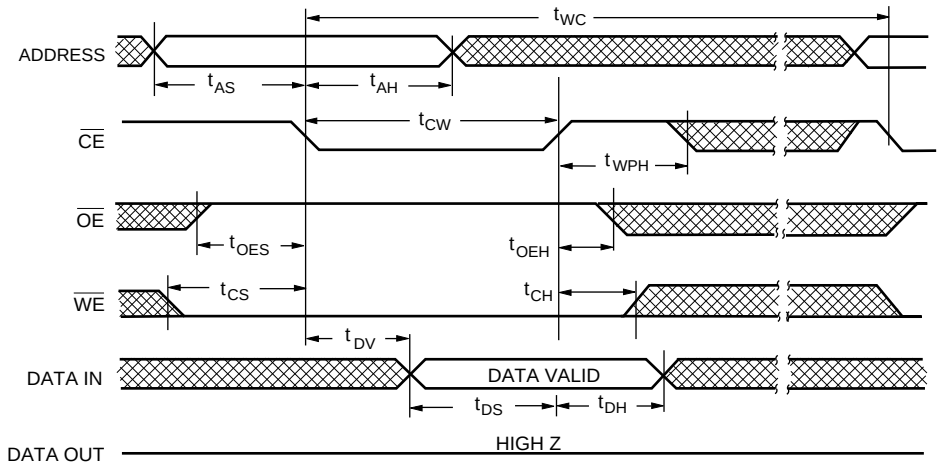

FIGURE 5. $\overline{CE}$ CONTROLLED WRITE CYCLE TIMING

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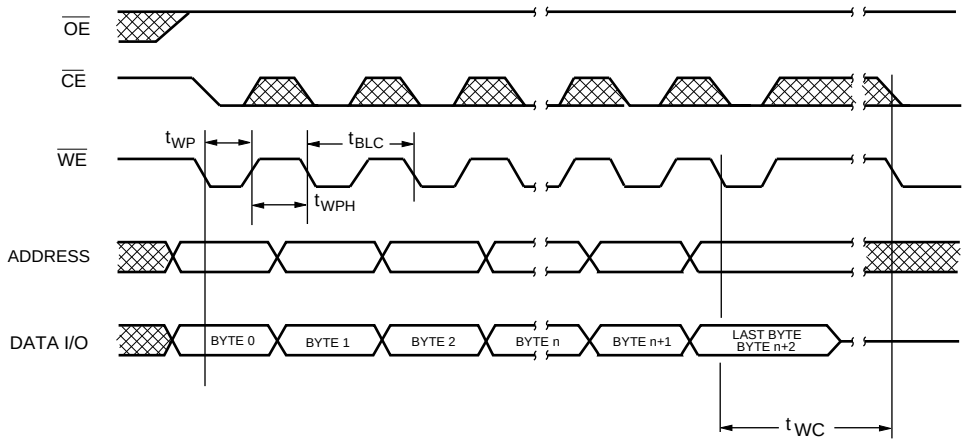

FIGURE 6. PAGE MODE WRITE CYCLE TIMING

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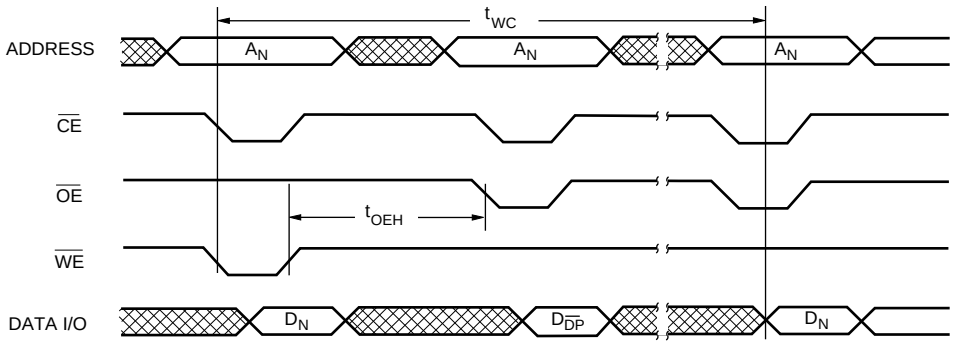

FIGURE 7. $\overline{DATA}$ POLLING TIMING

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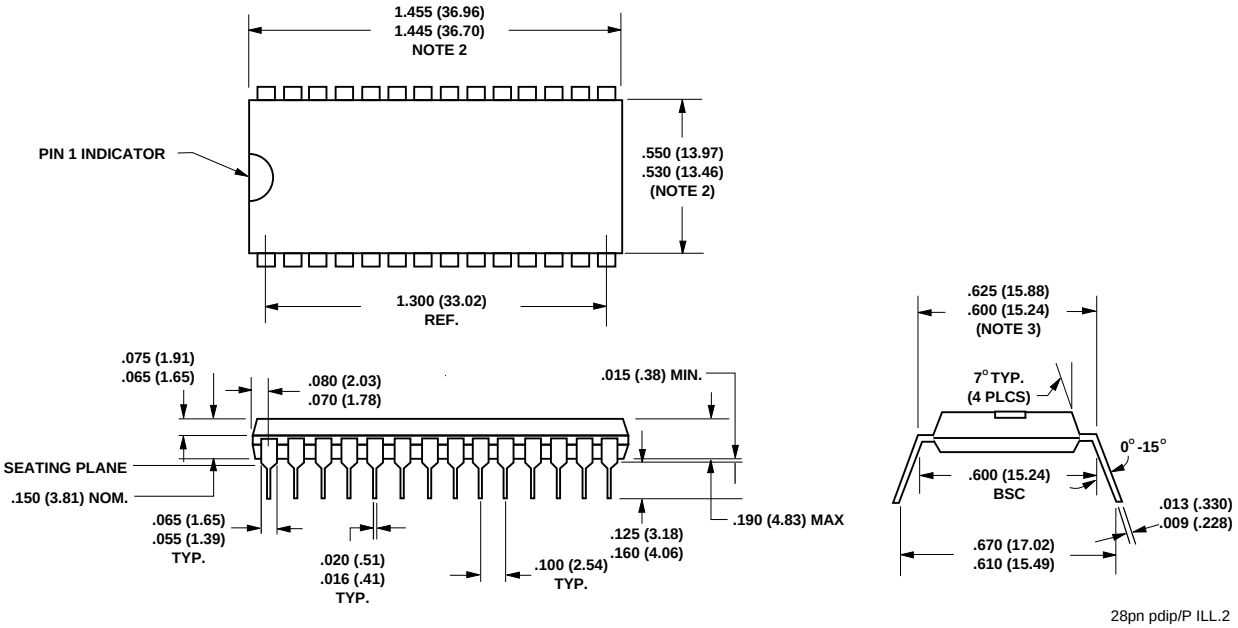
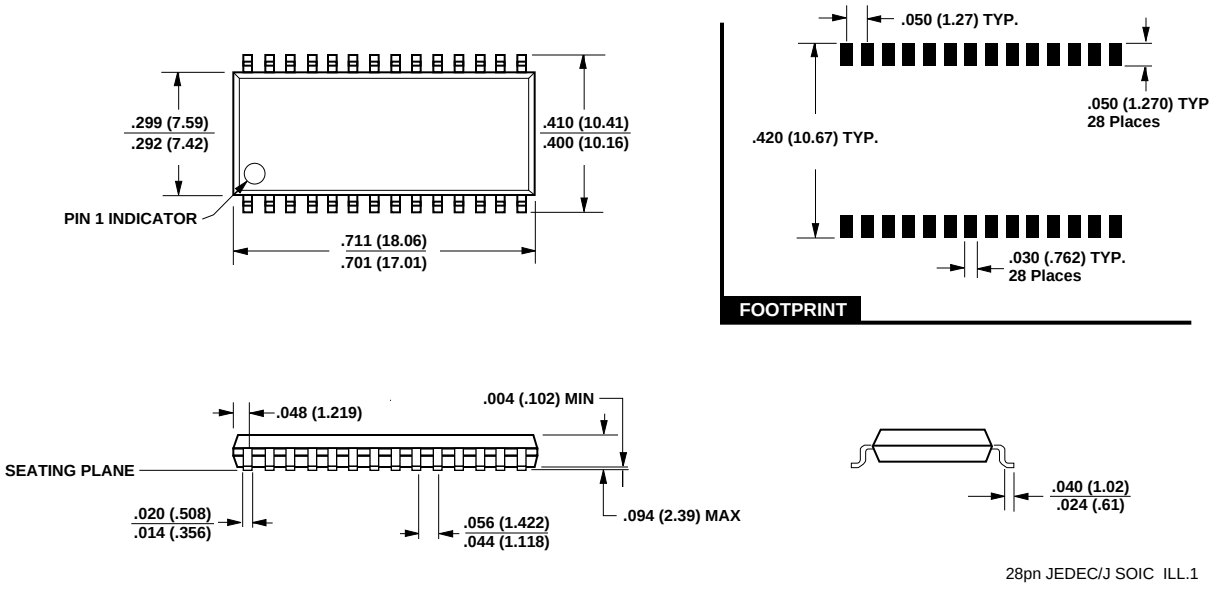
PACKAGE DIAGRAMS

28-pin Plastic DIP (Type “P”) Package



28pn pdip/P ILL.2

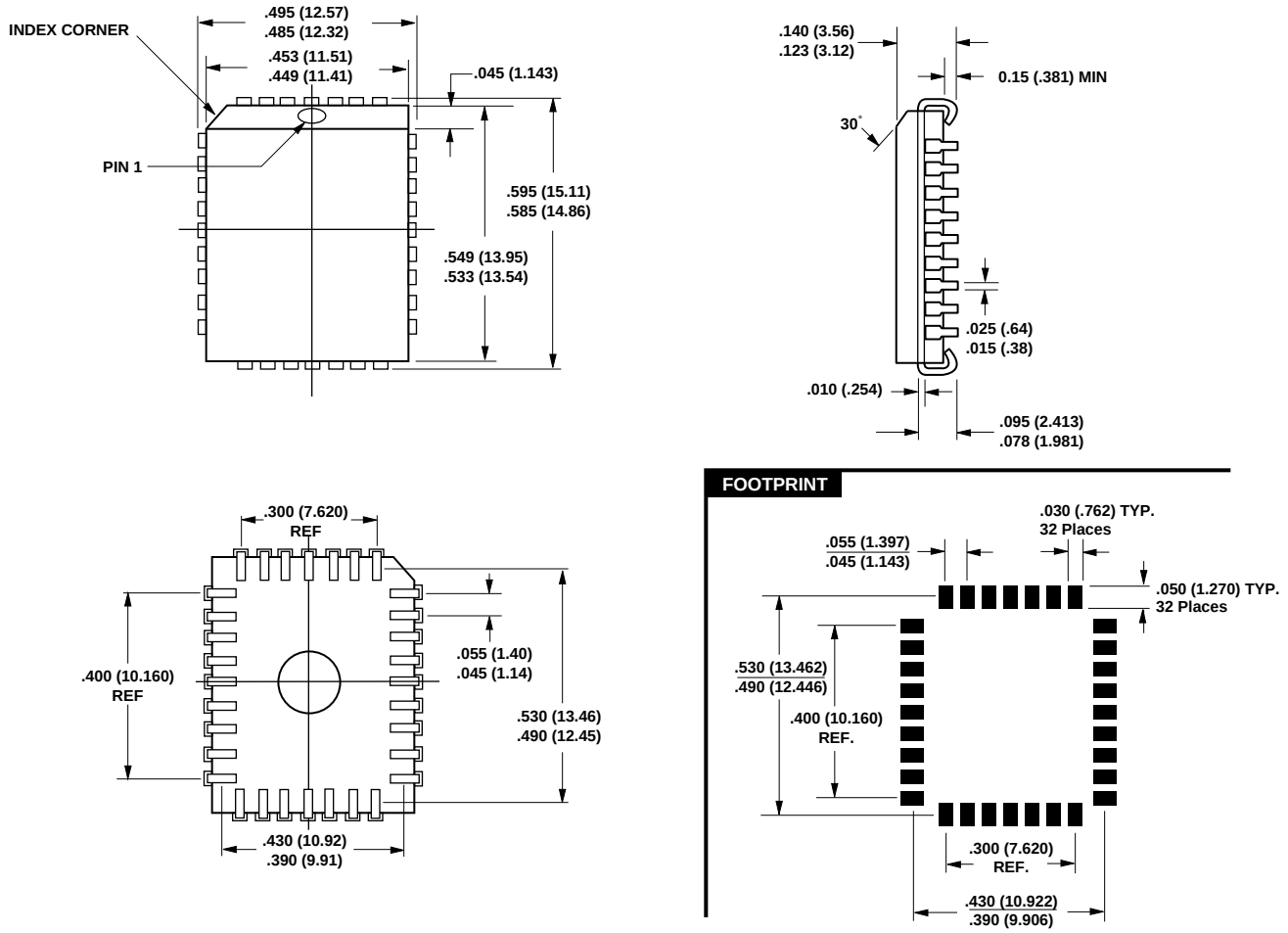
28-pin SOIC (Type “J”) Package



28pn JEDEC/J SOIC ILL.1

PACKAGE DIAGRAMS (Continued)

32-pin PLCC (Type “D”) Package



32pn plcc/D ILL.1

ORDERING INFORMATION

Standard Configurations

Prefix	Temperature Range*	Part Type	Package Type*	Access Time
XL	S, E	28C64B	D, J, P	150, 200, 250

*Contact EXEL for your special temperature and packaging requirements.

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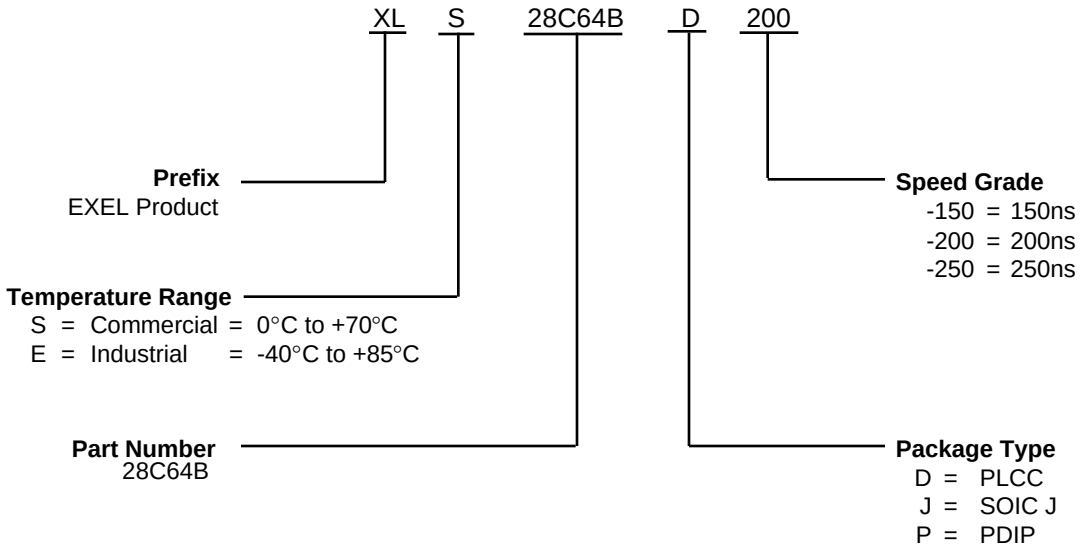
Part Numbers:



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